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Introduction

The Xilinx® LogiCORE™ AXI Verification IP (VIP) core has been developed to support the simulation of customer designed AXI-based IP. The AXI VIP core supports three versions of the AXI protocol (AXI3, AXI4, and AXI4-Lite).

The AXI VIP is unencrypted SystemVerilog source that is comprised of a SystemVerilog class library and synthesizeable RTL.

The embedded RTL interface is controlled by the AXI VIP through a virtual interface. AXI transactions are constructed in the customer’s verification environment and passed to the AXI driver class. The driver class then manages the timing and drives the content on the interface.

Features

- Supports all protocol data widths, address widths, transfer types, and responses
- Transaction-level protocol checking (burst type, length, size, lock type, and cache type)
- ARM®-based protocol transaction level checker for tools that support assertion property [Ref 1]
- Behavioral SystemVerilog Syntax
- SystemVerilog class-based API
- Synthesizes to nets and constant tie-offs

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</tr>
<tr>
<td>Synthesis</td>
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Support

Provided by Xilinx at the Xilinx Support web page

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
3. This IP does not deliver VIP for Zynq PS. It only delivers the VIP core for AXI3, AXI4, and AXI4-Lite interfaces.
4. To take advantage of the full features of this IP, it requires simulators supporting advanced simulation capabilities.
5. The AXI VIP can only act as a protocol checker when contained within a VHDL hierarchy.
6. Do not import two different revisions/versions of the axi_vip packages. This causes elaboration failures.
7. All AXI VIP and parents to the AXI VIP must be upgraded to the latest version.
Chapter 1

Overview

The Xilinx® LogiCORE™ AXI Verification IP (VIP) core is used in the following manner:

- Generating master AXI commands and write payload
- Generating slave AXI read payload and write responses
- Checking protocol compliance of AXI transactions

The AXI VIP can be configured in three different modes:

- AXI master VIP
- AXI slave VIP
- AXI pass-through VIP

Figure 1-1 shows the AXI master VIP which generates AXI commands and write payload and sends it to the AXI system.

Figure 1-2 shows the AXI slave VIP which responds to the AXI commands and generates read payload and write responses.
Figure 1-3 shows the AXI pass-through VIP which protocol checks all AXI transactions that pass through it. The IP can be configured to behave in the following modes:

- Monitor only
- Master
- Slave

The AXI protocol checker does not exist in the synthesized netlist.

[Diagram of AXI Pass-Through VIP]

**Feature Summary**

- Supports AXI3, AXI4, or AXI4-Lite interface
- Configurable as an AXI master, AXI slave, and in pass-through mode
- Configurable simulation messaging
- Provides simulation AXI protocol checking

**Applications**

The AXI VIP is for verification and system engineers who want to:

- Monitor transactions between two AXI connections
- Generate AXI transactions
- Check for AXI protocol compliance

**IMPORTANT:** When using the Vivado® simulator, the AXI Protocol Checker IP [Ref 3] is used in place of the ARM AMBA Assertions.
Licensing and Ordering

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.
Chapter 2

Product Specification

The AXI VIP core supports the AXI3, AXI4, and AXI4-Lite protocols.

Standards

The AXI interfaces conform to the ARM® Advanced Microcontroller Bus Architecture (AMBA®) AXI version 4 specification [Ref 2], including the AXI4-Lite control register interface subset.

Performance

The AXI VIP core synthesizes to wires and does not impact performance.

User Parameters

Table 2-1 shows the AXI VIP core user parameters.

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Format/Range</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROTOCOL</td>
<td>Type: string Value range: AXI4, AXI3, AXI4LITE</td>
<td>AXI4</td>
<td>Used to enable protocol specific signals.</td>
</tr>
<tr>
<td>INTERFACE_MODE</td>
<td>Type: string Value range: PASS_THROUGH, MASTER, SLAVE</td>
<td>PASS_THROUGH</td>
<td>Used to control the mode of protocol to be configured as master, slave, or pass-through.</td>
</tr>
<tr>
<td>READ_WRITE_MODE</td>
<td>Type: string Value range: READ_WRITE, READ_ONLY, WRITE_ONLY</td>
<td>READ_WRITE</td>
<td>Used to enable the corresponding AXI read/write signals.</td>
</tr>
<tr>
<td>Parameter Name</td>
<td>Format/Range</td>
<td>Default Value</td>
<td>Description</td>
</tr>
<tr>
<td>---------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>---------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>ADDR_WIDTH</td>
<td>1 ≤ integer ≤ 64 (AXI4LITE) 12 ≤ integer ≤ 64 (AXI4/AXI3)</td>
<td>32</td>
<td>Width of *<em>axi</em>{ar,aw}addr;</td>
</tr>
<tr>
<td>DATA_WIDTH</td>
<td>Type: long Value range: 32, 64, 128, 256, 512, 1024 AXI4LITE: 32, 64</td>
<td>32</td>
<td>Width of the *_axi_wdata and *_axi_rdata</td>
</tr>
<tr>
<td>ID_WIDTH</td>
<td>Type: long Value range: 0..32 AXI4LITE: 0</td>
<td>0</td>
<td>Width of the *<em>axi</em>{aw,ar,r,b}id. When the VIP is configured for AXI3 use, this parameter also controls the width of *_axi_wid.</td>
</tr>
<tr>
<td>AWUSER_WIDTH</td>
<td>Type: long Value range: 0..1024 AXI4LITE: 0 READ_ONLY: 0</td>
<td>0</td>
<td>Width of the *_axi_awuser</td>
</tr>
<tr>
<td>ARUSER_WIDTH</td>
<td>Type: long Value range: 0..1024 AXI4LITE: 0 WRITE_ONLY: 0</td>
<td>0</td>
<td>Width of the *_axi_aruser</td>
</tr>
<tr>
<td>WUSER_WIDTH</td>
<td>Type: long Value range: 0..1024 AXI4LITE: 0 READ_ONLY: 0</td>
<td>0</td>
<td>Width of the *_axi_wuser</td>
</tr>
<tr>
<td>BUSER_WIDTH</td>
<td>Type: long Value range: 0..1024 AXI4LITE: 0 READ_ONLY: 0</td>
<td>0</td>
<td>Width of the *_axi_buser</td>
</tr>
<tr>
<td>RUSER_WIDTH</td>
<td>Type: long Value range: 0..1024 AXI4LITE: 0 WRITE_ONLY: 0</td>
<td>0</td>
<td>Width of the *_axi_ruser</td>
</tr>
<tr>
<td>SUPPORTS_NARROW</td>
<td>Type: long Value range: 0,1 AXI4LITE: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arsize and *_axi_awsize. When it is 0, *_axi_arsize and *_axi_awsize values are log2(DATA_WIDTH/8).</td>
</tr>
<tr>
<td>HAS_BURST</td>
<td>Type: long Value range: 0,1 AXI4LITE: 0</td>
<td>2'b01</td>
<td>Used to control the enablement of the *_axi_arburst and *_axi_awburst. When it is 0, *_axi_arburst and *_axi_awburst values are 2'b01.</td>
</tr>
<tr>
<td>HAS_LOCK</td>
<td>Type: long Value range: 0, 1 AXI4LITE: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arlock and *_axi_awlock. When it is 0, *_axi_arlock and *_axi_awlock values are 0.</td>
</tr>
</tbody>
</table>
### Table 2-1: AXI VIP User Parameters (Cont’d)

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Format/Range</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HAS_CACHE</td>
<td>Type: long Value range: 0, 1 AXI4LITE: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arcache and *_axi_awcache. When it is 0, *_axi_arcache and *_axi_awcache values are 0.</td>
</tr>
<tr>
<td>HAS_REGION</td>
<td>Type: long Value range: 0, 1 AXI4LITE/AXI3: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arregion and *_axi_awregion. When it is 0, *_axi_arregion and *_axi_awregion values are 0.</td>
</tr>
<tr>
<td>HAS_PROT</td>
<td>Type: long Value range: 0, 1 AXI4LITE/AXI3: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arprot and *_axi_awprot. When it is 0, *_axi_arprot and *_axi_awprot values are 0.</td>
</tr>
<tr>
<td>HAS_QOS</td>
<td>Type: long Value range: 0, 1 AXI4LITE/AXI3: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_arqos and *_axi_awqos. When it is 0, *_axi_arqos and *_axi_awqos values are 0.</td>
</tr>
<tr>
<td>HAS_WSTRB</td>
<td>Type: long Value range: 0, 1 READ_ONLY: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_wstrb. When HAS_BURST or SUPPORTS_NARROW(1) is 1, HAS_WSTRB must be 1. When it is 0, all bits of *_axi_wstrb are 1.</td>
</tr>
<tr>
<td>HAS_BRESP</td>
<td>Type: long Value range: 0, 1 READ_ONLY: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_bresp. When HAS_LOCK is 1, HAS_BRESP must also be 1. When it is 0, *_axi_bresp value is 0.</td>
</tr>
<tr>
<td>HAS_RRESP</td>
<td>Type: long Value range: (0, 1) WRITE_ONLY: 0</td>
<td>1</td>
<td>Used to control the enablement of the *_axi_rresp. When HAS_LOCK is 1, HAS_RRESP must also be 1. When it is 0, *_axi_rresp value is 0.</td>
</tr>
<tr>
<td>HAS_ACLKEN</td>
<td>Type: long Value range: (0, 1)</td>
<td>0</td>
<td>Used to control the enablement of the ACLKEN port. User parameter only. When it is 0, it is treated as 1.</td>
</tr>
<tr>
<td>HAS_USER_BITS_PER_BYTE</td>
<td>Type: long Value range: (0, 1) AXI4LITE: 0</td>
<td>1</td>
<td>Used to control whether write/read user bits per byte is 1 or 0. 1: user bits per byte, this means ruser/wuser size are per byte based 0: user bits per transfer, this means ruser/wuser size are per transfer based</td>
</tr>
<tr>
<td>WUSER_BITS_PER_BYTE</td>
<td>Type: long Value range: (0, 32) AXI4LITE: 0 READ_ONLY: 0</td>
<td>0</td>
<td>When HAS_USER_BITS_PER_BYTE is 1, then the value of WUSER is calculated. WUSER_WIDTH = WUSER_BITS_PER_BYTE * (DATA_WIDTH/8).</td>
</tr>
</tbody>
</table>
Table 2-2 shows the AXI VIP independent port descriptions.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>aclk</td>
<td>I</td>
<td>1</td>
<td>Interface clock input</td>
<td></td>
</tr>
<tr>
<td>aresetn</td>
<td>I</td>
<td>1</td>
<td>Interface reset input (active-Low)</td>
<td>HAS_ARESETN == 1</td>
</tr>
<tr>
<td>aclken</td>
<td>I</td>
<td>1</td>
<td>Interface Clock enable signal. (active-High)</td>
<td>HAS_ACLKEN == 1</td>
</tr>
</tbody>
</table>

Table 2-3 lists the interface signals for the AXI VIP core in master or pass-through mode. The m_axi_aw*, m_axi_w*, and m_axi_b* signals are not shown on the port list when the READ_WRITE MODE parameter is READ_ONLY. The m_axi_ar* and m_axi_r* signals are not shown on the port list when the READ_WRITE MODE parameter is WRITE_ONLY. See the AXI specification for port definitions.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>AXI4</th>
<th>AXI3</th>
<th>AXI4-LITE</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>m_axi_awid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>ID_WIDTH</td>
<td>Write Address Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_awaddr</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>ADDR_WIDTH</td>
<td>Write Address Channel Transaction Address (12-64)</td>
<td></td>
</tr>
<tr>
<td>m_axi_awlen</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>8 for AXI4 4 for AXI3</td>
<td>Write Address Channel Transaction Burst Length (0-255)</td>
<td></td>
</tr>
<tr>
<td>m_axi_awsize</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>3</td>
<td>Write Address Channel Transfer Size Code (0-7)</td>
<td>SUPPORTS_NARROW[1] == 1</td>
</tr>
<tr>
<td>m_axi_awburst</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>2</td>
<td>Write Address Channel Burst Type Code (0-2)</td>
<td>HAS_BURST == 1</td>
</tr>
<tr>
<td>m_axi_awlock</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>2 for AXI4 1 for AXI3</td>
<td>Write Address Channel Atomic Access Type (0-1)</td>
<td>HAS_LOCK == 1</td>
</tr>
</tbody>
</table>
## Chapter 2: Product Specification

### Table 2-3: AXI Master or Pass-Through VIP Port Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>AXI4</th>
<th>AXI3</th>
<th>AXI4-LITE</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>m_axi_awcache</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>4</td>
<td>Write Address Channel Cache Characteristics</td>
<td>HAS_CAHCE == 1</td>
</tr>
<tr>
<td>m_axi_awprot</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>3</td>
<td>Write Address Channel Protection Characteristics</td>
<td>HAS_PROT == 1</td>
</tr>
<tr>
<td>m_axi_awqos</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Write Address Channel Quality of Service</td>
<td>HAS_QOS == 1</td>
</tr>
<tr>
<td>m_axi_awregion</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Write Address Channel Region Index</td>
<td>HAS_REGION == 1</td>
</tr>
<tr>
<td>m_axi_awuser</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
<td>Write Address Channel User-defined signals</td>
<td>AWUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_awvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>1</td>
<td>Write Address Channel Valid</td>
<td></td>
</tr>
<tr>
<td>m_axi_awready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td></td>
<td>1</td>
<td>Write Address Channel Ready</td>
<td></td>
</tr>
<tr>
<td>m_axi_arid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td></td>
<td>Read Address Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_araddr</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>ADDR_WIDTH</td>
<td>Read Address Channel Transaction Address (12-64)</td>
<td></td>
</tr>
<tr>
<td>m_axi_arlen</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>8 for AXI4 4 for AXI3</td>
<td>Read Address Channel Transaction Burst Length (0-255)</td>
<td>Always ON AXI4/AXI3</td>
</tr>
<tr>
<td>m_axi_arsize</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>3</td>
<td>Read Address Channel Transfer Size Code (0-7)</td>
<td>SUPPORTS_NARROW[1] == 1</td>
</tr>
<tr>
<td>m_axi_arburst</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>2</td>
<td>Read Address Channel Burst Type Code (0-2)</td>
<td>HAS_BURST == 1</td>
</tr>
<tr>
<td>m_axi_arlock</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>2 for AXI4 1 for AXI3</td>
<td>Read Address Channel Atomic Access Type (0-1)</td>
<td>HAS_LOCK == 1</td>
</tr>
<tr>
<td>m_axi_arcache</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>4</td>
<td>Read Address Channel Cache Characteristics</td>
<td>HAS_CAHCE == 1</td>
</tr>
<tr>
<td>m_axi_arprot</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>3</td>
<td>Read Address Channel Protection Characteristics</td>
<td>HAS_PROT == 1</td>
</tr>
<tr>
<td>m_axi_arqos</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Read Address Channel Quality of Service</td>
<td>HAS_QOS == 1</td>
</tr>
<tr>
<td>m_axi_arregion</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Read Address Channel Region Index</td>
<td>HAS_REGION == 1</td>
</tr>
<tr>
<td>m_axi_aruser</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>ARUSER_WIDTH</td>
<td>Read Address Channel User-defined signals.</td>
<td>AWUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_arvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>1</td>
<td>Read Address Channel Valid</td>
<td></td>
</tr>
<tr>
<td>m_axi_arready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td></td>
<td>1</td>
<td>Read Address Channel Ready</td>
<td></td>
</tr>
<tr>
<td>m_axi_wid</td>
<td>O</td>
<td>x</td>
<td></td>
<td></td>
<td>ID_WIDTH</td>
<td>Write Data Channel Last Data Beat</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_wlast</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td></td>
<td>1</td>
<td>Write Data Channel Last Data Beat</td>
<td></td>
</tr>
</tbody>
</table>

[1]: AXI4-LITE only supports 32-bit narrow transactions.
### Table 2-3: AXI Master or Pass-Through VIP Port Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>AXI4</th>
<th>AXI3</th>
<th>AXI4-LITE</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>m_axi_wdata</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>DATA_WIDTH</td>
<td>Write Data Channel Data</td>
<td></td>
</tr>
<tr>
<td>m_axi_wstrb</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>DATA_WIDTH/8</td>
<td>Write Data Channel Byte Strobes</td>
<td>HAS_WSTRB == 1</td>
</tr>
<tr>
<td>m_axi_wuser</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>WUSER_WIDTH</td>
<td></td>
<td>Write Data Channel user-defined signal</td>
<td>WUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_wvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Data Channel Valid</td>
<td></td>
</tr>
<tr>
<td>m_axi_wready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Data Channel Ready</td>
<td></td>
</tr>
<tr>
<td>m_axi_rid</td>
<td>O</td>
<td>x</td>
<td></td>
<td>ID_WIDTH</td>
<td></td>
<td>Read Data Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_rlast</td>
<td>O</td>
<td>x</td>
<td></td>
<td>1</td>
<td></td>
<td>Read Data Channel Last Data Beat</td>
<td></td>
</tr>
<tr>
<td>m_axi_rdata</td>
<td>O</td>
<td>x</td>
<td></td>
<td>x</td>
<td>DATA_WIDTH</td>
<td>Read Data Channel Data</td>
<td></td>
</tr>
<tr>
<td>m_axi_rresp</td>
<td>O</td>
<td>x</td>
<td></td>
<td>x</td>
<td>2</td>
<td>Read Data Channel Response Code (0-3)</td>
<td>HAS_RRESP == 1</td>
</tr>
<tr>
<td>m_axi_ruser</td>
<td>O</td>
<td>x</td>
<td></td>
<td>RUSER_WIDTH</td>
<td></td>
<td>Read Data Channel user-defined signal</td>
<td>RUSER_WIDTH&gt; 0</td>
</tr>
<tr>
<td>m_axi_rvalid</td>
<td>O</td>
<td>x</td>
<td></td>
<td>x</td>
<td>1</td>
<td>Read Data Channel Valid</td>
<td></td>
</tr>
<tr>
<td>m_axi_rready</td>
<td>I</td>
<td>x</td>
<td></td>
<td>x</td>
<td>1</td>
<td>Read Data Channel Ready</td>
<td></td>
</tr>
<tr>
<td>m_axi_bid</td>
<td>O</td>
<td>x</td>
<td></td>
<td>ID_WIDTH</td>
<td></td>
<td>Write Response Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>m_axi_bresp</td>
<td>O</td>
<td>x</td>
<td></td>
<td>x</td>
<td>2</td>
<td>Write Response Channel Response Code (0-3)</td>
<td>HAS_BRESP &gt; 0</td>
</tr>
<tr>
<td>m_axi_buser</td>
<td>O</td>
<td>x</td>
<td></td>
<td>BUSER_WIDTH</td>
<td></td>
<td>Write Response Channel user-defined signal</td>
<td>BUSER_WIDTH&gt; 0</td>
</tr>
<tr>
<td>m_axi_bvalid</td>
<td>O</td>
<td>x</td>
<td></td>
<td>x</td>
<td>1</td>
<td>Write Response Channel Valid</td>
<td></td>
</tr>
<tr>
<td>m_axi_bready</td>
<td>I</td>
<td>x</td>
<td></td>
<td>x</td>
<td>1</td>
<td>Write Response Channel Ready</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. SUPPORTS_NARROW is treated as SUPPORTS_NARROW_BURST in Vivado IP integrator.
Table 2-4 lists the interface signals for the AXI VIP core when it has been configured to be in slave or pass-through mode.

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>AXI4</th>
<th>AXI3</th>
<th>AXI4-LITE</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>s_axi_awid</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>ID_WIDTH</td>
<td>Write Address Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_awaddr</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>ADDR_WIDTH</td>
<td>Write Address Channel Transaction Address (12-64)</td>
<td></td>
</tr>
<tr>
<td>s_axi_awlen</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>8 for AXI4 4 for AXI3</td>
<td>Write Address Channel Transaction Burst Length (0-255)</td>
<td></td>
</tr>
<tr>
<td>s_axi_awsize</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>3</td>
<td>Write Address Channel Transfer Size Code (0-7)</td>
<td>SUPPORTS_NARROW[1] == 1</td>
</tr>
<tr>
<td>s_axi_awburst</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>2</td>
<td>Write Address Channel Burst Type Code (0-2)</td>
<td>HAS_BURST == 1</td>
</tr>
<tr>
<td>s_axi_awlock</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>2 for AXI4 1 for AXI3</td>
<td>Write Address Channel Atomic Access Type (0-1)</td>
<td>HAS_LOCK == 1</td>
</tr>
<tr>
<td>s_axi_awcache</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>4</td>
<td>Write Address Channel Cache Characteristics</td>
<td>HAS_CACHE == 1</td>
</tr>
<tr>
<td>s_axi_awprot</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>3</td>
<td>Write Address Channel Protection Characteristics</td>
<td>HAS_PROT == 1</td>
</tr>
<tr>
<td>s_axi_awqos</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Write Address Channel Quality of Service</td>
<td>HAS_QOS == 1</td>
</tr>
<tr>
<td>s_axi_awregion</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>4</td>
<td>Write Address Channel Region Index</td>
<td>HAS_REGION== 1</td>
</tr>
<tr>
<td>s_axi_awuser</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>AWUSER_WIDTH</td>
<td>Write Address Channel User-defined signals</td>
<td>AWUSER_WIDTH&gt; 0</td>
</tr>
<tr>
<td>s_axi_awvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Address Channel Valid</td>
<td></td>
</tr>
<tr>
<td>s_axi_awready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Address Channel Ready</td>
<td></td>
</tr>
<tr>
<td>s_axi_arid</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>ID_WIDTH</td>
<td>Read Address Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_araddr</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>ADDR_WIDTH</td>
<td>Read Address Channel Transaction Address (12-64)</td>
<td></td>
</tr>
<tr>
<td>s_axi_arlen</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>8 for AXI4 4 for AXI3</td>
<td>Read Address Channel Transaction Burst Length (0-255)</td>
<td></td>
</tr>
<tr>
<td>s_axi_arsize</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>3</td>
<td>Read Address Channel Transfer Size Code (0-7)</td>
<td>SUPPORTS_NARROW[1] == 1</td>
</tr>
<tr>
<td>s_axi_arburst</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>2</td>
<td>Read Address Channel Burst Type Code (0-2)</td>
<td>HAS_BURST == 1</td>
</tr>
<tr>
<td>s_axi_arlock</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>2 for AXI4 1 for AXI3</td>
<td>Read Address Channel Atomic Access Type (0-1)</td>
<td>HAS_LOCK == 1</td>
</tr>
</tbody>
</table>
**Table 2-4: AXI Slave or Pass-Through VIP Port Descriptions (Cont’d)**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>I/O</th>
<th>AXI4</th>
<th>AXI3</th>
<th>Width</th>
<th>Description</th>
<th>Enablement</th>
</tr>
</thead>
<tbody>
<tr>
<td>s_axi_arcache</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>4</td>
<td>Read Address Channel Cache Characteristics</td>
<td>HAS_CAHCE == 1</td>
</tr>
<tr>
<td>s_axi_arprot</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>3</td>
<td>Read Address Channel Protection Characteristics</td>
<td>HAS_PROT == 1</td>
</tr>
<tr>
<td>s_axi_arqos</td>
<td>I</td>
<td>x</td>
<td></td>
<td>4</td>
<td>Read Address Channel Quality of Service</td>
<td>HAS_QOS == 1</td>
</tr>
<tr>
<td>s_axi_arregion</td>
<td>I</td>
<td>x</td>
<td></td>
<td>4</td>
<td>Read Address Channel Region Index</td>
<td>HAS_REGION == 1</td>
</tr>
<tr>
<td>s_axi_aruser</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>Read Address Channel User-defined signals</td>
<td>AWUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_arvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Read Address Channel Valid</td>
<td></td>
</tr>
<tr>
<td>s_axi_arready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Read Address Channel Ready</td>
<td></td>
</tr>
<tr>
<td>s_axi_wid</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>Write Data Channel</td>
<td>ID_WIDTH</td>
</tr>
<tr>
<td>s_axi_wlast</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Data Channel Last Data Beat</td>
<td></td>
</tr>
<tr>
<td>s_axi_wdata</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td></td>
<td>Write Data Channel Data</td>
<td></td>
</tr>
<tr>
<td>s_axi_wstrb</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td></td>
<td>Write Data Channel Byte Strobes</td>
<td>HAS_WSTRB == 1</td>
</tr>
<tr>
<td>s_axi_wuser</td>
<td>I</td>
<td>x</td>
<td></td>
<td></td>
<td>Write Data Channel User-defined signal</td>
<td>WUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_wvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Data Channel Valid</td>
<td></td>
</tr>
<tr>
<td>s_axi_wready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Write Data Channel Ready</td>
<td></td>
</tr>
<tr>
<td>s_axi_rid</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>ID_WIDTH</td>
<td>Read Data Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_rlast</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Read Data Channel Last Data Beat</td>
<td></td>
</tr>
<tr>
<td>s_axi_rdata</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>DATA_WIDTH</td>
<td>Read Data Channel Data</td>
<td></td>
</tr>
<tr>
<td>s_axi_rresp</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>2</td>
<td>Read Data Channel Response Code (0-3)</td>
<td>HAS_RRESP == 1</td>
</tr>
<tr>
<td>s_axi_ruser</td>
<td>I</td>
<td>x</td>
<td></td>
<td>RUSER_WIDTH</td>
<td>Read Data Channel User-defined signal</td>
<td>RUSER_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_rvalid</td>
<td>O</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Read Data Channel Valid</td>
<td></td>
</tr>
<tr>
<td>s_axi_rready</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>Read Data Channel Ready</td>
<td></td>
</tr>
<tr>
<td>s_axi_bid</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>ID_WIDTH</td>
<td>Write Response Channel Transaction ID</td>
<td>ID_WIDTH &gt; 0</td>
</tr>
<tr>
<td>s_axi_bresp</td>
<td>I</td>
<td>x</td>
<td>x</td>
<td>2</td>
<td>Write Response Channel Response Code (0-3)</td>
<td>HAS_BRESP &gt; 0</td>
</tr>
</tbody>
</table>
Table 2-5: AXI Protocol Checks and Descriptions

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI_ERRM_AWADDR_BOUNDARY</td>
<td>AXI4/AXI3</td>
<td>A write burst cannot cross a 4 KB boundary.</td>
</tr>
<tr>
<td>AXI_ERRM_AWADDR_WRAP_ALIGN</td>
<td>AXI4/AXI3</td>
<td>A write transaction with burst type WRAP has an aligned address.</td>
</tr>
<tr>
<td>AXI_ERRM_AWBURST</td>
<td>AXI4/AXI3</td>
<td>A value of 2'b11 on AWBURST is not permitted when AWVALID is High.</td>
</tr>
<tr>
<td>AXI_ERRM_AWLEN_LOCK</td>
<td>AXI4/AXI3</td>
<td>Exclusive access transactions cannot have a length greater than 16 beats.</td>
</tr>
<tr>
<td>AXI_ERRM_AWCACHE</td>
<td>AXI4/AXI3</td>
<td>If not cacheable (AWCACHE[1] == 1'b0), AWCACHE = 2'b00.</td>
</tr>
<tr>
<td>AXI_ERRM_AWLEN_FIXED</td>
<td>AXI4/AXI3</td>
<td>Transactions of burst type FIXED cannot have a length greater than 16 beats.</td>
</tr>
<tr>
<td>AXI_ERRM_AWLEN_WRAP</td>
<td>AXI4/AXI3</td>
<td>A write transaction with burst type WRAP has a length of 2, 4, 8, or 16.</td>
</tr>
<tr>
<td>AXI_ERRM_AWSIZE</td>
<td>AXI4/AXI3</td>
<td>The size of a write transfer does not exceed the width of the data interface.</td>
</tr>
<tr>
<td>AXI_ERRM_AWVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>AWVALID is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>AXI_ERRM_AWADDR_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Handshake Checks AWADDR must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWBURST_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks A WBURST must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWCACHE_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWCACHE must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
</tbody>
</table>

Notes:
1. SUPPORTS_NARROW is treated as SUPPORTS_NARROW_BURST in Vivado IP integrator.

AXI Protocol Checks and Descriptions

Table 2-5 lists the AXI protocol checks and descriptions which are essentially the same as the assertions that are found in the AXI Protocol Checker LogiCORE IP Product Guide (PG101) [Ref 3].
### Table 2-5: AXI Protocol Checks and Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI_ERRM_AWID_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWID must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWLEN_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWLEN must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWLOCK_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWLOCK must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWPROT_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Handshake Checks AWPROT must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWSIZE_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWSIZE must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWQOS_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks AWQOS must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWREGION_STABLE</td>
<td>AXI4</td>
<td>Handshake Checks AWREGION must remain stable when ARVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_AWVALID_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Handshake Checks Once AWVALID is asserted, it must remain asserted until AWREADY is High.</td>
</tr>
<tr>
<td>AXI_RECS_AWREADY_MAX_WAIT</td>
<td>AXI4/AXI3/Lite</td>
<td>Recommended that AWREADY is asserted within MAXWAITS cycles of AWVALID being asserted.</td>
</tr>
</tbody>
</table>
| AXI_ERRM_WDATA_NUM                  | AXI4/AXI3        | The number of write data items matches AWLEN for the corresponding address. This is triggered when any of the following occurs:  
  - Write data arrives and WLAST is set, and the WDATA count is not equal to AWLEN  
  - Write data arrives and WLAST is not set, and the WDATA count is equal to AWLEN  
  - ADDR arrives, WLAST is already received, and the WDATA count is not equal to AWLEN |
| AXI_ERRM_WSTRB                      | AXI4/AXI3/Lite   | Write strobes must only be asserted for the correct byte lanes as determined from the: Start Address, Transfer Size, and Beat Number. |
| AXI_ERRM_WVALID_RESET               | AXI4/AXI3/Lite   | WVALID is Low for the first cycle after ARESETn goes High. |
| AXI_ERRM_WDATA_STABLE               | AXI4/AXI3/Lite   | Handshake Checks WDATA must remain stable when WVALID is asserted and WREADY Low. |
| AXI_ERRM_WLAST_STABLE               | AXI4/AXI3        | Handshake Checks WLAST must remain stable when WVALID is asserted and WREADY Low. |
| AXI_ERRM_WSTRB_STABLE               | AXI4/AXI3/Lite   | Handshake Checks WSTRB must remain stable when WVALID is asserted and WREADY Low. |
| AXI_ERRM_WVALID_STABLE              | AXI4/AXI3/Lite   | Handshake Checks Once WVALID is asserted, it must remain asserted until WREADY is High. |
| AXI_RECS_WREADY_MAX_WAIT            | AXI4/AXI3/Lite   | Recommended that WREADY is asserted within MAXWAITS cycles of WVALID being asserted. |
### Table 2-5: AXI Protocol Checks and Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI_ERRS_BRESP_WLAST</td>
<td>AXI4/AXI3</td>
<td>A slave must not take BVALID High until after the last write data is handshake is complete.</td>
</tr>
<tr>
<td>AXI_ERRS_BRESP_EXOKAY</td>
<td>AXI4/AXI3</td>
<td>An EXOKAY write response can only be given to an exclusive write access.</td>
</tr>
<tr>
<td>AXI_ERRS_BVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>BVALID is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>AXI_ERRS_BRESP_AW</td>
<td>AXI4/AXI3/Lite</td>
<td>A slave must not take BVALID High until after the write address is handshake is complete.</td>
</tr>
<tr>
<td>AXI_ERRS_BID_STABLE</td>
<td>AXI4/AXI3</td>
<td>Handshake Checks BID must remain stable when BVALID is asserted and BREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_BRESP_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Checks BRESP must remain stable when BVALID is asserted and BREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_BVALID_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Once BVALID is asserted, it must remain asserted until BREADY is High.</td>
</tr>
<tr>
<td>AXI_RECM_BREADY_MAX_WAIT</td>
<td>AXI4/AXI3/Lite</td>
<td>Recommended that BREADY is asserted within MAXWAITS cycles of BVALID being asserted.</td>
</tr>
<tr>
<td>AXI_ERRM_ARADDR_BOUNDARY</td>
<td>AXI4/AXI3</td>
<td>A read burst cannot cross a 4 KB boundary.</td>
</tr>
<tr>
<td>AXI_ERRM_ARADDR_WRAP_ALIGN</td>
<td>AXI4/AXI3</td>
<td>A read transaction with a burst type of WRAP must have an aligned address.</td>
</tr>
<tr>
<td>AXI_ERRM_ARBURST</td>
<td>AXI4/AXI3</td>
<td>A value of 2'b11 on ARBURST is not permitted when ARVALID is High.</td>
</tr>
<tr>
<td>AXI_ERRM_ARLEN_LOCK</td>
<td>AXI4/AXI3</td>
<td>Exclusive access transactions cannot have a length greater than 16 beats.</td>
</tr>
<tr>
<td>AXI_ERRM_ARCACHE</td>
<td>AXI4/AXI3</td>
<td>When ARVALID is High, if ARCACHE[1] is Low, then ARCACHE[3:2] must also be Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARLEN_FIXED</td>
<td>AXI4/AXI3</td>
<td>Transactions of burst type FIXED cannot have a length greater than 16 beats.</td>
</tr>
<tr>
<td>AXI_ERRM_ARLEN_WRAP</td>
<td>AXI4/AXI3</td>
<td>A read transaction with burst type of WRAP must have a length of 2, 4, 8, or 16.</td>
</tr>
<tr>
<td>AXI_ERRM_ARSIZE</td>
<td>AXI4/AXI3</td>
<td>The size of a read transfer must not exceed the width of the data interface.</td>
</tr>
<tr>
<td>AXI_ERRM_ARVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>ARVALID is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>AXI_ERRM_ARADDR_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>ARADDR must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARBURST_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARBURST must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARCACHE_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARCACHE must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARID_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARID must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
</tbody>
</table>
Chapter 2: Product Specification

Table 2-5: AXI Protocol Checks and Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI_ERRM_ARLEN_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARLEN must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARLOCK_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARLock must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARPROT_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>ARPROT must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARSIZE_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARSIZE must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARQOS_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARQOS must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARREGION_STABLE</td>
<td>AXI4</td>
<td>ARREGION must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARVALID_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Once ARVALID is asserted, it must remain asserted until ARREADY is High.</td>
</tr>
<tr>
<td>AXI_RECS_ARREADY_MAX_WAIT</td>
<td>AXI4/AXI3/Lite</td>
<td>Recommended that ARREADY is asserted within MAXWAITS cycles of ARVALID being asserted.</td>
</tr>
<tr>
<td>AXI_ERRS_RDATA_NUM</td>
<td>AXI4/AXI3</td>
<td>The number of read data items must match the corresponding ARLEN.</td>
</tr>
<tr>
<td>AXI_ERRS_RID</td>
<td>AXI4/AXI3</td>
<td>The read data must always follow the address that it relates to. Therefore, a slave can only give read data with an ID to match an outstanding read transaction.</td>
</tr>
<tr>
<td>AXI_ERRS_RRESP_EXOKAY</td>
<td>AXI4/AXI3</td>
<td>An EXOKAY write response can only be given to an exclusive read access.</td>
</tr>
<tr>
<td>AXI_ERRS_RVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>RVALID is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>AXI_ERRS_RDATA_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>RDATA must remain stable when RVALID is asserted and RREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_RID_STABLE</td>
<td>AXI4/AXI3</td>
<td>RID must remain stable when RVALID is asserted and RREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_RLAST_STABLE</td>
<td>AXI4/AXI3</td>
<td>RLAST must remain stable when RVALID is asserted and RREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_RRESP_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>RRESP must remain stable when RVALID is asserted and RREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_RVALID_STABLE</td>
<td>AXI4/AXI3/Lite</td>
<td>Once RVALID is asserted, it must remain asserted until RREADY is High.</td>
</tr>
<tr>
<td>AXI_RECM_RREADY_MAX_WAIT</td>
<td>AXI4/AXI3/Lite</td>
<td>Recommended that RREADY is asserted within MAXWAITS cycles of RVALID being asserted.</td>
</tr>
<tr>
<td>AXI_ERRM_EXCL_ALIGN</td>
<td>AXI4/AXI3</td>
<td>The address of an exclusive access is aligned to the total number of bytes in the transaction.</td>
</tr>
<tr>
<td>AXI_ERRM_EXCL_LEN</td>
<td>AXI4/AXI3</td>
<td>The number of bytes to be transferred in an exclusive access burst is a power of 2, that is, 1, 2, 4, 8, 16, 32, 64, or 128 bytes.</td>
</tr>
</tbody>
</table>
Table 2-5: AXI Protocol Checks and Descriptions (Cont’d)

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI_RECM_EXCL_MATCH</td>
<td>AXI4/AXI3</td>
<td>Recommended that the address, size, and length of an exclusive write with a given ID is the same as the address, size, and length of the preceding exclusive read with the same ID.</td>
</tr>
<tr>
<td>AXI_ERRM_EXCL_MAX</td>
<td>AXI4/AXI3</td>
<td>128 is the maximum number of bytes that can be transferred in an exclusive burst.</td>
</tr>
<tr>
<td>AXI_RECM_EXCL_PAIR</td>
<td>AXI4/AXI3</td>
<td>Recommended that every exclusive write has an earlier outstanding exclusive read with the same ID.</td>
</tr>
<tr>
<td>AXI_ERRM_AWUSER_STABLE</td>
<td>AXI4/AXI3</td>
<td>AWUSER must remain stable when AWVALID is asserted and AWREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_WUSER_STABLE</td>
<td>AXI4/AXI3</td>
<td>WUSER must remain stable when WVALID is asserted and WREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_BUSER_STABLE</td>
<td>AXI4/AXI3</td>
<td>BUSER must remain stable when BVALID is asserted and BREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRM_ARUSER_STABLE</td>
<td>AXI4/AXI3</td>
<td>ARUSER must remain stable when ARVALID is asserted and ARREADY Low.</td>
</tr>
<tr>
<td>AXI_ERRS_RUSER_STABLE</td>
<td>AXI4/AXI3</td>
<td>RUSER must remain stable when RVALID is asserted and RREADY Low.</td>
</tr>
<tr>
<td>AXI_AUXM_RCAM_OVERFLOW</td>
<td>AXI4/AXI3/Lite</td>
<td>Read CAM overflow, increase MAXRBURSTS parameter.</td>
</tr>
<tr>
<td>AXI_AUXM_RCAM_UNDERFLOW</td>
<td>AXI4/AXI3/Lite</td>
<td>Read CAM Underflow</td>
</tr>
<tr>
<td>AXI_AUXM_WCAM_OVERFLOW</td>
<td>AXI4/AXI3/Lite</td>
<td>Write CAM overflow, increase MAXWBURSTS parameter.</td>
</tr>
<tr>
<td>AXI_AUXM_WCAM_UNDERFLOW</td>
<td>AXI4/AXI3/Lite</td>
<td>Write CAM Underflow</td>
</tr>
<tr>
<td>AXI_AUXM_EXCL_OVERFLOW</td>
<td>AXI4/AXI3</td>
<td>Exclusive access monitor overflow, increase EXMON_WIDTH parameter.</td>
</tr>
<tr>
<td>AXI4LITE_ERRS_BRESP_EXOKAY</td>
<td>Lite</td>
<td>A slave must not give an EXOKAY response on an AXI4-Lite interface.</td>
</tr>
<tr>
<td>AXI4LITE_ERRS_RRESP_EXOKAY</td>
<td>Lite</td>
<td>A slave must not give an EXOKAY response on an AXI4-Lite interface.</td>
</tr>
<tr>
<td>AXI4LITE_AUXM_DATA_WIDTH</td>
<td>Lite</td>
<td>DATA_WIDTH parameter is 32 or 64.</td>
</tr>
</tbody>
</table>
Xilinx Configuration Checks and Descriptions

Table 2-6 lists the Xilinx configuration checks and descriptions.

<table>
<thead>
<tr>
<th>Name of Protocol Check</th>
<th>Protocol Support</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XILINX_AW_SUPPORTS_NARROW_BURST</td>
<td>AXI4/AXI3</td>
<td>When the connection does not support narrow transfers, the AW Master cannot issue a transfer with AWLEN &gt; 0 and AWSIZE less than the defined interface DATA_WIDTH.</td>
</tr>
<tr>
<td>XILINX_AR_SUPPORTS_NARROW_BURST</td>
<td>AXI4/AXI3</td>
<td>When the connection does not support narrow transfers, the AR Master cannot issue a transfer with ARLEN &gt; 0 and ARSIZE less than the defined interface DATA_WIDTH.</td>
</tr>
<tr>
<td>XILINX_AW_SUPPORTS_NARROW_CACHE</td>
<td>AXI4/AXI3</td>
<td>When the connection does not support narrow transfers, the AW Master cannot issue a transfer with AWLEN &gt; 0 and AWCACHE modifiable bit not asserted.</td>
</tr>
<tr>
<td>XILINX_AR_SUPPORTS_NARROW_CACHE</td>
<td>AXI4/AXI3</td>
<td>When the connection does not support narrow transfers, the AR Master cannot issue a transfer with ARLEN &gt; 0 and ARCACHE modifiable bit not asserted.</td>
</tr>
<tr>
<td>XILINX_AW_MAX_BURST</td>
<td>AXI4/AXI3</td>
<td>AW Master cannot issue AWLEN greater than the configured maximum burst length.</td>
</tr>
<tr>
<td>XILINX_AR_MAX_BURST</td>
<td>AXI4/AXI3</td>
<td>AR Master cannot issue ARLEN greater than the configured maximum burst length.</td>
</tr>
<tr>
<td>XILINX_AWVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>AWREADY is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>XILINX_WVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>WREADY is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>XILINX_BVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>BREADY is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>XILINX_ARVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>ARREADY is Low for the first cycle after ARESETn goes High.</td>
</tr>
<tr>
<td>XILINX_RVALID_RESET</td>
<td>AXI4/AXI3/Lite</td>
<td>RREADY is Low for the first cycle after ARESETn goes High.</td>
</tr>
</tbody>
</table>
Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

The AXI VIP core should be inserted into a system as shown in Figure 3-1 for AXI master VIP, Figure 3-2 for AXI slave VIP, and Figure 3-3 for AXI pass-through VIP.

![AXI Master VIP Example Topology](image)

Figure 3-1: AXI Master VIP Example Topology
Clocking

This section is not applicable for this IP core.

 Resets

The AXI VIP requires one active-Low reset, \texttt{aresetn}. The reset is synchronous to \texttt{aclk}. The reset is optional based on \texttt{HAS_ARESETN}. 

---

**Figure 3-2**: AXI Slave VIP Example Topology

**Figure 3-3**: AXI Pass-Through VIP Example Topology
Chapter 4

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- Vivado Design Suite User Guide: Designing with IP (UG896) [Ref 5]
- Vivado Design Suite User Guide: Getting Started (UG910) [Ref 6]
- Vivado Design Suite User Guide: Logic Simulation (UG900) [Ref 7]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator (UG994) [Ref 4] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the validate_bd_design command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the Vivado Design Suite User Guide: Designing with IP (UG896) [Ref 5] and the Vivado Design Suite User Guide: Getting Started (UG910) [Ref 6].

Note: Figures in this chapter are an illustration of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.
Figure 4-1 shows the AXI VIP Vivado IDE **Basic Settings** tab configuration screen.

For the runtime parameter descriptions, see Table 2-1.

- **Component Name** – The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and ".".
- **Interface Mode** – Control the mode of protocol to be configured as master, slave, or pass-through.
- **Protocol** – Select the specific AXI protocol.
- **Read or Write Mode** – Enable the AXI read or write mode.
- **Address Width** – Select the address width. Default at 32.
- **Data Width** – Select the data width. Default at 32.
- **ID Width** – Select the ID width. Default at 0.
- **User Signal Widths** – Select the width for each user signal. Default at 0.
Figure 4-2 shows the AXI VIP Vivado IDE **Advanced Settings** tab configuration screen. For more information on the user parameters, see **Table 2-1**.

**User Parameters**

For the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console), see **Table 2-1**.

**Output Generation**

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

The AXI VIP deliverables are organized in the directory `<project_name>/` `<project_name>.srcs/sources_1/ip/<component_name>` and are designed as the `<ip_source_dir>`. The relevant contents or directories are described in the following sections.
**Vivado Design Tools Project Files**

The Vivado design tools project files are located in the root of the `<ip_source_dir>`.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;component_name&gt;.xci</code></td>
<td>Vivado tools IP configuration options file. This file can be imported into any Vivado tools design and be used to generate all other IP source files.</td>
</tr>
<tr>
<td>`&lt;component_name&gt;.{veo</td>
<td>vho}`</td>
</tr>
</tbody>
</table>

**IP Sources**

The IP sources are held in the subdirectories of the `<ip_source_dir>`.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>hdl/*.sv</td>
<td>AXI VIP source files.</td>
</tr>
<tr>
<td>synth/&lt;component_name&gt;.sv</td>
<td>AXI VIP generated top-level file for synthesis. Optional, generated if synthesis target selected.</td>
</tr>
<tr>
<td>sim/&lt;component_name&gt;.sv</td>
<td>AXI VIP generated top-level file for simulation. Optional, generated if simulation target selected.</td>
</tr>
</tbody>
</table>

**AXI VIP in Vivado IP Integrator**

This section contains information about how to use the AXI VIP in a design and test bench environment. Figure 4-3 shows a possible design with the AXI VIPs.

![AXI VIP Design](image)
The AXI VIP is a SystemVerilog class library that is supported by most simulators. The AXI VIP uses similar naming and structures as the Universal Verification Methodology (UVM) for core design. The AXI VIP uses advanced verification techniques such as constrained randomization and transaction level modeling. It is coded in SystemVerilog. The AXI VIP is comprised of two parts. One is instanced like other traditional IP (modules in the static/physical world) and the second part is used in the dynamic world in your verification environment. The AXI VIP is an IP which has a static world connected to the dynamic world with a virtual interface. The virtual interface is the only mechanism that can bridge the dynamic world of objects with the static world of modules and interfaces.

**AXI Master VIP**

Figure 4-4 shows the AXI master VIP with its test bench. The test bench has three parts:

- User environment
- Master agent
- AXI master VIP

The user environment and master agent are in the dynamic world while the AXI master VIP is in the static world. The user environment communicates with the master agent and the master agent communicates with the AXI VIP interface though a virtual interface. The master agent has four class members:

- Master write driver
- Master read driver
- Monitor
- Virtual interface

For more information about the master agent, see Appendix C, AXI VIP Agent and Flow Methodology.
Figure 4-5 shows how a write transaction is constructed and sent to the AXI VIP interface. The user environment first declares a variable of the transaction type and then requests the Master Write Driver for a handle to a new transaction. During the create_transaction, the Master Write Driver sets properties on the transaction based on the physical configuration of the AXI VIP.

Using the handle, the user environment sets up the members of the transaction by either filling in using access methods or randomization. Once the transaction has been configured, the transaction is passed back to the Master Write Driver which sends it to the AXI VIP through a virtual interface and the AXI VIP interface pins start to wiggle. The read transaction flow follows a similar process, except using the Master Read Driver as the source of the handle to the transaction.
Chapter 4: Design Flow Steps

AXI Slave VIP

Figure 4-6 shows the AXI slave VIP with its test bench. The test bench has three parts:

- User environment
- Slave agent without a memory model
- AXI slave VIP

The user environment and slave agent are in the dynamic world, while the AXI slave VIP is in the static world. The user environment communicates with the slave agent and the slave agent communicates with the AXI VIP interface though a virtual interface. The slave agent without a memory model has four class members:

- Slave write driver
- Slave read driver
- Monitor
- Virtual interface

For more information about the slave agent, see Appendix C, AXI VIP Agent and Flow Methodology.

Figure 4-5: Write Transaction Flow
Figure 4-7 shows how a write response transaction is constructed and sent to the AXI VIP interface. The user environment first declares a variable of the transaction type which is used by the user environment to manage the transaction. The user environment then calls `get_wr_reactive` which blocks until a write transaction has been received by the Slave Write Driver.

The Slave Write Driver waits until it receives a write command, and then it returns the handle to the transaction. The user environment fills in the response portion of the transaction by either randomization or member functions of the transaction class. The Slave Write Driver then sends it to the AXI VIP interface through a virtual interface and the AXI VIP interface related pins start to wiggle. The read response transaction flow follows a similar process.
Simple SRAM Memory Model

The AXI slave VIP has a simple memory model (see Figure 4-8) and it is an associate array of SystemVerilog. The write transaction can write to the memory model and the read transaction can read data from the memory (also called front door access to differ from the backdoor access APIs). These two features are implemented in the AXI slave VIP and AXI pass-through VIP in runtime slave mode. At the same time, the memory model has backdoor APIs for you to access memory directly, which are backdoor_memory_write and backdoor_memory_read. The backdoor_memory_write writes data to memory and backdoor_memory_read reads data from memory. For usage of memory model APIs, see the Xilinx AXI API Documentation [Ref 11].

**IMPORTANT:** This memory has no support for built-in system tasks such as readmemh. You can use the backdoor_memory_write to write all of the file information into the memory. Reset has no effect on memory content.
AXI Slave Simple Memory VIP

As shown in Figure 4-6, the AXI slave simple memory VIP is similar to the AXI slave VIP. The only difference is that the AXI slave simple memory VIP has a simple memory model. The user environment does not need to fill in read/write reactive transaction information. Its test bench has three parts:

- User environment
- Slave agent with a memory model
- AXI slave VIP

The user environment and slave agent are in the dynamic world, while the AXI slave VIP is in the static world. The user environment communicates with the slave agent and the slave agent communicates with the AXI VIP interface though a virtual interface. The slave agent without a memory model has five class members:

- Slave write driver
- Slave read driver
- Monitor
- Virtual interface
- Memory model

For more information about the slave agent with memory model, see Appendix C, AXI VIP Agent and Flow Methodology.

Different from the AXI slave VIP, the AXI slave simple memory VIP does not need the user environment to create and fill in write/read reactive transaction since all these are being done in the slave memory agent. Refer to the multiple simsets for its usage.
Multiple AXI VIP

Figure 4-9 shows multiple AXI VIPs in one design and its test bench. Similar to the single AXI VIP, it has dynamic and static worlds that are bridged through a virtual interface.

Finding the AXI VIP Hierarchy Path in IP Integrator

As mentioned earlier, the user environment has to declare the agent for the AXI VIP. Also, the AXI VIP interface has to be passed to the agent when the user environment constructs it to set it as a virtual interface. The following guidelines describe how to find the hierarchy path of the AXI VIP in the IP integrator.
1. Right-click **bd design** and select **Generate Output Products** (Figure 4-10).

   ![Figure 4-10: Generate Output Products](image)

   **Figure 4-10:** Generate Output Products

2. After the **General Output Products** is delivered, right-click **bd design** again and select **Create HDL Wrapper**.
3. Figure 4-11 shows the complete hierarchy of the instances after the wrapper generates.

4. Use the generated wrapper as a DUT module in the test bench and the hierarchy path of these three AXI VIPs are DUT.design_1.axi_vip_0.inst, DUT.design_1.axi_vip_1.inst, and DUT.design_1.axi_vip_2.inst.

5. The best method to identify the VIP instance in the hierarchy is after the connection of all the IPs and the validation check. Click the Simulation Settings, set up the tool, and then click Run Simulation. Figure 4-12 shows the Mentor Graphics Questa Advanced Simulator results. After the hierarchy is identified, it is used in the SystemVerilog test bench to drive the VIP APIs.
Chapter 4: Design Flow Steps

After the AXI VIP is instantiated in the IP integrator design and its hierarchy path found, the next step is using the AXI VIP in the test bench. See Chapter 5, Example Design.

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.
Clock Placement
This section is not applicable for this IP core.

Banking
This section is not applicable for this IP core.

Transceiver Placement
This section is not applicable for this IP core.

I/O Standard and Placement
This section is not applicable for this IP core.

Simulation
For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the Vivado Design Suite User Guide: Logic Simulation (UG900) [Ref 7].

IMPORTANT: For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.

Synthesis and Implementation
The AXI VIP core is a verification IP set to synthesize as wires. The axi_protocol_checker contained in the AXI VIP is for simulation only and does not synthesize. There is no implementation for the AXI VIP.
Example Design

This chapter contains information about the example design provided in the Vivado® Design Suite.

**IMPORTANT:** The example design of this IP is customized to the IP configuration. The intent of this example design is to demonstrate how to use the AXI VIP. The AXI VIP can only act as a protocol checker when contained within a VHDL hierarchy. Do not import two different revision/versions of the axi_vip packages. This will cause elaboration failures. All AXI VIP and parents to the AXI VIP must be upgraded to the latest version.

Overview

*Figure 5-1* shows the AXI VIP example design.

*Figure 5-1: AXI VIP Example Design*

This section describes the example tests used to demonstrate the abilities of the AXI VIP core. Example tests are delivered in SystemVerilog. The example design is available in the AXI VIP installation area in the Tcl Console folder in an unencrypted format.

When the core example design is open, the example files are delivered in a standard path test bench and bd design are under directory imports. The packages are under the directory example.srcs/sources_1/bd/ex_sim/ipshared.

The example design consists of three components:

- AXI VIP in master mode
- AXI VIP in pass-through mode
• **AXI VIP in slave mode**

The AXI master VIP creates write/read transactions and sends them to the AXI pass-through VIP. The AXI pass-through VIP receives transactions from the AXI master VIP and sends them to the AXI slave VIP. The AXI slave VIP receives transactions from the AXI pass-through VIP, generates write/read responses, and sends the responses back to the AXI pass-through VIP and then back to AXI master VIP.

Monitors for the AXI VIP (master, pass-through, and slave) are always on and collect all of the information from the interfaces. The monitors convert the interface information back to the transaction level and sends it to the scoreboard. Two scoreboards are built in the test bench which performs self-checking for the AXI master VIP against the AXI pass-through VIP and the AXI slave VIP against the AXI pass-through VIP.

The AXI VIP core is not fully autonomous. If tests are written using the APIs, there are different methods from the user environment to set up the transaction. It is possible that the AXI protocol can be accidentally violated. The member functions of the transaction class performs quick protocol and configuration checks. Xilinx recommends the use of transaction randomization and constraints for generating generic transactions. Furthermore, it is possible to further modify a transaction after it was originally generated through a randomization.

When the AXI VIP is configured in pass-through mode, it has the ability to be a passive monitor or it can take control of the interface. The AXI VIP can change to be a master driving a downstream slave or a slave responding to the master. This process can be done during a simulation at any time and then changed back to pass-through mode according to your preference.

When it is switched to runtime master mode, it behaves exactly as an AXI master VIP. When it is switched to runtime slave mode, it behaves exactly as an AXI slave VIP.

**IMPORTANT:** Make sure all transactions have completed before switching modes. Examples of how to wait for the transactions finishing can be found in the example design.
Test Bench

This chapter contains information about the test bench for the example design provided in the Vivado® Design Suite.

To open the example design either from the Vivado IP catalog or Vivado IP integrator design, follow these steps:

1. Open the example from the Vivado IP catalog.
2. Open a new project and click IP Catalog.
3. Search for AXI Verification IP. Double-click it, configure the IP, and generate the IP.
4. Right-click the IP and choose Open IP Example Design. If you have the AXI VIP as one component in the IP integrator design, right-click AXI VIP and click Open IP Example Design…

In both scenarios, a new project with the example design is created. The example design has the master, pass-through, and slave VIP connected directly to each other as shown in Figure 5-1. The configuration of the example design matches the original VIP configuration.

Multiple Simulation Sets

The Vivado Design Suite has a feature that each design can have multiple simulation sets according to your settings (AR: 64111). Especially, multiple test benches can be constructed for the same design. For example, one test bench provides stimulus for behavioral simulation of a complicated design and a different test bench provides stimulus for timing simulation of the implemented design.

The AXI VIP example design in the 2017.1 release has simulation sets listed in Table 6-1. The sim_all_config is a comprehensive simulation set. See the AXI VIP Example Test Bench and Test section for a list of features. It shows different examples of how to use the AXI VIP in a complex method.

For ease of use, 10 additional simulation sets with simple codes are also included in the example design. Naming of these 10 simulation sets:

```
sim_<basic or adv>_mst_<mode>_pt_<mode>_slv_<mode>
```
Where mode = active, mem, passive, or combo.

For example, sim_basic_mst_passive__pt_mst__slv_comb means this simulation set is performing a basic feature of the AXI VIP when the AXI master VIP is in passive mode. The AXI pass-through VIP is in the runtime master mode and communicates to the AXI slave VIP which does not include the memory model.

For the 10 simulation set test benches, it includes three files which are generic_tb.sv, master stimulus, and slave stimulus.

- The generic_tb performs a simple self-checking of the master side (can be AXI master VIP or AXI pass-through VIP in runtime master mode) against the slave side (can be AXI slave VIP or AXI pass-through VIP in runtime slave mode).
- Master stimulus is generated by the AXI master VIP or AXI pass-through VIP in the runtime master mode.
- Slave stimulus is generated by the AXI slave VIP or AXI pass-through VIP in the runtime slave mode with/without the memory model. The slave mem stimulus file is included and you can access the file to check the AXI slave VIP with the memory model.

The difference between basic and advanced simulation sets is that the basic simulation set shows the code snippets which are needed in the test bench to use the AXI VIP. Advanced simulation set adds more APIs such as user-configured READY signals which are optional. For more information, see the example design in the Vivado Design Suite and for usage of APIs, see the Xilinx AXI VIP API Documentation [Ref 11].

The following shows how to generate a transaction for each mode:

1. To generate a transaction for the AXI master VIP, see the mst_stimulus.sv from any of the 10 simulation sets in Table 6-1.
2. To generate a transaction response for a basic AXI slave VIP, see the slv_basic_stimulus.sv from any of the 10 simulation sets in Table 6-1. For memory model requirements, see the mem_basic_stimulus.sv.
3. To generate a transaction response for an advanced AXI slave VIP, see the slv_stimulus.sv from any of the 10 simulation sets in Table 6-1. For memory model requirements, see the mem_stimulus.sv.
4. To generate a transaction for the AXI pass-through VIP, see the passthrough_mst_stimulus.sv from any of the simulation sets in Table 6-1.
5. To generate a transaction response for a basic AXI pass-through VIP, see the passthrough_slv_basic_stimulus.sv from any of the simulation sets in Table 6-1. For memory model requirements, see the passthrough_mem_basic_stimulus.sv.
6. To generate a transaction response for an advanced AXI pass-through VIP, see the passthrough_slv_stimulus.sv from any of the simulation sets in Table 6-1. For memory model requirements, see the passthrough_mem_stimulus.sv.
7. When you open the AXI VIP example design under the **Sources** window, it shows 11 simulation sets. You can choose any simulation sets and run simulation or view the source codes of each test bench.

### Table 6-1: Simulation Sets for AXI VIP

<table>
<thead>
<tr>
<th>Simulation Set Name</th>
<th>Files Included</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sim_basic_mst_passive_pt_mst_slv_comb</td>
<td>passthrough_mst_stimulus.sv, slv_basic_stimulus.sv, generic_tb.sv</td>
<td>Basic feature of AXI VIP when AXI master VIP is in passive mode. AXI pass-through VIP is in runtime master mode and talks to AXI slave VIP which does not include memory model.</td>
</tr>
<tr>
<td>sim_basic_mst_active_pt_slv_slv_passive</td>
<td>mst_stimulus.sv, passthrough_slv_basic_stimulus.sv, generic_tb.sv</td>
<td>Basic feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in runtime slave mode without memory model. AXI slave VIP is in passive mode.</td>
</tr>
<tr>
<td>sim_basic_mst_active_pt_mem_slv_passive</td>
<td>mst_stimulus.sv, passthrough_mem_basic_stimulus.sv, generic_tb.sv</td>
<td>Basic feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in runtime slave mode with memory model. AXI slave VIP is in passive mode.</td>
</tr>
<tr>
<td>sim_basic_mst_active_pt_passive_slv_mem</td>
<td>mst_stimulus.sv, mem_basic_stimulus.sv, generic_tb.sv</td>
<td>Basic feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in passive mode. AXI slave VIP is in active mode with memory model.</td>
</tr>
<tr>
<td>sim_basic_mst_active_pt_passive_slv_comb</td>
<td>mst_stimulus.sv, slv_basic_stimulus.sv, generic_tb.sv</td>
<td>Basic feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in passive mode. AXI slave VIP is in active mode without memory model.</td>
</tr>
<tr>
<td>sim_adv_mst_passive_pt_mst_slv_comb</td>
<td>passthrough_mst_stimulus.sv, slv_stimulus.sv, generic_tb.sv</td>
<td>Advanced feature of AXI VIP when AXI master VIP is in passive mode. AXI pass-through VIP is in runtime master mode and talks to AXI slave VIP which does not include memory model.</td>
</tr>
<tr>
<td>sim_adv_mst_active_pt_slv_slv_passive</td>
<td>passthrough_slv_stimulus.sv, generic_tb.sv</td>
<td>Advanced feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in runtime slave mode without memory model. AXI slave VIP is in passive mode.</td>
</tr>
</tbody>
</table>
Table 6-1: Simulation Sets for AXI VIP (Cont’d)

<table>
<thead>
<tr>
<th>Simulation Set Name</th>
<th>Files Included</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sim_adv_mst_active_pt_mem_slv_passive</td>
<td>mst_stimulus.sv</td>
<td>Advanced feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in runtime slave mode with memory model. AXI slave VIP in passive mode.</td>
</tr>
<tr>
<td></td>
<td>passthrough_mem_stimulus.sv</td>
<td></td>
</tr>
<tr>
<td></td>
<td>generic_tb.sv</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sim_adv_mst_active_pt_passive_slv_mem</td>
<td>mst_stimulus.sv</td>
<td>Advanced feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in passive mode. AXI slave VIP in active mode with memory model.</td>
</tr>
<tr>
<td></td>
<td>mem_stimulus.sv</td>
<td></td>
</tr>
<tr>
<td></td>
<td>generic_tb.sv</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>sim_adv_mst_active_pt_passive_slv_comb</td>
<td>mst_stimulus.sv</td>
<td>Advanced feature of AXI VIP when AXI master VIP is in active mode. AXI pass-through VIP is in passive mode. AXI slave VIP in active mode without memory model.</td>
</tr>
<tr>
<td></td>
<td>slv_stimulus.sv</td>
<td></td>
</tr>
<tr>
<td></td>
<td>generic_tb.sv</td>
<td></td>
</tr>
<tr>
<td>sim_all_config</td>
<td></td>
<td>Shows all of the configured examples.</td>
</tr>
</tbody>
</table>
Figure 6-1 to Figure 6-3 show the basic, advanced, and all configured simulation sets for AXI VIP.

**Figure 6-1: Basic Simulation Sets**

- **sim_basic_mst_passive_pt_mst_slv_comb**
  - Testbench
  - Master VIP (Passive)
  - Pass-Through VIP (Runtime Master)
  - Slave VIP (Without Memory Model)
  - passthrough_mst_stimulus.sv
  - slv_basic_stimulus.sv

- **sim_basic_mst_active_pt_slv_slv Passive**
  - Testbench
  - Master VIP
  - Pass-Through VIP (Runtime Slave without Memory Model)
  - Slave VIP (Passive)
  - mst_stimulus.sv
  - passthrough_slv_basic_stimulus.sv

- **sim_basic_mst_active_pt_mem_slv Passive**
  - Testbench
  - Master VIP
  - Pass-Through VIP (Runtime Slave with Memory Model)
  - Slave VIP (Passive)
  - mst_stimulus.sv
  - passthrough_mem_basic_stimulus.sv

- **sim_basic_mst_active_pt_passive_slv_comb**
  - Testbench
  - Master VIP
  - Pass-Through VIP (Passive)
  - Slave VIP (Without Memory Model)
  - mst_stimulus.sv
  - mem_basic_stimulus.sv
  - slv_basic_stimulus.sv
Figure 6-2: Advanced Simulation Sets
Chapter 6: Test Bench

Figure 6-3: All Configured Simulation Set

Figure 6-4 shows a simulation configuration example in Vivado IDE.

Figure 6-4: Simulation Configuration in Vivado Design Suite

AXI VIP Example Test Bench and Test

The example design is generated to match the VIP’s configuration, so is the test bench. Eleven different test benches have been implemented for this VIP and each simulation set fits different needs described in the Multiple Simulation Sets section. For more information, see Chapter 5, Example Design.
Useful Coding Guidelines and Examples

Must Haves in the Test Bench

While coding test bench for the AXI VIP, the following requirements must be met. Otherwise, the AXI VIP does not work. These are the requirements for all VIPs.

1. Create module test bench as all other standard SystemVerilog test benches.
   ```systemverilog
   module testbench();
   ...
   endmodule
   ```

2. Import two required packages: `axi_vip_v1_0_1_pkg` and `<component_name>_pkg` as shown in Figure 6-5. The `<component_name>_pkg` includes agent classes and its subclasses for AXI VIP. For each VIP instance, it has a component package which is automatically generated when the outputs are created. This component package includes a `typedef` class of a parameterized agent. Xilinx recommends importing this package because reconfiguration of the VIP has no impact of the test bench.

   ![Figure 6-5: Component Name Location](https://www.xilinx.com/support/answers/98254.html)

In order to use the virtual part of this IP you will need to add the following lines into your testbench file:

- `import axi_vip_v1_0_1_pkg;`
- `import <component_name>_pkg;`

The API for the virtual part of this IP can be found: [https://www.xilinx.com/support/answers/98254.html](https://www.xilinx.com/support/answers/98254.html)
3. Declare agents. One agent for one AXI VIP has to be declared. Depending on the AXI VIP interface mode, different typedef class should be called for declaration of the agent.

4. Create a new for the agent and pass the hierarchy path of IF correctly into the new function. Before the agent is set to new, run the simulation with an empty test bench to find the hierarchy path of the AXI VIP instance. A message like this shows up and then puts the path into a new function (see Figure 4-12).

```c
agent = new("my VIP agent", <hierarchy_path>.IF);
```

### Start Agent

For the VIP to start running, start agent has to be called. The following shows how the master, slave, and pass-through VIPs start to run.

**AXI Master VIP**

Start agent:

```c
mst_agent.start_master();
```

Then, generate the transaction. For more information about how to generate transaction, see the Vivado example design simset and look for `mst_stimulus.sv`.

**AXI Slave VIP**

Start agent:

```c
slv_agent.start_slave();
```

If `<component_name>_slv_t` is used, the user environment has to fill a write response if READ_WRITE_MODE is not READ_ONLY, and read response if READ_WRITE_MODE is not WRITE_ONLY. For more information, see the Vivado example design simset and look for `slv_basic_stimulus.sv`/`slv_stimulus.sv`.

If `<component_name>_slv_mem_t` is used, write response and read response are handled in the agent. The user environment does not need to do anything here. For more information, see the Vivado example design simset and look for `mem_basic_stimulus.sv`/`mem_stimulus.sv`.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;component_name&gt;_mst_t</code></td>
<td>Master VIP</td>
</tr>
<tr>
<td><code>&lt;component_name&gt;_slv_t</code></td>
<td>Slave VIP without memory model</td>
</tr>
<tr>
<td><code>&lt;component_name&gt;_slv_mem_t</code></td>
<td>Slave VIP with memory model</td>
</tr>
<tr>
<td><code>&lt;component_name&gt;_passthrough_t</code></td>
<td>Pass-through VIP without memory model</td>
</tr>
<tr>
<td><code>&lt;component_name&gt;_passthrough_mem_t</code></td>
<td>Pass-through VIP with memory model</td>
</tr>
</tbody>
</table>
**AXI Pass-Through VIP**

**Runtime Slave Mode**

Switch AXI pass-through VIP into the runtime slave mode. The `<hierarchy_path>` can be found in step 4 and then start the slave agent.

```c
<hierarchy_path>.set_slave_mode();
passthrough_agent.start_slave();
```

If `<component_name>_passthrough_slv_t` is used, the write response/read response have to be filled in through the user environment.

For more information, see the Vivado example design simset and look for `passthrough_slv_basic_stimulus.sv/passthrough_slv_stimulus.sv`.

If `<component_name>_passthrough_mem_t` is used, the user environment does not need to do anything. For more information, see the Vivado example design simset and look for `passthrough_mem_basic_stimulus.sv/passthrough_mem_stimulus.sv`.

**Runtime Master Mode**

Switch AXI pass-through VIP into the runtime master mode. The `<hierarchy_path>` can be found in step 4 and then start the master agent.

```c
<hierarchy_path>.set_master_mode();
passthrough_agent.start_master();
```

Create transaction. For more information, see the Vivado example design simset and look for `passthrough_mst_stimulus.sv`.

**Runtime Pass-Through Mode**

Default is in pass-through mode. If you want to switch back to the pass-through mode from the master/slave mode, you have to call API `set_passthrough_mode`. The `<hierarchy_path>` can be found in step 4 and then start the pass-through agent.

```c
<hierarchy_path>.set_passthrough_mode();
```

The `start_monitor` is optional.

The following shows a list of related parameters and type definitions used in the AXI VIP:

```c
parameter XIL_AXI_MAX_DATA_WIDTH = 1024;
parameter XIL_AXI_USER_BEAT_WIDTH = 1024;
parameter XIL_AXI_USER_ELEMENT_WIDTH = 32;
parameter XIL_AXI_VERBOSITY_NONE = 0;
parameter XIL_AXI_VERBOSITY_FULL = 400;
typedef integer               xil_axi_int;
typedef longint              xil_axi_long;
typedef integer unsigned    xil_axi_uint;
typedef longint unsigned    xil_axi_ulong;
```
typedef logic [7:0] xil_axi_payload_byte;
typedef logic xil_axi_strb_byte;
typedef logic [XIL_AXI_USER_BEAT_WIDTH-1:0] xil_axi_user_beat;
typedef logic [XIL_AXI_MAX_DATA_WIDTH-1:0] xil_axi_data_beat;
typedef logic [XIL_AXI_MAX_DATA_WIDTH/8-1:0] xil_axi_strb_beat;
typedef integer unsigned xil_axi_user_element;

IMPORTANT: You have to call stop_master when pass-through VIP switches from the runtime master mode to the other mode. Similarly, you have to call stop_slave when pass-through VIP switches from runtime slave mode to the other mode. For more information, see the example design in Vivado. The start_master and start_slave of the pass-through VIP agent cannot be called at the same time. When the pass-through VIP is switching from the runtime master mode to the runtime slave mode, the stop_master has to be called. Vice versa, stop_slave has to be called.

Optional Test Bench Controls

Create Ready Signal

The following shows how to create a specified rready signal. Use the AXI master VIP or AXI pass-through VIP in runtime master mode. Use the create API to create rready, set the low and high pattern, and then send it to the VIP interface. For other rready signals, if nothing is done, the AXI VIP itself generates this rready signal.

// master agent create rready
rready_gen = mst_agent.rd_driver.create_ready("rready");
// set the feature of rready signal. If nothing is done here, default pattern of ready will be generated
rready_gen.set_ready_policy(XIL_AXI_READY_GEN_OSC);
rready_gen.set_low(1);
rready_gen.set_high(2);
// send the rready to VIP interface
mst_agent.rd_driver.send_rready(rready_gen);

Other Optional Controls

Using APIs to set agents’ tag and verbosity for debug purpose.

//set tag for agents for easy debug
mst_agent.set_agent_tag("Master VIP");
//verbosity level which specifies how much debug information to produce
// 0       - No information will be shown.
// 400     - All information will be shown.
mst_agent.set_verbosity(mst_agent_verbosity);
Transaction Examples

There are different methods of configuring the transaction after it is created. In the example design, simset_all_config, three methods are shown for write and read transactions. Method 1 is to fully randomize the transaction after it is being created. Method 2 is similar to AXI BFM WRITE_BURST and READ_BURST for migration purpose. Method 3 shows how to use the APIs to set the transaction.

Write Transaction Methods

Method 1 for Write Transaction

For a write transaction, follow these steps:

1. Create the transaction from the write driver of the master agent.
2. Randomize the transaction.
3. Send the transaction from the master agent write driver.

**IMPORTANT:** The API sent here is non-blocking. By default, the driver does not return transaction information. If you want to receive transaction information back, the API, set_driver_return_item, can be called and the related driver_return_item_policy can be called here.

```cpp
wr_transaction = mst_agent.wr_driver.create_transaction("write transaction");
WR_TRANSACTION_FAIL_1b: assert(wr_transaction.randomize());
mst_agent.wr_driver.send(wr_transaction);
```

Method 2 for Write Transaction

**Note:** This is a blocking write and it blocks until the BRESP is returned.

```cpp
//The following shows the AXI4_WRITE_BURST. For other options. see the Xilinx AXI VIP API Documentation [Ref 11].
mst_agent.AXI4_WRITE_BURST(
    mtestID,
    mtestADDR,
    mtestBurstLength,
    mtestDataSize,
    mtestBurstType,
    mtestLOCK,
    mtestCacheType,
    mtestProtectionType,
    mtestRegion,
    mtestQOS,
    mtestAWUSER,
    mtestWData,
    mtestWUSER,
    mtestBresp
);
```
Chapter 6: Test Bench

Method 3 for Write Transaction

This method shows how to use the APIs to set the command and data of the write transaction.

```plaintext
wr_transaction = mst_agent.wr_driver.create_transaction("write transaction");
wr_transaction.set_write_cmd(mtestADDR, mtestBurstType, mtestID,
                             mtestBurstLength, mtestDataSize);
wr_transaction.set_data_block(mtestWData);
for(int beat=0; beat<wr_transaction.get_len()+1; beat++) begin
    wr_transaction.set_data_beat(beat, dbeat);
end
mst_agent.wr_driver.send(wr_transaction);
```

Read Transaction Methods

Method 1 for Read Transaction

For a read transaction, follow these steps:

1. Create the transaction from the read driver of the master agent.
2. Randomize the transaction.
3. Send the transaction from the master agent read driver.

**IMPORTANT:** The API sent here is non-blocking. If you want to receive transaction information back, the driver return item policy needs to be set here.

```plaintext
rd_transaction = mst_agent.rd_driver.create_transaction("read transaction");
RD_TRANSACTION_FAIL_1a:assert(rd_transaction.randomize());
mst_agent.rd_driver.send(rd_transaction);
```

Method 2 for Read Transaction

**Note:** This is a blocking read and it blocks until the BRESP is returned.

```plaintext
// The following shows the AXI4_READ_BURST. For other options, see the Xilinx AXI VIP API Documentation [Ref 11].
mst_agent.AXI4_READ_BURST {
    mtestID,
    mtestADDR,
    mtestBurstLength,
    mtestDataSize,
    mtestBurstType,
    mtestLOCK,
    mtestCacheType,
    mtestProtectionType,
    mtestRegion,
    mtestQOS,
    mtestARUSER,
    mtestRData,
    mtestRresp,
    mtestRUSER
};
```
Method 3 for Read Transaction

This method shows how to use the APIs to set the command and data of the read transaction.

```java
rd_transaction = mst_agent.rd_driver.create_transaction("read transaction");
rd_transaction.set_read_cmd(mtestADDR, mtestBurstType, mtestID,
                           mtestBurstLength, mtestDataSize);
mst_agent.rd_driver.send(rd_transaction);
```
Appendix A

Upgrading

This appendix is not applicable for the first release of the core.
Appendix B

Migrating from BFM to VIP

This appendix contains information about migrating a Vivado® design with AXI BFM to AXI VIP.

1. In Vivado IP integrator BD design, replace BFM with AXI VIP and configure the AXI VIP. If the old BFM is AXI4 in slave mode, for example, set up the AXI VIP protocol to AXI4 and the interface mode to slave.

2. In the test bench, remove all BFM related tasks and add the following codes:
   - Import two packages, see Chapter 6, Test Bench on how to obtain `<component_name>_pkg`:
     ```
     import <component_name>_pkg::*
     import axi_vip_v1_0_0_pkg::*;
     ```
   - Declare agent, see Chapter 6, Test Bench for requirements. Because it is for migration purpose, no pass-through agent is declared since BFM did not support pass-through mode.
   - Construct the agent.
     - For example, AXI VIP in master mode:
       ```
       mst_agent = new("master vip agent",<hierarchy path to AXI VIP instance> inst.IF);
       ```
       See Chapter 4, Design Flow Steps to find the hierarchy path.
   - Start agent:
     - If AXI VIP is in master mode:
       ```
       mst_agent.start_master();
       ```
   - Replace the existing BFM WRITE/READ_BURST with the VIP WRITE/READ_BURST.
     - If AXI VIP is AXI4:
       ```
       AXI4_WRITE/READ_BURST
       ```
     - If AXI VIP is AXI3:
       ```
       AXI3_WRITE/READ_BURST
       ```
     - If AXI VIP is AXI4LITE:
       ```
       AXI4LITE_WRITE/READ_BURST
       ```
Appendix C

AXI VIP Agent and Flow Methodology

This appendix contains information about the AXI VIP agents and flow methodologies. The AXI VIP has three agents:

- AXI Master Agent
- AXI Slave Agent
- AXI Pass-Through Agent

AXI Master Agent

When instantiating an AXI master VIP, a master agent has to be declared and constructed. Class `axi_mst_agent` contains other components that consist of the entire master Verification IP. These are the read driver, write driver, and monitor.

![AXI Master VIP Agent](image)

*Figure C-1: AXI Master VIP Agent*
Appendix C: AXI VIP Agent and Flow Methodology

AXI Master Read Driver

- Receives READ transactions from the user environment and drives the AR channel.
- Triggers an event when the AR Command is accepted.
- Receives READY transactions from the user environment and drives the RREADY signal of the R channel.
- By default, transaction does not return until you set the driver return item policy. For usage, see the Xilinx AXI VIP API Documentation [Ref 11].

AXI Master Write Driver

- Receives WRITE transactions from the user environment and drives the AW and W channels.
- Triggers an event when the AW Command is accepted.
- Triggers an event when the WLAST is accepted.
- Receives READY transactions from the user environment and drives the BREADY signal of the B channel.
- By default, transaction does not return until you set the driver return item policy. For usage, see the Xilinx AXI VIP API Documentation [Ref 11].

AXI Monitor

- Monitors all five AXI channels: AW, AR, R, W, and B.
- It has seven analysis ports which you can select to use. By default, only item_collect_port is ON, all other ports are OFF. You can use the API, set_enabled, in each analysis port to switch ON the port. They include:

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>item_collect_port</td>
<td>Collects both write/read transaction information and converts to axi_monitor_transaction.</td>
</tr>
<tr>
<td>axi_cmd_port</td>
<td>Collects both write/read channel information and converts to xil_axi_cmd_beat.</td>
</tr>
<tr>
<td>axi_rd_cmd_port</td>
<td>Collects read address channel information and converts to xil_axi_cmd_beat.</td>
</tr>
<tr>
<td>axi_wr_cmd_port</td>
<td>Collects write address channel information and converts to xil_axi_cmd_beat.</td>
</tr>
<tr>
<td>axi_bresp_port</td>
<td>Collects write response channel information and converts to xil_axi_resp_beat.</td>
</tr>
<tr>
<td>axi_wr_beat_port</td>
<td>Collects write data channel information and converts to xil_axi_wr_beat.</td>
</tr>
<tr>
<td>axi_rd_beat_port</td>
<td>Collects read data channel information and converts to xil_axi_read_beat.</td>
</tr>
</tbody>
</table>

- Collects and reorders R Channel beats and returns a completed transaction when the RLAST is accepted.
Appendix C: AXI VIP Agent and Flow Methodology

- Collects and reorders B Channel response and returns a completed transaction when the B channel is accepted.
- Transaction based protocol checking.

**Transaction Return Item Policy Implementation**

*Table C-1* shows the transaction return descriptions.

\[
\text{last\_handshake} = *\text{LAST} + *\text{VALID} + *\text{READY}
\]

\[
\text{cmd\_handshake} = *\text{VALID} + *\text{READY}
\]

\[
\text{bresp\_handshake} = \text{BVALID} + \text{BREADY}
\]

*Table C-1: Transaction Return Descriptions*

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO_RETURN</td>
<td>Item is not returned by the driver.</td>
</tr>
<tr>
<td>CMD_RETURN</td>
<td>Item is returned when at cmd_handshake.</td>
</tr>
<tr>
<td>PAYLOAD_RETURN</td>
<td>For writes, the item is returned at bresp_handshake.</td>
</tr>
<tr>
<td></td>
<td>For reads, the item is returned at last_handshake</td>
</tr>
<tr>
<td>CMD_PAYLOAD_RETURN</td>
<td>Item is returned twice.</td>
</tr>
<tr>
<td></td>
<td>At cmd_handshake.</td>
</tr>
<tr>
<td></td>
<td>At:</td>
</tr>
<tr>
<td></td>
<td>For writes: bresp_handshake.</td>
</tr>
<tr>
<td></td>
<td>For reads: last_handshake.</td>
</tr>
<tr>
<td>CMD_WL_RETURN</td>
<td>Item is returned twice:</td>
</tr>
<tr>
<td></td>
<td>At cmd_handshake.</td>
</tr>
<tr>
<td></td>
<td>At last_handshake.</td>
</tr>
<tr>
<td></td>
<td><em>Note:</em> This return type is not valid for read transactions.</td>
</tr>
<tr>
<td>CMD_WL_LAST_PAYLOAD_RETURN</td>
<td>Item is returned three times:</td>
</tr>
<tr>
<td></td>
<td>At cmd_handshake.</td>
</tr>
<tr>
<td></td>
<td>At last_handshake.</td>
</tr>
<tr>
<td></td>
<td>At bresp_handshake.</td>
</tr>
<tr>
<td></td>
<td><em>Note:</em> This return type is not valid for read transactions.</td>
</tr>
<tr>
<td>WLAST_PAYLOAD_RETURN</td>
<td>Item is returned twice:</td>
</tr>
<tr>
<td></td>
<td>At last_handshake.</td>
</tr>
<tr>
<td></td>
<td>At bresp_handshake.</td>
</tr>
<tr>
<td></td>
<td><em>Note:</em> This return type is not valid for read transactions.</td>
</tr>
<tr>
<td>WLAST_RETURN</td>
<td>Item is returned at last_handshake.</td>
</tr>
<tr>
<td></td>
<td><em>Note:</em> This return type is not valid for read transactions.</td>
</tr>
</tbody>
</table>
Items Returned During Reset

When a reset is applied, transactions that are in flight are returned to the user environment (sequencer). There are cases where the same transaction exist in multiple queues, so in those cases the process modifies the transaction and changes it to NO_RETURN. Therefore, the user environment does not return the item multiple times.
Figure C-2: Write Command and Data Flow
Write Transaction Flow

The AXI master write transaction flows through the write agent in the following steps:

1. Driver asks for the next transaction through a `get_next_item`. This is a blocking get.

2. The user environment creates a single transaction. The transaction contains the following:
   - **Command Information** – AWADDR, AWLEN, AWSIZE, AWID, etc.
   - **Payload** – WDATA byte array and WSTRB array
   - **Master Controlled Timing** – Inter-beat timing and address delay

3. The user environment pushes the transaction to the driver.

4. The driver pops the transaction from the REQUEST port and places it on a queue to be processed and driven onto the interface. If the transaction depth > 1, the driver continues to accept transactions until this value has been met.

5. When the interface receives the BRESP from the slave, the master driver returns a copy of the transaction to the user environment if the transaction driver return item policy is set to one of the following values:
   - XIL_AXI_CMD_RETURN
   - XIL_AXI_CMD_WLAST_RETURN
   - XIL_AXI_WLAST_RETURN
   - XIL_AXI_PAYLOAD_RETURN
   - XIL_AXI_CMD_PAYLOAD_RETURN
   - XIL_AXI_WLAST_PAYLOAD_RETURN
   - XIL_AXI_WLAST_PAYLOAD_RETURN

6. The user environment receives the completed transaction if the driver return item policy is not XIL_NO_RETURN.

![Diagram of Write Transaction Flow](image-url)
Appendix C: AXI VIP Agent and Flow Methodology

Read Command Timing Diagram

- GET
  - Address Channel Delay (Driver Property)
  - Address Insertion Delay (Transaction)
  - AR Back Pressure Delay from Slave
- Assert ARVALID
- Address Accepted
- Address Channel Done

Figure C-4: Read Command Diagram
Appendix C: AXI VIP Agent and Flow Methodology

Read Transaction Flow

An AXI master read transaction flows through the read agent in the following steps:

1. Driver asks for the next transaction through a `get_next_item`. This is a blocking get.
2. The user environment creates a single transaction. The transaction contains the following:
   - **Command Information** – AWADDR, AWLEN, AWSIZE, AWID, etc.
   - **Master Controlled Timing** – Address delay
3. The user environment pushes the transaction to the driver.
4. The driver pops the transaction from the REQUEST port and places it on a queue to be processed and driven onto the interface. If the transaction depth > 1, the driver continues to accept transactions until this value has been met.
5. When the interface receives the RDATA from the slave for the given RID, it fills in the Payload field as RDATA byte array, RRESP.
6. The user environment receives the completed transaction when the transaction driver return item policy is set to either XIL_AXI_CMD$return item policy is set to either XIL_AXI_CMD\_RETURN or XIL\_AXI\_CMD\_PAYLOAD\_RETURN.

![Read Transaction Flow Diagram](image)

Figure C-5: Read Transaction Flow

BREADY Data Flow

- BREADY is generated independently of the AW and W channels.
- Configuration of the BREADY does not come from a transaction or analysis port as the transaction that carries the AW and W payload.
- BREADY configuration can change at different times than the AW/W channels.
- See the Configurable Ready Delays for different timing options.
Appendix C: AXI VIP Agent and Flow Methodology

Figure C-6: BREADY Data Flow
Appendix C: AXI VIP Agent and Flow Methodology

**RREADY Data Flow**

- RREADY is generated independently of the AR channel.
- Configuration of the RREADY is not from the same transaction or analysis port as the transaction that carries the AR payload.
- RREADY configuration can change asynchronously to the AR channels.
- See the Configurable Ready Delays for different timing options.
Appendix C: AXI VIP Agent and Flow Methodology

Figure C-7: RREADY Data Flow
AXI Slave Agent

When instantiating an AXI slave VIP, a slave agent has to be declared and constructed. Class axi_slv_agent contains other components that consist of the entire slave Verification IP. These are the read driver, write driver, and monitor.

AXI Slave Read Driver

- Receives AR Command from the interface and then passes that command to the user environment. Create a READ transaction and pass it back to the driver to drive the R channel.
- Triggers an event when the AR Command is accepted.
- Triggers an event when the RLAST is accepted.
- Receives READY transactions from the user environment and drives the ARREADY signal of the AR channel.
- Drives the R channel.
- Configurable command reordering.
**AXI Slave Write Driver**

- Receives AW Command and the WLAST from the interface and then passes that transaction to the user environment. The user environment creates a BRESP transaction and pass it back to the driver to drive the B channel.
- Receives WRITE transactions from the user environment and drives the AW and W channels.
- Triggers an event when the AW Command is accepted.
- Triggers an event when the WLAST is accepted.
- Receives READY transactions from the user environment and drives the AWREADY signal of the AW channel.
- Receives READY transactions from the user environment and drives the WREADY signal of the W channel.
- Generates reordered B Channel responses.

**AXI Monitor**

- Monitors all five AXI channels: AW, AR, R, W, and B.
- Collects and reorders R Channel beats and returns a completed transaction when the RLAST is accepted.
- Collects and reorders B Channel response and returns a completed transaction when the B channel is accepted.
- Transaction-based protocol checking.
Appendix C: AXI VIP Agent and Flow Methodology

Write Response/Reaction Data Flow Diagram

Figure C-9: Write Response/Reaction Data Flow
Appendix C: AXI VIP Agent and Flow Methodology

Write Transaction Flow

An AXI slave write agent has three concurrent transaction flows:

- Address channel servicing
- Data channel serving
- Response channel generation

Both the address and data channels have their READY responses configured independently from the user environment. Only the response channel, B, relies on communication with the user environment to make forward progress. The transaction flows through the write agent in the following steps:

1. Master write response driver performs a blocking get to the user environment through a `get_next_item`. Because the command has not yet been received, the user environment must wait until the command has been received from the master.

2. The user environment performs a blocking get, `get_next_item`, on the reactive port of the driver.

3. The driver at this time can accept the incoming beats of WDATA and AWADDR and places them in a holding structure.

4. Only after the slave driver receives the complete AWADDR phase and the WDATA phase, it transfers the command object through the reactive port to the user environment.

5. The user environment determines the correct response to the request and puts the complete transaction on the REQUEST port of the driver. The transaction has:

   - **Command Information** – AWADDR, AWLEN, AWSIZE, AWID, etc. From the original command passed to the user environment.

   - **Response Controlled Timing and Response** – Response delay, BRESP.

6. The driver pops the transaction from the REQUEST port and places it on the queue to be processed on the response interface and starts the response channel delay timer. It is possible that before the response channel delay timer has expired more than one transaction can exist in the response list. When there is more than one item on the response list, the driver selects the next response to be sent.

7. When the transaction has been configured to be returned following a BRESP acceptance event, the slave driver fills in the beats WDATA and places it on the RESPONSE port of the driver.

8. The user environment receives the completed transaction.
AWREADY Timing Flow

- AWREADY is generated independently of the AW and W channels.
- Configuration of the AWREADY is not from the same transaction or analysis port as the transaction that carries the AW and W payload.
- AWREADY configuration can change asynchronously to the AW/W channels.
- See the Configurable Ready Delays for different timing options.
Figure C-11: AWREADY Timing Flow
Appendix C: AXI VIP Agent and Flow Methodology

WREADY Timing Flow

- WREADY is generated independently of the AW and W channels.
- Configuration of the WREADY is not from the same transaction or analysis port as the transaction that carries the AW and W payload.
- WREADY configuration can change asynchronously to the AW/W channels.
- See the Configurable Ready Delays for different timing options.
Appendix C: AXI VIP Agent and Flow Methodology

Figure C-12: WREADY Timing Flow

- **Initial WREADY Configuration**
- **Initialize Current WREADY Configuration**
- **GET**
- **WREADY Configuration Queue**
- **Process Current WREADY Configuration**
- **Assert WREADY**
- **Write Beat Accepted**
- **WLAST Asserted**
- **Write Data Channel Done**

If not empty, replace current WREADY configuration.
Appendix C: AXI VIP Agent and Flow Methodology

Read Data/Reaction Data Timing Flow Diagram

Figure C-13: Read Data/Reaction Flow
Appendix C: AXI VIP Agent and Flow Methodology

Read Transaction Flow

An AXI slave read agent has two concurrent transaction flows:

- Address channel servicing
- Data channel serving

The address channel has its READY responses configured through the user environment. The data channel relies on the user environment for timing and payload generation. The transaction flows through the read agent in the following steps:

1. Master read response driver performs a blocking get to the user environment through a `get_next_item`. Because the command has not yet been received the user environment must wait until the command has been received from the master.

2. The user environment performs a blocking get, `get_next_item`, on the reactive port of the driver.

3. The slave driver waits for an ARADDR command.

4. Only after the slave driver receives the completion ARADDR phase, it transfers the command object through the reactive port to the sequencer. The command information consists of the Command Information field with ARADDR, ARLEN, ARSIZE, ARID, etc.

5. The user environment creates a single transaction. The transaction contains the following:
   - **Payload** – RDATA byte array and RRESP array
   - **Slave Controlled Timing** – Inter-beat timing and data insertion delay

6. The driver pops the transaction from the REQUEST port and places it on a queue to be processed and driven on the interface. If the system was idle at the time, the driver starts the slave data channel delay timer.

7. After the expiration of the timer, the driver processes the beats of data to be driven on the interface. In the case of multiple transactions pending and the slave being configured to support read, it interleaves the beats of the pending transactions.

8. Upon the acceptance of the last beat of a given command, if the transaction is configured to be returned to the user environment, the slave driver places it on the RESPONSE port to be sent.

9. The user environment receives the completed transaction.
ARREADY Timing Flow

- ARREADY is generated independently of the AR channel.
- Configuration of the ARREADY is not from the same transaction or analysis port as the transaction that carries the AR payload.
- ARREADY configuration can change asynchronously to the AR channels.
- See the Configurable Ready Delays for different timing options.

Figure C-14: ARREADY Timing Flow
# AXI Pass-Through Agent

When instantiating an AXI pass-through VIP, a pass-through agent has to be declared and constructed. Class `axi_passthrough_agent` contains other components that consist of the entire pass-through Verification IP. The pass-through VIP has the options to be switched to runtime master or runtime slave modes. It includes master read driver, master write driver, slave read driver, slave write driver, and monitor.

### AXI Master Read Driver

The same features as the AXI master read driver in `axi_mst_agent`.

### AXI Master Write Driver

The same features as the AXI master write driver in `axi_mst_agent`.

### AXI Slave Read Driver

The same features as the AXI slave read driver in `axi_slv_agent`.

### AXI Slave Write Driver

The same features as the AXI slave write driver in `axi_slv_agent`.

### AXI Monitor

The same features for both master/slave agent monitors.

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**Figure C-15: AXI Pass-Through VIP Agent**

[Diagram showing AXI Pass-Through Agent components: User Environment, AXI Pass-Through Agent, AXI Monitor, Master Write Driver, Master Read Driver, Slave Write Driver, Slave Read Driver, Virtual Interface, AXI Interface.]

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**X-Ref Target - Figure C-15**

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READY Generation

READY signals of write command channel, write data channel, write response channel, read command channel, and read data channel are generated independently from other attributes. The axi_ready_gen is the class used for READY generation.

Configurable Ready Delays

There is no one way that the READY signals on a channel are supposed to behave. There are no requirements for when READY should be asserted or how long READY should remain asserted, nor any that states that the READY must be asserted following a power up.

The control of the READY signal is set in the DRIVER of the given AGENT. For masters these are:

- RREADY
- BREADY

For slaves these are:

- AWREADY
- ARREADY
- WREADY

To control the generation of the READY signal there are two main configurations, however, to simplify the programming model these might be presented as different configurations.

Table C-2 shows the configurable READY delay description.

<table>
<thead>
<tr>
<th>Member Name</th>
<th>Default</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>use_variable_ranges</td>
<td>FALSE</td>
<td>0..1</td>
<td>When set TRUE, this property instructs the ready_gen class to generate a random value for high_time, low_time, and event_count based on the minimum/maximum ranges. When set FALSE, the ready_gen uses the programmed value of the high_time, low_time, and event_count.</td>
</tr>
<tr>
<td>max_low_time</td>
<td>5</td>
<td>0..2^{32} - 1</td>
<td>Used to constrain the low_time value. Indicates the maximum range of the low_time constraint.</td>
</tr>
<tr>
<td>min_low_time</td>
<td>0</td>
<td>0..2^{32} - 1</td>
<td>Used to constrain the low_time value. Indicates the minimum range of the low_time constraint.</td>
</tr>
<tr>
<td>low_time</td>
<td>2</td>
<td>0..2^{32} - 1</td>
<td>When used, indicates the number of cycles that *READY is driven Low.</td>
</tr>
<tr>
<td>max_high_time</td>
<td>5</td>
<td>0..2^{32} - 1</td>
<td>Used to constrain the high_time value. Indicates the maximum range of the high_time constraint.</td>
</tr>
</tbody>
</table>
### Table C-2: Configurable Ready Delays (Cont’d)

<table>
<thead>
<tr>
<th>Member Name</th>
<th>Default</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>min_high_time</td>
<td>0</td>
<td>0..2^32 - 1</td>
<td>Used to constrain the high_time value. Indicates the minimum range of the high_time constraint.</td>
</tr>
<tr>
<td>high_time</td>
<td>5</td>
<td>0..2^32 - 1</td>
<td>When used, indicates the number of cycles that *READY is driven High.</td>
</tr>
<tr>
<td>max_event_count</td>
<td>1</td>
<td>1..2^32 - 1</td>
<td>Used to constrain the event_count value. Indicates the maximum range of the event_count constraint.</td>
</tr>
<tr>
<td>min_event_count</td>
<td>1</td>
<td>1..2^32 - 1</td>
<td>Used to constrain the event_count value. Indicates the minimum range of the event_count constraint.</td>
</tr>
<tr>
<td>event_count</td>
<td>1</td>
<td>0..2^32 - 1</td>
<td>When used, indicates the number of handshakes that are sampled before the end of the policy.</td>
</tr>
<tr>
<td>event_count_reset</td>
<td>2000</td>
<td>0..2^32 - 1</td>
<td>Watchdog wait time.</td>
</tr>
</tbody>
</table>

**GEN_SINGLE/RAND_SINGLE (Default Policy)**

While this policy is active, it drives the *READY signal 0 for low_time cycles and then drives 1 until one handshake occurs on this channel. The policy repeats until the channel is given a different policy.

![Diagram of GEN_SINGLE/RAND_SINGLE](X18603-031517)

*Figure C-16: GEN_SINGLE/RAND_SINGLE*
**GEN_OSC/RAND_OSC – Assert and Remain Asserted for a Number of Cycles**

When this policy is active, it drives the *READY signal 0 for \( \text{low\_time} \) cycles and then drives 1 for \( \text{high\_time} \) cycles.

*Note:* The *READY does not drop until the specified number of cycles has occurred. The policy repeats until the channel is given a different policy.

Figure C-17 shows that following event A, there is a delay of \( \text{low\_time} \) ACLKS, then READY is asserted. After \( \text{high\_time} \) cycles of ACLK, READY is deasserted and the counter restarts at A.

![Diagram](X18601-031517)

**Figure C-17: GEN_OSC/RAND_OSC**

**GEN_EVENTS/RAND_EVENTS – Assert and Remain Asserted for a Number of Events**

When this policy is active, it drives the *READY signal 0 for \( \text{low\_time} \) cycles and then drives 1 until \( \text{event\_count} \) handshakes occur.

*Note:* There is a built-in watchdog that triggers after the \( \text{event\_cycle\_count\_reset} \) cycles and the programmed number of events has not been satisfied. This terminates that part of the policy. The policy repeats until the channel is given a different policy.

The value of \( \text{low\_time} \) can range from 0 to 256 cycles. The READY remains asserted for N channel accept events, where N can be from 1 to N beats. This allows you to assert a READY after some number of cycles and keep it asserted indefinitely or for some number of events.

When attempting to model a self-draining FIFO, an event cycle count time reset is provided. This allows you to configure the READY to be deasserted after some number of events,
unless the event cycle count time has expired. In this case, the event count resets and the READY remains asserted for N more events.

Figure C-18 shows that following event A, there is a delay of low_time ACLKs, then the READY is asserted. It remains asserted for events E1 to E4 then deasserts since the event count is satisfied. The algorithm then restarts at A.

Figure C-18: GEN_EVENTS/RAND_EVENTS
**GEN_AFTER_VALID_SINGLE/RAND_AFTER_VALID_SINGLE**

This policy is active when *VALID is detected to be asserted. When enabled, it drives the *READY Low for low_time and then asserts the *READY until one handshake has been detected. The policy repeats until the channel is given a different policy.

---

**GEN_AFTER_VALID_EVENTS/RAND_AFTER_VALID_EVENTS**

This policy is active when *VALID is detected to be asserted. When enabled, it drives the *READY Low for low_time and then drives the *READY High until either event_count handshakes have been received OR event_count_reset number of cycles have passed. The policy repeats until the channel is given a different policy.
**GEN_AFTER_VALID_OSC/RAND_AFTER_VALID_OSC**

This policy is active when the *VALID is detected to be asserted. When enabled, it drives the *READY Low for \( \text{low\_time} \) and then drives the *READY High for \( \text{high\_time} \). The policy repeats until the channel is given a different policy.

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**GEN_AFTER_VALID_EVENTS/RAND_AFTER_VALID_EVENTS**

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**Figure C-20: GEN_AFTER_VALID_EVENTS/RAND_AFTER_VALID_EVENTS**

**Figure C-21: GEN_AFTER_VALID_OSC/RAND_AFTER_VALID_OSC**
**GEN_AFTER_RANDOM**

This policy is used to randomly generate different policies including `low_time`, `high_time`, and `event_count`. When used, it randomly selects a new policy when the previous policy has completed.

This uses the minimum/maximum pairs for generating the value of the `low_time`, `high_time`, and `event_count` values.
Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the AXI VIP, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the AXI VIP. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.
Appendix D: Debugging

Master Answer Record for the AXI VIP

AR: 68234

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.
Additional Resources and Legal Notices

Xilinx Resources
For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select Help > Documentation and Tutorials.
- On Windows, select Start > All Programs > Xilinx Design Tools > DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.
References

These documents provide supplemental material useful with this product guide:

1. ARM® AMBA® 3 AXI Protocol Checker (DUI0305C)
2. Instructions on how to download the ARM AMBA AXI specifications are at ARM AMBA Specifications. See the:
   - AMBA AXI4-Stream Protocol Specification
   - AMBA AXI Protocol v2.0 Specification
8. ISE to Vivado Design Suite Migration Guide (UG911)
10. LogiCORE IP AXI Interconnect Product Guide (PG059)
11. Xilinx AXI VIP API Documentation
Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
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<tr>
<td>06/07/2017</td>
<td>1.0</td>
<td>• Added note #5-7 in IP Facts table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added description in Multiple Simulation Sets section in Test Bench chapter.</td>
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<tr>
<td></td>
<td></td>
<td>• Added type definition description in AXI Pass-Through VIP section in Test Bench chapter.</td>
</tr>
<tr>
<td>04/05/2017</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
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