LogiCORE IP ChipScope Pro IBERT for 7 Series GTX Transceivers

DS872 April 24, 2012 **Product Specification**

Introduction

The customizable LogiCORE™ IP ChipScope™ Pro Integrated Bit Error Ratio Test (IBERT) core for 7 series FPGA GTX transceivers is designed for evaluating and monitoring the GTX transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTX transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core
- Provides a user-selectable number of 7 series FPGA GTX transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTX transceivers

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	7 Series				
Supported User Interfaces	N/A				
	Resources(2)				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq. in MHz(3)**
Config1	2,428	3,369	0	0	165
Config2	13,698	20,396	0	0	322.4
Config3	48,358	73,683	0	0	312.5
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Netlist				
Example Design	Verilog /VHDL				
Test Bench	Not Provided				
Constraints File	Xilinx Constraints and Synthesis Constraints				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	Xilinx CORE Generator™ tool				
Simulation	Not Provided				
Synthesis Tools	Not Provided				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. Including the variants for this FPGA device.
2. Resources listed here are for 7 series devices. For more complete device performance numbers, see Table 2.
3. Performance numbers listed are for 7 series FPGAs. For more complete performance data, see Performance and Resource Utilization, page 6.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of 7 Series FPGA GTX transceivers.

Functional Description

The IBERT core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for 7 series FPGA GTX transceivers. Parameterizable to use different GTX transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTX transceiver desired, giving a variety of different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels. In addition, the configuration and tuning of the GTX transceivers is accessible though logic that communicates to the DRP port of the GTX transceiver, in order to change attribute settings, as well as registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

GTX Transceiver Features

The IBERT core is designed for Physical Medium Attachment (PMA) evaluation and demonstration. All the major PMA features of the GTX transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) Divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver channel, there is a ring Phase-Locked Loop (PLL) called Channel PLL (CPLL). The GTX in the 7 series FPGA has an additional shared PLL per quad, Quad PLL (QPLL). This QPLL is shared LC PLL to support high speed, high performance and low power multi-lane applications.

Figure 1 shows a Quad in a 7 series device. The GTXE2_CHANNEL component has the serial transceiver and CPLL units and the GTXE2_COMMON has the QPLL unit.

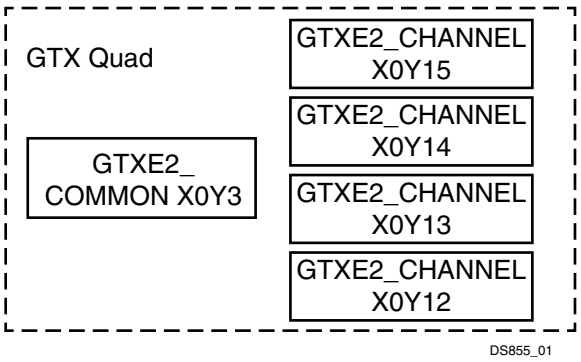

Figure 1: **Quad in a 7 Series Device**

The serial transceiver REFCLK can be sourced from either CPLL or QPLL based on multiplexers as shown in Figure 2. This can be selected from the 7 series FPGA IBERT CORE Generator tools GUI.

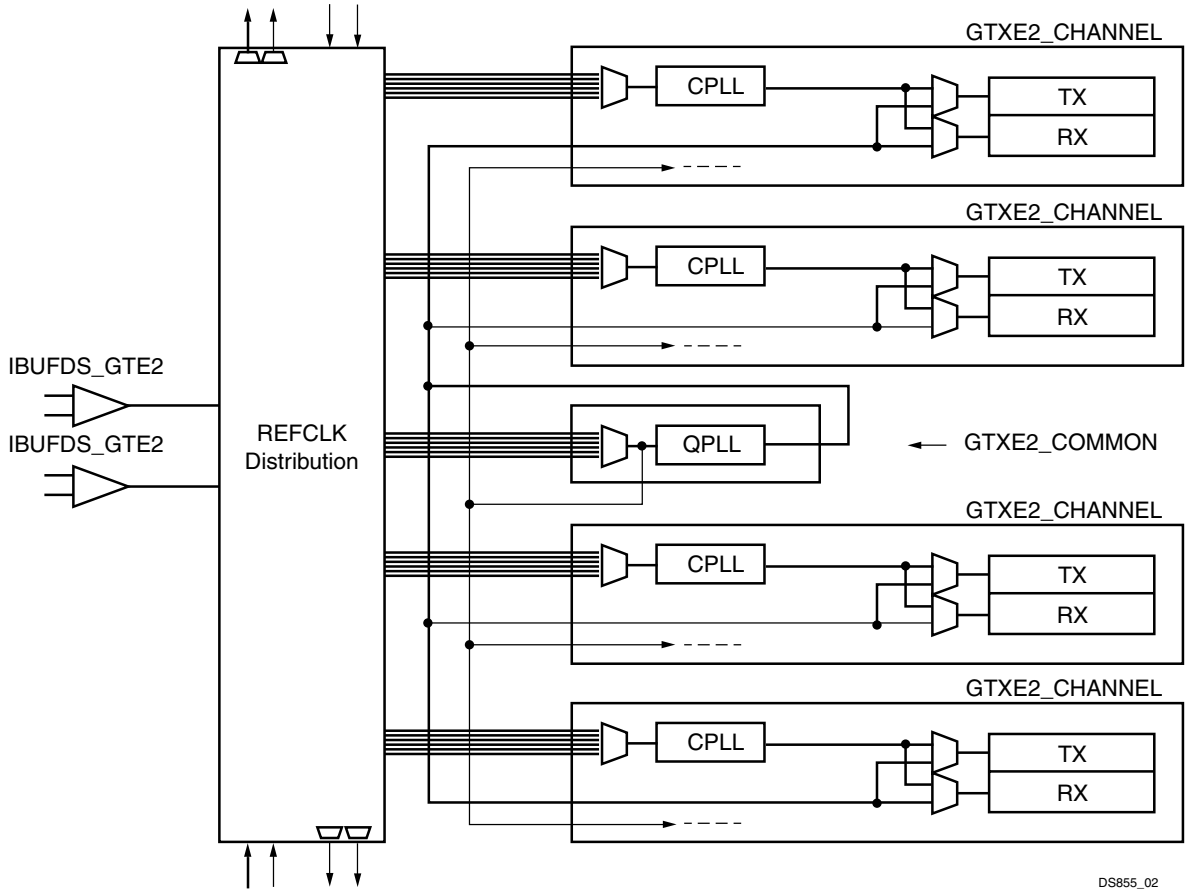

Figure 2: **Serial Transceiver REFCLK Sourcing**

Pattern Generation and Checking

Each GTX transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks

it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX pattern and RX pattern are individually selected.

The Analyzer software displays a 'link' signal until there are five consecutive cycles with errors. Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with errors, the ChipScope Pro Analyzer software disables the link signal. Internal counters accumulate the number of words and errors received.

DRP and Port Access

You can change GTX transceiver ports and attributes. The DRP interface logic allows the run-time software to monitor and change any attribute of the GTX transceivers and the corresponding CPLL/QPLL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTX transceiver. All are accessible at run time using the ChipScope Analyzer tool.

CORE Generator Tool

The CORE Generator tool allows you to define and generate a customized IBERT core to use to validate the transceivers of the device. You can customize the number of serial transceivers, line rate and reference clock, and PLL selection for each serial transceiver.

Entering the Component Name

The Component Name field, stored as `component_name` in the generated XCO parameter file, can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Generating an Example Design

The IBERT CORE Generator tool normally generates example design along with standard Xilinx CORE Generator output files, such as a netlist and instantiation template files. Example design and Implement scripts are generated under the folder with the component name.

Generate Bitstream

The Generate Bitstream is enabled by default. When generated, it runs through the entire implementation flow, including bitstream generation. When Generate Bitstream is disabled and generated, the design runs through synthesis. You can edit the example design and embed the custom design along with the IBERT instance. The implement script provided with the generated files allows you to run the example design until bitstream generation.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

GTX Transceiver Naming Style

There are two conventions for naming the GTX transceiver, based on the location in the serial transceiver tile in the device. M and n in XmYn naming convention indicate the X and Y coordinates of the serial transceiver location. M and n in serial transceiver m_n naming convention indicating serial transceiver number and quad associated.

System Clock

The IBERT core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to orginate from an FPGA pin, or to be driven from the TXOUTCLK port of one of the GTX transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT core design. If the system clock is running faster than 150 MHz, it is divided down internally using an Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. Note that the clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT core.

Line Rate Support

IBERT supports a maximum of three different line rates in a single design. For each of these line rates, you can select a custom value based on your requirements, or you can choose from pre-provided industry standard protocols (for example, CPRI™, Gigabit Ethernet, or XAUI). Specify the number of serial transceivers for each line rate that will be programmed with these settings. Because usage of QPLL is recommended for line rates above 6.5 Gb/s, you can select QPLL/CPLL for each line rate falling in the range 0.6 Gb/s to 6.5 Gb/s.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south quads.

Generating the Core

After entering the IBERT core parameters, click Generate to create the IBERT core files. After the IBERT core has been generated, a list of files that are generated will appear in a separate window called "Readme <corename>".

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTX transceiver reference clocks, the GTX transceiver transmit and receive pins, and a system clock (optional).

Table 1: **Interface Ports**

Port Name	Direction	Description
IBERT_SYSCLOCK_I	IN	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
CONTROL[35:0]	IN/OUT	Control bus connection to the ICON core.
XiYj_TX_P_OPAD-1:0](1) XiYj_TX_P_OPAD[n-1:0](1)	OUT	Transmit differential pairs for each of the n GTX transceivers used.
XiYj_RX_N_IPAD[n-1:0](1) XiYj_RX_P_IPAD[n-1:0](1)	IN	Receive differential pairs for each of the n GTX transceivers used.
Qk_CLK0_MGTREFCLK_I[m-1:0](2) Qk_CLK1_MGTREFCLK_I[m-1:0]	IN	GTX transceiver reference clocks used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTX transceivers can share clock inputs.
XiYj_RXOUTCLK_O(1)	OUT	Quad based RX output clock.

1. The XiYj name refers to the GTX site location.
2. The Qk name refers to the GTX quad site location.

Performance and Resource Utilization

Table 2: **Configuration Details**

Configuration	Device	IBERT Setup
Config1	XC7K70T-FBG676-1	1 GT, 1 protocol set to 40b data width at 6.6 Gb/s with QPLL enabled. Dependent RX/TX user clocking disabled.
Config2	XC7VX485T-FFG1761-2	8 GTs, 2 protocols set to 32b data width at 10 Gb/s with QPLL enabled. Dependent RX/TX user clocking disabled.
Config3	XC7VX485T-FFG-1761-3	28 GTs, 1 protocol set to 40b data width at 12.5 Gb/s with Quad PLL enabled. Dependent RX/TX user clocking enabled.

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

More information about the ChipScope Pro software and cores is available in the *Chipscope Pro Software and Cores User Guide*, located at www.xilinx.com/documentation.

For more information about the 7 series FPGA GTX transceiver, see the *7 Series FPGAs GTX Transceivers User Guide*, located at www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that

are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The IBERT core is provided under the Xilinx ISE® Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator system 13.3 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Spelled Out
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The following table shows a summary of changes to this document:

Date	Version	Description of Revisions
04/24/12	1.0	Initial Xilinx release.

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