

## Introduction

The ChipScope™ Pro Integrated Bit Error Ratio Tester (IBERT) core for Virtex-5 GTP is a customizable core that can be used to evaluate and monitor the health of Virtex-5 GTP Transceivers. The design includes pattern generators and checkers implemented in FPGA logic, as well as access to the ports and DRP attributes of the MGTs. Communication logic is also included, to allow the design to be runtime accessible through JTAG. The IBERT core is a self-contained design, and when it is generated, will run through the entire implementation flow, including bitstream generation.

## Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core.
- Has user-selectable number of Virtex-5 GTP Transceivers.
- Each transceiver can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width.
- Requires a system clock that can be sourced from a pin or one of the enabled MGTs.

For more information about the IBERT core, refer to the *ChipScope Pro Software and Cores User Guide*.

LogiCORE IP Facts				
Core Specifics				
Supported Device Family <sup>(1)</sup>	Virtex®-5			
Resources Used <sup>(2)</sup>	I/O	LUTs	FFs	Block RAMs
	4	2634	2768	0
Special Features	N/A			
Provided with Core				
Documentation	Product Specification			
Design File Formats	N/A			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Reference Designs /Application Notes	None			
Additional Items	.bit (design bitstream)			
Design Tool Requirements				
Xilinx Implementation Tools	Xilinx® ISE® 11.3			
Verification	ChipScope Pro 11.3			
Simulation	Not supported in simulation			
Synthesis	Netlist is pre-synthesized by XST			
Support				
Provided by Xilinx, Inc.				

1. Including the variants of these FPGA device families.
2. For single-MGT design with 20-bit fabric width

## Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Virtex-5 GTP Transceivers.

## Functional Description

The IBERT core provides a broad-based PMA evaluation and demonstration platform for Virtex-5 GTP Transceivers. Parameterizable to use different MGTs and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and fabric widths. Data pattern generators and checkers are included for each MGT desired, giving a variety of different PRBS and clock patterns to be sent over the channels. In addition, the configuration and tuning of the MGTs is accessible through logic that communicates to the DRP port of the MGT, in order to change attribute settings, as well as registers that control the values on the ports. At runtime, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

## MGT Features

IBERT is designed for PMA evaluation and demonstration. All the major PMA features of the MGT are supported and controllable in IBERT, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- PLL Divider settings

Some of the PCS features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

## Pattern Generation and Checking

Each MGT enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns. These patterns are optimized for the fabric width chosen, and are selectable at runtime. The TX pattern and RX pattern are individually selectable.

The pattern checker logic also generates a 'link' signal that displays in the Analyzer software. The channel is linked when there are five consecutive cycles of data with no errors. The incoming data is compared against a pattern that is generated internally. When the checker receives five consecutive cycles of data with errors, it removes the channel link. Internal counters accumulate the number of words and error received.

## DRP and Ports Access

IBERT also provides flexibility for the user to change MGT ports and attributes. DRP interface logic is included that allows the runtime software to monitor and change any attribute in any of the MGTs included in the IBERT core. Readable and writable (when applicable) registers are also included that are connected to the various ports of the MGT. All are accessible at runtime using the ChipScope Analyzer tool.

## System Clock

The IBERT Core requires a free-running system clock to clock the communication and other logic included in the IBERT core. This clock can be chosen at generation time to come from an FPGA pin, or be driven from the TXOUTCLK port of one of the MGTs in the core. If the system clock is running faster than 150 MHz, it is divided down internally using an DCM to satisfy timing constraints.

## IBERT Interface Ports

The I/O signals of the IBERT core consist only of the MGT reference clocks, the MGT transmit and receive pins, and a system clock (optional).

*Table 1: ILA Interface Ports*

Port Name	Direction	Description
SYSCLK	IN	Design clock that clocks all communication logic. This port is optional, because you can select an internal MGT clock at generation time to perform this function.
TXN[n-1:0], TXP[n-1:0]	OUT	Transmit differential pairs for each of the n MGTs used.
RXN[n-1:0], RXP[n-1:0]	OUT	Receive differential pairs for each of the n MGTs used.
MGTREFCLK_P[ m-1:0], MGTREFCLK_N[ m-1:0]	IN	MGT reference clocks used. Not necessarily m = n because some MGTs can share clock inputs.

## Restrictions

Only one IBERT core can be generated for a device, and the IBERT core will constitute the entire design. The IBERT core cannot be merged in with user logic.

## Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

## References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at <http://www.xilinx.com/documentation>.
- Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11 online help, located at <http://www.xilinx.com/documentation>.
- Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at <http://www.xilinx.com/documentation>.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Ordering Information

The IBERT core is provided under the ISE Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator system 11 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Please contact your local Xilinx [sales representative](#) for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/19/2010	1.0	Release 12.1 (Initial Xilinx release).

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