# ChipScope Pro Integrated Bit Error Ratio Test (IBERT) for Virtex-5 FPGA GTX (v2.01a)

DS774 October 19, 2011

**Product Specification**

## Introduction

The ChipScope™ Pro IBERT core for Virtex®-5 FPGA GTX transceivers is a customizable core that can be used to evaluate and monitor Virtex-5 FPGA GTX transceivers. The design includes pattern generators and checkers implemented in FPGA logic, as well as access to the ports and DRP attributes of the transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. The IBERT core is a self-contained design and when it is generated, it will run through the entire implementation flow, including bitstream generation.

## Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core.
- Has user-selectable number of Virtex-5 GTX transceivers.
- Each transceiver can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width.
- Requires a system clock that can be sourced from a pin or one of the enabled GTX transceivers.

For more information about the IBERT core, see the *ChipScope Pro Software and Cores User Guide*.

| LogiCORE IP Facts Table | | | | | |
|---|---|---|---|---|---|
| **Core Specifics** | | | | | |
| Supported Device Family(1) | Virtex-5 | | | | |
| Supported User Interfaces | N/A | | | | |
| | **Resources(2)** | | | | **Frequency** |
| Configuration | **LUTs** | **FFs** | **DSP Slices** | **Block RAMs** | **Max. Freq. (MHz)(3)** |
| Config 1 | 2589 | 3938 | 0 | 0 | |
| **Provided with Core** | | | | | |
| Documentation | Product Specification User Guide | | | | |
| Design Files | Not Provided | | | | |
| Example Design | Not Provided | | | | |
| Test Bench | Not Provided | | | | |
| Constraints File | Not Provided | | | | |
| Simulation Model | Not Supported in Simulation | | | | |
| **Tested Design Tools** | | | | | |
| Design Entry Tools | Xilinx CORE Generator™ tool | | | | |
| Synthesis Tools | Not Provided. | | | | |
| **Support** | | | | | |
| Provided by Xilinx @ www.xilinx.com/support | | | | | |

1. Includes the device derivatives/variants of this FPGA device family.
2. One GT-DUAL selected running at 3.125 Gb/s using 40-bit data width and an internal system clock on an XC5VFX70T part.
3. Performance numbers listed are for Virtex-5 FPGAs. For more complete performance data, see Table 2.

## Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Virtex-5 FPGA GTX transceivers.

## Functional Description

The IBERT core provides a broad-based PMA evaluation and demonstration platform for Virtex-5 GTX transceivers. Parameterizable to use different transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and fabric widths. Data pattern generators and checkers are included for each transceiver desired, giving a variety of different PRBS and clock patterns to be sent over the channels. To change attribute settings, the configuration and tuning of the transceivers is accessible though logic that communicates to the DRP port of the transceiver, as well as registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

## GTX Transceiver Features

IBERT is designed for PMA evaluation and demonstration. All the major PMA features of the transceiver are supported and controllable in IBERT, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- PLL Divider settings

Some of the PCS features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

### Pattern Generation and Checking

Each transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns. These patterns are optimized for the fabric width chosen, and are selectable at run time. The TX pattern and RX pattern are individually selectable.

The pattern checker logic also generates a 'link' signal that displays in the Analyzer software. The channel is linked when there are five consecutive cycles of data with no errors. The incoming data is compared against a pattern that is generated internally. When the checker receives five consecutive cycles of data with errors, it removes the channel link. Internal counters accumulate the number of words and error received.

### DRP and Ports Access

IBERT also provides flexibility for the user the change transceiver ports and attributes. DRP interface logic is included that allows the run time software to monitor and change any attribute in any of the transceivers included in the IBERT core. Readable and writable (when applicable) registers are also included that are connected to the various ports of the transceiver. All are accessible at run time using the ChipScope Analyzer tool.

### System Clock

The IBERT Core requires a free-running system clock to clock the communication and other logic included in the IBERT core. This clock can be chosen at generation time to come from an FPGA pin, or be driven from the TXOUTCLK port of one of the transceiver in the core. If the system clock is running faster than 150 MHz, it is divided down internally using an DCM to satisfy timing constraints.

## Generating the IBERT v2.0 Core

The Xilinx CORE Generator™ tool allows you to define and generate a customized IBERT v2.0 core for Virtex-5 FPGA GTX transceivers. When all the IBERT parameters are selected, a full design is generated, including a bitstream. The IBERT core cannot be included in your design; it can only be generated in its own standalone design. The ISE tools are invoked by the Xilinx CORE Generator to generate a bitstream file (.bit) rather than a design netlist file (.ngc or .edn).

### Generating the IBERT Core

1. In the **Debug & Verification > ChipScope Pro** category of the CORE Generator tool, select the I**BERT Virtex5 GTX** (ChipScope Pro - IBERT) core.
2. Click the **Customize and Generate** in the right side of the window.

### General IBERT Options

The first screen in the IBERT Core customization wizard is used to set up general IBERT options.

#### Choosing the Component Name

The Component Name field can consist of any combination of alpha-numeric characters in addition to the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

#### Selecting the Number of Line Rates (Protocols)

The IBERT Core can have multiple transceivers, which do not have to operate at the same line rate, or use the same reference clock. Choose the number of distinct line rate/reference clock rate combinations needed from the Number of Line Rates (protocols) dialog.

#### Choosing the Line Rate Settings

For each line rate setting desired, choose between a custom setting (“Start from scratch”) or a pre-defined protocol setting from the Protocol combo box. If a named protocol is chosen, the fields for Max Rate, Data Width, and REFCLK are filled out automatically, according to the protocol. If specifying a custom protocol, enter the desired values.

## Selecting the GTX_DUALs and Reference Clocks

After selecting the protocol options for the IBERT core, click **Next** to view the **Select GTXs and Reference Clocks for Line Rate 1** panel. After youtransceiver have customized the Line Rate 1 selections, click **Next** to go on to Line Rate 2. Continue until all the line rates are completed.

### Choosing GTX_DUALs

Each GTX_DUAL (also referred to as "DUAL" in this section) available is listed with its location, each with a checkbox beside it. If the checkbox is greyed out, that means that transceiver is already configured with a different line rate. Check the DUALs that will use the given line rate. At generate time, transceivers within a DUAL must be configured at the same line rate.

### Choosing REFCLK Sources

From the dialog, choose the reference clock desired to clock the transceiver. One reference clock is available from the DUAL, and reference clocks are also available from neighboring DUALs. See the *Virtex-5 FPGA GTX Transceiver User Guide* for more information on the clocking topology.

## Enabling RXRECCLK Probes

After selecting the GTX transceivers and REFCLK options for the IBERT core for all the line rates, click Next to view the RXRECCLK options.

For each of the GTX transceivers used, it is possible to drive the RXRECCLK (recovered clock) out to a pin for use in external measurement. To enable this, check the Enable checkbox next to the desired recovered clock. Then specify the pin location in the Location text field, and choose the I/O Standard from the IO Standard combo box. For differential standards, specify the P pin location.

## Choosing the System Clock Source

After selecting the RXRECCLK probing options, click Next to view the System Clock options.

IBERT needs a clock for the internal communication logic. Ideally, this comes from an external pin but can also be driven from a GTX transceiver TXOUTCLK. To use a clock from a pin, enable the Use External Clock source radio button, type the frequency in the Frequency field, type the pin location in the Pin Location field, and choose the Pin Input Standard. For differential standards, specify the P pin location.

To specify an internal clock, enable the Use Internal REFCLK radio button and specify the GTX transceiver in the Use REFCLK from combo box.

## Generating the Design

After entering the IBERT core parameters, click **Next** to view the IBERT Design Summary. This includes the GTX transceivers used, system clock, and the details of the global clock resources used. To generate the design, click **Generate**.

## IBERT Interface Ports

The I/O signals of the IBERT core consist only of the transceiver reference clocks, the transceiver transmit and receive pins, and a system clock (optional).

*Table 1:* **IBERT Interface Ports**

| Port Name | Direction | Description |
|---|---|---|
| IBERT_SYSCLK_P_IPAD<br>IBERT_SYSCLK_N_IPAD | IN | Design clock that clocks all communication logic. This port is optional, because you can select an internal transceiver clock at generation time to perform this function. |
| X*m*Y*n*_TX0_P_OPAD<br>X*m*Y*n*_TX0_N_OPAD<br>X*m*Y*n*_TX1_P_OPAD<br>X*m*Y*n*_TX1_N_OPAD | OUT | Transmit differential pairs for each of the transceivers used.(1) |
| X*m*Y*n*_RX0_P_IPAD<br>X*m*Y*n*_RX0_N_IPAD<br>X*m*Y*n*_RX1_P_IPAD<br>X*m*Y*n*_RX1_N_IPAD | IN | Receive differential pairs for each of the transceivers used.(1) |
| X*m*Y*n*_REFCLK_P_IPAD<br>X*m*Y*n*_REFCLK_N_IPAD | IN | Transceiver reference clocks used.(1) |

1.*m* = GT column. Possible values are 0 and 1. *n* = GT row. Possible values are 0 to 11.

### Performance and Resource Utilization

*Table 2:* **Configuration Details**

| Configuration | Device | Setup |
|---|---|---|
| Config 1 | XC5VFX70T-1FFG1136 | One serial transceiver with line rate set to 3.125 Gb/s |

### Restrictions

Only one IBERT core can be generated for a device, and the IBERT core will constitute the entire design. The IBERT core cannot be merged in with user logic.

## Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

## References

- More information on the ChipScope Pro software and cores is available in the *ChipScope Pro Software and Cores User Guide*, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 12 online help, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at http://www.xilinx.com/documentation.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Ordering Information

The IBERT core is provided under the ISE Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator system 13 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

## List of Acronyms

| Acronym | Definition |
|---|---|
| CPRI | Common Packet Radio Interface |
| DFE | Decision Feedback Equalizer |
| DRP | Dynamic Reconfiguration Port |
| FF | Flip-Flop |
| FPGA | Field Programmable Gate Array |
| IBERT | Integrated Bit Error Ratio Tester |
| I/O | Input/Output |
| ILA | Integrated Logic Analyzer |
| ISE | Integrated Software Environment |
| JTAG | Joint Test Action Group |
| LUT | Lookup Table |
| MMCM | Mixed-Mode Clock Manager |
| MHz | Mega Hertz |
| PCS | Physical Coding Sublayer |
| PLL | Phase-Locked Loop |
| PMA | Physical Medium Attachment |
| PRBS | Pseudorandom binary sequence |
| RAM | Random Access Memory |
| RX | Receive |
| TX | Transmit |
| XAUI | eXtended Attachment Unit Interface |

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 04/19/2010 | 1.0 | Release 12.1(Initial Xilinx release). |
| 10/19/2011 | 2.0 | • Updated for ISE 13.3 support and tools<br>• Added section for generating the IBERT core using Xilinx CORE Generator software<br>• Updated notice of disclaimer and copyright information<br>• Replaced use of MGT with term transceiver throughout document |

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