ChipScope Pro Integrated Bit Error Ratio Test (IBERT) for Virtex-6 FPGA GTH Transceivers

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Product Specification

Introduction

The Xilinx ChipScope™ Pro IBERT core for Virtex®-6 FPGA GTH transceivers is customizable and can be used to evaluate and monitor the GTH transceivers. The design includes pattern generators and checkers implemented in FPGA logic, and access to the ports and DRP attributes of the serial transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. The IBERT core is a self-contained design; when generated, it runs through the entire implementation flow, including bitstream generation.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core.
- Has a user-selectable number of Virtex-6 FPGA GTH transceivers.
- Each transceiver can be customized for the desired line rate, reference clock rate, reference clock source, and datapath width.
- Requires a system clock sourced from a pin.

For more information about the IBERT core, see the *ChipScope Pro Software and Cores User Guide*.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-6				
Supported User Interfaces	N/A				
	Resources				**Frequency**
Configuration (2)	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	5561	7649	0	0	248
Config2	10735	14688	0	0	251
Config3	15946	21730	0	0	274
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Netlist				
Example Design	Verilog/VHDL				
Test Bench	Not Provided				
Constraints File	Xilinx Constraints and Synthesis Constraints				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	Xilinx CORE Generator™ software				
Simulation	Not Provided				
Synthesis Tools	Not Provided				
Support					
Provided by Xilinx, Inc.					

1. Includes variants for this FPGA device.
2. For configuration details, see Table 2, page 5.

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Virtex-6 FPGA GTH transceivers.

Functional Description

The IBERT core provides a broad-based PMA evaluation and demonstration platform for Virtex-6 FPGA GTH transceivers. Parameterizable to use different serial transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and fabric widths. Data pattern generators and checkers are included for each serial transceiver desired, giving a variety of different PRBS and clock patterns to be sent over the channels. The configuration and tuning of the transceivers is accessible though logic that communicates to the DRP port of the transceiver to change attribute settings and registers that control the values on the ports. At runtime, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

Features

IBERT is designed for PMA evaluation and demonstration. All the major PMA features of the GTH transceivers are supported and controllable in IBERT, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- DFE
- PLL Divider settings

Some of the PCS features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

Pattern Generation and Checking

Each GTH transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(11111111110000000000...) patterns. These patterns are optimized for the fabric width chosen, and are selectable at runtime. The TX pattern and RX pattern are individually selectable.

The pattern checker logic also generates a ‘link’ signal that displays in the Analyzer software. The channel is linked when there are five consecutive cycles of data with no errors. The incoming data is compared against a pattern that is generated internally. When the checker receives five consecutive cycles of data with errors, it removes the channel link. Internal counters accumulate the number of words and error received.

DRP and Ports Access

IBERT also provides flexibility for the user the change GTH transceiver ports and attributes. DRP interface logic is included that allows the runtime software to monitor and change any attribute in any of the GTH transceivers included in the IBERT core. Readable and writable (when applicable) registers are also included that are connected to the various ports of the GTH transceiver. All are accessible at runtime using the ChipScope Analyzer tool.

System Clock

The IBERT Core requires a free-running system clock to clock the communication and the DRP ports of the QUADs. You must choose this clock at generation time to come from an FPGA pin. If the system clock is running faster than 150 MHz, it is divided down internally using an MMCM to satisfy timing constraints.

Generating IBERT Cores

Xilinx CORE Generator software provides the ability to define and generate a customized IBERT core for Virtex-6 HXT FPGA GTH transceivers. When all the IBERT parameters have been chosen, a full design is generated, including a bitstream. The IBERT core cannot be included in your design; it can only be generated in its own stand-alone design. The ISE tools are invoked by CORE Generator to generate a bitstream file (.bit) in addition to a design netlist file (.ngc or .edn).

1. In the **Debug & Verification > ChipScope Pro IP** category of the CORE Generator tool, select **IBERT Virtex6 GTH** (ChipScope Pro - IBERT) core.
2. Click the Customize and Generate link in the right side of the window.

General IBERT Options

The first screen in the CORE Generator tool is used to set up general IBERT options.

Choosing the Component Name

The Component Name field can consist of any combination of alpha-numeric characters including the underscore ("_") symbol. However, the underscore symbol cannot be the first character in the component name.

Choosing to Generate a Bitstream

The Generate Bitstream checkbox selects whether the implementation tools suite is used to fully implement the IBERT design when the Generate button is eventually pressed. Unchecking this box will generate some netlist files and a script to implement the design at a later time.

Adding RXRECCLK Probes

Checking the Add RXRECCLK probe checkbox enables a panel later in customization process for you to choose which RXRECCLK signals to route to FPGA pins and the parameters of those pins.

GTH Naming Style

Each GTH transceiver can be identified using two different schemes: an XY coordinate or an GTH transceiver number. Choosing the preference in this combo box causes all future references to GTH transceivers to use that convention.

Using an External Clock Source

The IBERT design requires use of an external clock source for the internal communication logic. This clock must come from an external pin. To set up your external clock, type the frequency in the Frequency field, type the pin

location in the Pin Location field, and choose the Pin Input Standard. For differential standards, specify the P pin location (the N pin location is inferred).

Setting up Protocols

After selecting the IBERT general options, click Next to view the protocol options panel.

Selecting the Number of Protocols

The IBERT core can have multiple GTH transceivers present, and those transceivers do not have to operate at the same line rate, or use the same reference clock. Choose the number of distinct line rate/reference clock rate combinations needed from the Number of Protocols dialog.

Choosing the Line Rate Settings

For each line rate setting desired, choose between a custom setting ("Name Protocol") or a pre-defined protocol setting from the Protocol combo box. If a named protocol is selected, the fields for Max Rate, Data Width, and REFCLK are automatically filled according to the protocol. If specifying a custom protocol, enter the desired values.

The IBERT v2.0 core for Virtex-6 FPGA GTH transceivers supports all protocol line rates in the following ranges:

- 1.24 Gb/s to 1.397 Gb/s
- 2.48 Gb/s to 2.795 Gb/s
- 4.96 Gb/s to 5.591 Gb/s
- 9.92 Gb/s to 11.182 Gb/s

See the *Virtex-6 FPGA GTH Transceivers User Guide* for more information.

Assigning the GTH Transceivers

After selecting the protocol options for the IBERT core, click Next to view the first GTH Transceiver Options panel. For each transceiver you see, set the combo box to None (if the transceiver is not used) or to any of the protocols defined on the previous panel. Click Next to do the same on the next panel of transceivers.

Choosing REFCLK Sources

After selecting which transceivers should be enabled in the IBERT core, click Next to view the REFCLK Source Options panel. For each transceiver you see, choose the reference clock source from the combo box given.

Choosing RXRECCLK Probes (Optional)

After selecting the REFCLK sources for each transceiver, click Next to view the RXRECCLK Probes option panel. This panel is displayed only if Add RXUSERCLK Probe was checked in the first panel.

Generating the Design

After entering the IBERT core parameters, click **Next** to view the IBERT Design Summary. This includes the GTH transceiver used, system clock, and the details of the global clock resources used. To generate the design, click **Generate**.

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTH transceiver reference clocks, the GTH transceiver transmit and receive pins, and a system clock (optional).

Table 1: **Interface Ports**

Port Name	Direction	Description
SYSCLK	IN	Design clock that clocks all communication logic and the DRP ports of the GTH transceiver.
TXN[n-1:0], TXP[n-1:0]	OUT	Transmit differential pairs for each of the n GTH transceivers used.
RXN[n-1:0], RXP[n-1:0]	IN	Receive differential pairs for each of the n GTH transceivers used.
MGTREFCLK_P[m-1:0], MGTREFCLK_N[m-1:0]	IN	GTH transceiver reference clocks used. Not necessarily m = n because some GTH transceivers can share clock inputs.

Restrictions

Only one IBERT core can be generated for a device, and the IBERT core will constitute the entire design. The IBERT core cannot be merged in with user logic.

Configuration

Table 2: **Configuration Details**

Configuration Name	Device	IBERT Setup
Config1	xc6vhx255t-ff1155-1	1 Quad (4 GTHs) with line rate set to 9.92 Gb/s
Config2	Xc6vhx380t-ff1155-2	2 Quads (8 GTHs) with line rate set to 10 Gb/s
Config3	Xc6vhx565t-ff1924-2	3 Quads (8 GTHs) with line rate set to 10 Gb/s

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio 11.1 online help, located at http://www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The IBERT core is provided under the ISE® Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator™ system 13.3. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Spelled Out
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/24/09	1.0	Release 11.2 (Initial Xilinx release).
05/03/10	2.0	Release 12.1, minor error correction.
12/14/10	3.0	Release 12.4. Update core and tool versions.Added Configuration, page 5.
10/19/11	4.0	Updated for ISE v13.3 tools and software. Added section for Generating the IBERT v2.0 cores Added list of acronyms

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