LogiCORE IP ChipScope IBERT for Virtex-6 FPGA GTX Transceivers

DS732 October 19, 2011 **Product Specification**

Introduction

The ChipScope™ Pro IBERT core for Virtex®-6 GTX transceivers can be used to evaluate and monitor GTX transceivers. The design includes pattern generators and checkers implemented in FPGA logic, and access to the ports and dynamic reconfiguration port (DRP) attributes of the GTX transceivers. Communication logic is also included to allow the design to be run-time accessible through JTAG. The IBERT core is a self-contained design. When generated, it will run through the entire implementation flow, including bitstream generation.

Features

- Provides a communication path between the ChipScope Pro Analyzer software and the IBERT core
- Contains a user-selectable number of Virtex-6 GTX transceivers
- Transceivers can be customized for desired line rate, reference clock rate, reference clock source, and datapath width
- Requires a system clock that can be sourced from a pin or one of the enabled GTX transceivers

For more information about the IBERT core, see the *ChipScope Pro Software and Cores User Guide*.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-6				
Supported User Interfaces	N/A				
	Resources(2)				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq. in MHz(3)**
Config1	2476	3114	0	0	398.955
Config2	17123	22316	0	0	398.955
Config3	73847	54926	0	0	398.955
Provided with Core					
Documentation	Product Specification				
Design Files	Product Specification User Guide				
Example Design	Netlist				
Test Bench	Verilog /VHDL				
Constraints File	Not Provided				
Simulation Model	Xilinx Constraints and Synthesis Constraints				
Tested Design Tools					
Design Entry Tools	Xilinx CORE Generator™ tool				
Simulation	Not Provided				
Synthesis Tools	Not Provided				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. Including the variants of this FPGA device.
2. Resources listed here are for Virtex®-6 devices. For more complete device performance numbers, see Table 2.
3. Performance numbers listed are for Virtex-6 FPGAs. .

Applications

The IBERT core is designed to be used in any application that requires verification or evaluation of Virtex-6 GTX transceivers.

Functional Description

The IBERT core provides a broad-based PMA evaluation and demonstration platform for Virtex-6 GTX transceivers. Parameterizable to use different GTX transceivers and clocking topologies, the IBERT core can also be customized to use different line rates, reference clock rates, and fabric widths. Data pattern generators and checkers are included for each GTX transceiver desired, giving a variety of different PRBS and clock patterns to be sent over the channels. In addition, the configuration and tuning of the GTX transceivers is accessible though logic that communicates to the DRP port of the GTX transceiver, to change attribute settings, as well as registers that control the values on the ports. At run time, the ChipScope Analyzer tool communicates to the IBERT core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT core.

GTX Transceiver Features

IBERT is designed for PMA evaluation and demonstration. All the major PMA features of the GTX transceiver are supported and controllable in IBERT, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- PLL Divider settings

Some of the PCS features offered by the transceiver are outside the scope of IBERT, including

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

Pattern Generation and Checking

Each GTX transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS31-bit, Clk 2x (101010...) and Clk 10x(1111111110000000000...) patterns. These patterns are optimized for the fabric width chosen, and are selectable at run time. The TX pattern and RX pattern are individually selectable.

The ChipScope Analyzer software displays a 'link' signal until there are five consecutive cycles with errors. Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with errors, the Analyzer software disables the link signal. Internal counters accumulate the number of words and error received.

DRP and Port Access

IBERT also provides flexibility for the user the change GTX transceiver ports and attributes. DRP interface logic is included that allows the run time software to monitor and change any attribute in any of the GTX transceivers included in the IBERT core. When applicable, readable and writable registers are also included that are connected to the various ports of the GTX transceiver. All are accessible at run time using the ChipScope Analyzer tool.

System Clock

The IBERT Core requires a free-running system clock to clock the communication and other logic included in the IBERT core. This clock can be chosen at generation time to come from an FPGA pin, or be driven from the TXOUTCLK port of one of the GTX transceivers in the core. If the system clock is running faster than 150 MHz, it is divided down internally using an MMCM to satisfy timing constraints.

Generating the IBERT Core

Xilinx CORE Generator™ software provides the ability to define and generate a customized IBERT v2.0 core for Virtex-6 GTX transceivers. When all the IBERT parameters are selected, a full design is generated, including a bitstream. The IBERT core cannot be included in your design; it can only be generated in its own stand-alone design. The ISE tools are invoked by the Xilinx CORE Generator tool to generate a bitstream file (.bit) rather than a design netlist file (.ngc or .edn).

To generate the core:

1. In the **Debug & Verification > ChipScope Pro** category of the IP catalog, select the **IBERT Virtex6 GTX (ChipScope Pro - IBERT)** core.
2. Click the **Customize and Generate** link in the right side of the window to open the IBERT core customization wizard.

General IBERT Options

The first screen in the IBERT core customization wizard is used to set up general IBERT options.

Choosing the Component Name

The **Component Name** field can consist of any combination of alpha-numeric characters and the underscore ("_") symbol. However, the underscore symbol cannot be the first character in the component name.

Selecting the Number of Line Rates (Protocols)

The IBERT core can have multiple transceivers present. They do not have to operate at the same line rate or use the same reference clock. Choose the number of distinct line rate/reference clock rate combinations needed from the **Number of Line Rates (protocols)** dialog.

Choosing the Line Rate Settings

For each line rate setting desired, choose between a custom setting ("Start from scratch") or a pre-defined protocol setting from the Protocol dialog. If a named protocol is selected, the fields for **Max Rate**, **Data Width**, and **REFCLK** are automatically filled in according to the protocol. If specifying a custom protocol, type in the desired values.

Selecting the GTX Transceivers and Reference Clocks

After selecting the protocol options for the IBERT core, click **Next** to view the GTX transceiver and Reference Clock Options for Line Rate 1. After Line Rate 1 is complete, click **Next** to set up Line Rate 2. Repeat these steps until all desired line rates are set.

Choosing GTXs

Each available GTX transceiver is listed with its location and a checkbox next to it. If the checkbox is greyed out, that means that GTX is already configured with a different line rate. Use the checkboxes to select the GTXs that will use the given line rate.

Choosing REFCLK Sources

Choose the desired reference clock for the GTX transceiver. Two reference clocks are available from the QUAD tile of the GTX transceiver. Reference clocks are also available from neighboring QUAD tiles. See the *Virtex-6 FPGA GTX Transceivers User Guide* for more information on the clocking topology.

Enabling RXRECCLK Probes

After selecting the GTX transceiver and REFCLK options for the IBERT core for all the line rates, click **Next** to view the RXRECCLK (RX recovered clock) options.

For each of the GTXs used, it is possible to drive the RXRECCLK out to a pin for use in external measurement. To enable this, activate the **Enable** checkbox next to the desired recovered clock. Then specify the pin location in the **Location** text field, and choose the I/O Standard from the **IO Standard** dialog. For differential standards, specify the P pin location (the N pin location is inferred).

Choosing the System Clock Source

After selecting the RXRECCLK probing options, click **Next** to view the System Clock options.

IBERT needs a clock for the internal communication logic. This can come from an external pin or from the TXOUTCLK of one of the GTXs enabled in the IBERT design. To use a clock from a pin, enable **Use External Clock source**, enter the frequency in the **Frequency** field, enter the pin location in the **Pin Location** field, and choose the **Pin Input Standard**. For differential standards, specify the P pin location (the N pin location is inferred).

To specify an internal clock, enable **Use MGT TXOUTCLK**, and specify the GTX transceiver in the **Use TXOUTCLK from** dialog.

Generating the Design

After entering the IBERT core parameters, click **Next** to view the IBERT Design Summary. This includes the GTX transceivers used, system clock, and the details of the global clock resources used. To generate the design, click **Generate**.

IBERT Interface Ports

The I/O signals of the IBERT core consist only of the GTX transceiver reference clocks, the GTX transceiver transmit and receive pins, and a system clock (optional).

Table 1: **Interface Ports**

Port Name	Direction	Description
SYSCLK	IN	Design clock that clocks all communication logic. This port is optional, because you can select an internal GTX transceiver clock at generation time to perform this function.
TXN[n-1:0], TXP[n-1:0]	OUT	Transmit differential pairs for each of the n GTX transceivers used.
RXN[n-1:0], RXP[n-1:0]	IN	Receive differential pairs for each of the n GTX transceivers used.
MGTREFCLK_P[m-1:0], MGTREFCLK_N[m-1:0]	IN	GTX transceiver reference clocks used. ***Note:*** The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports, because some GTX transceivers can share clock inputs.

Performance and Resource Utilization

Table 2: **Configuration Details**

Configuration	Device	IBERT Setup
Config1	XC6VLX240T-3FF1156	1 serial transceiver with line rate set to 12.5 Gb/s
Config2	XC6VLX240T-3FF1156	8 serial transceivers with line rate set to 12.5 Gb/s
Config3	XC6VLX240T-3FF1156	28 serial transceivers with line rate set to 12.5 Gb/s

Restrictions

Only one IBERT core can be generated for a device, and the IBERT core will constitute the entire design. The IBERT core cannot be merged in with user logic.

Verification

Xilinx has verified the IBERT core in a proprietary test environment, using an internally developed bus functional model.

References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/documentation.
- For more information about the Virtex-6 FPGA GTX transceiver, see the *Virtex-6 FPGA GTX Transceiver User Guide*, located at http://www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

The IBERT core is provided under the ISE Design Suite End-User License Agreement and can be generated using the Xilinx CORE Generator system 13.3 or higher. The CORE Generator system is shipped with Xilinx ISE Design Suite development software.

Please contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Definition
CPRI	Common Packet Radio Interface
DFE	Decision Feedback Equalizer
DRP	Dynamic Reconfiguration Port
FF	Flip-Flop
FPGA	Field Programmable Gate Array
IBERT	Integrated Bit Error Ratio Tester
I/O	Input/Output
ILA	Integrated Logic Analyzer
ISE	Integrated Software Environment
JTAG	Joint Test Action Group
LUT	Lookup Table
MMCM	Mixed-Mode Clock Manager
MHz	Mega Hertz
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
PMA	Physical Medium Attachment
PRBS	Pseudorandom binary sequence
RAM	Random Access Memory
RX	Receive
TX	Transmit
XAUI	eXtended Attachment Unit Interface

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
05/24/2009	1.0	Release 10.1 (Initial Xilinx release).
10/19/2011	2.0	• Updated to support XIlinx ISE v13.3 tools and sofware • Added section for generating the IBERT core • Replaced IP Facts table with updated template • Updated Notice of Disclaimer and Copyright statement

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