ChipScope PLB IBA (Bus Analyzer) (v. 1.01a)

DS283 April 7, 2009 **Product Specification**

Introduction

The ChipScope™ PLB IBA core is a specialized Bus Analyzer core designed to debug embedded systems that contain the IBM CoreConnect Processor Local Bus (PLB). The ChipScope PLB IBA core in EDK is based on Tcl script that generates a HDL wrapper to the PLB IBA and calls the ChipScope Core Generator to generate the netlist based on user parameters.

Features

- Multiple Match Units for Trigger and Data capture
- Each Match Unit can be enabled and configured independently
- The Match Units for the PLB IBA are:
  - PLB Control signals
  - PLB Address Units
  - PLB Read Data Unit
  - PLB Write Data Units
  - PLB Master Units (based on no. of masters)
  - PLB Slave Units (based on no. of slaves)
- Generic Trigger/Data Unit with selectable width
- For more information refer to the ChipScope Pro Software and Cores User Guide in the ChipScope installation

For more information about the PLB IBA core, refer to the *ChipScope Pro Software and Cores User Guide*.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex®-4	
Version of Core	chipscope_plb_iba	v1.01a
Resources Used		
	Min	Max
Slices	219	411
LUTs	87	112
FFs	215	320
Block RAMs	1	187
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL/EDIF	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.1 or later	
Verification	ChipScope Pro 11.1 or later	
Simulation	Not Supported in Simulation	

Functional Description

The ChipScope OPB IBA core is a specialized Bus Analyzer core designed to debug embedded systems containing the IBM CoreConnect On-Chip Processor Local Bus (PLB). The modules and interconnects are shown in Figure 1.

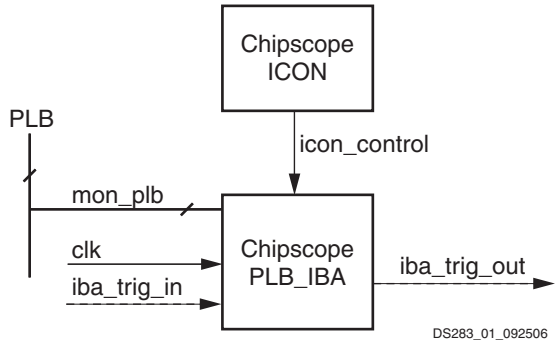

Figure 1: **ChipScope PLB IBA Block Diagram**

ChipScope PLB IBA I/O Signals

The I/O signals for the ChipScope PLB IBA are listed and described in Table 1.

Table 1: **ChipScope PLB IBA I/O Signals**

Signal Name	Match Unit	Interface	I/O	Description
chipscope_icon_control	N/A	N/A	I[35:0]	ICON Control signals
iba_trig_in	GENERIC	N/A	I	Generic Trigger Inputs
iba_trig_out	GENERIC	N/A	O	IBA Trigger Output
PLB_Clk	CONTROL	MON_PLB	I	PLB Clock
PLB_Rst	CONTROL	MON_PLB	I	PLB Reset
PLB_Abort	CONTROL	MON_PLB	I	PLB abort bus request indicator
PLB_BE	CONTROL	MON_PLB	I	PLB Byte Enable
PLB_BusLock	CONTROL	MON_PLB	I	PLB Bus Lock
PLB_MasterID	CONTROL	MON_PLB	I	PLB Current Master Identifier
PLB_MSize	CONTROL	MON_PLB	I	PLB data bus port width indicator
PLB_PAValid	CONTROL	MON_PLB	I	PLB primary address valid indicator
PLB_SAValid	CONTROL	MON_PLB	I	PLB secondary address valid indicator
PLB_RdPrim	CONTROL	MON_PLB	I	PLB secondary to primary read request indicator
PLB_WrPrim	CONTROL	MON_PLB		PLB secondary to primary write request indicator
PLB_RNW	CONTROL	MON_PLB	I	PLB read not write
PLB_Size	CONTROL	MON_PLB	I	PLB transfer size
PLB_ABus	ADDR	MON_PLB	I	PLB address bus
PLB_WrDBus	WRDATA	MON_PLB	I	PLB write data bus

Table 1: **ChipScope PLB IBA I/O Signals *(Cont'd)***

Signal Name	Match Unit	Interface	I/O	Description
Sl_RdDBus	RDDATA	MON_PLB	I	PLB read data bus
PLB_MAddrAck	MASTER<n>	MON_PLB	I	PLB master n address acknowledge
PLB_MBusy	MASTER<n>	MON_PLB	I	PLB master n slave busy indicator
PLB_MErr	MASTER<n>	MON_PLB	I	PLB master n slave error indicator
PLB_MRdDAck	MASTER<n>	MON_PLB	I	PLB master n read data acknowledge
PLB_MRdWdAddr	MASTER<n>	MON_PLB	I	PLB master n read word address
PLB_MRearbitrate	MASTER<n>	MON_PLB	I	PLB master n bus rearbitrate indicator
PLB_MSsize	MASTER<n>	MON_PLB	I	PLB master n slave data bus port width
PLB_MWrDAck	MASTER<n>	MON_PLB	I	PLB master n write data acknowledge
M_Abort	MASTER<n>	MON_PLB	I	Master n abort bus request indicator
M_BE	MASTER<n>	MON_PLB	I	Master n byte enables
M_BusLock	MASTER<n>	MON_PLB	I	Master n bus lock
M_MSize	MASTER<n>	MON_PLB	I	Master n data bus port width
M_Priority	MASTER<n>	MON_PLB	I	Master n bus request priority
M_Request	MASTER<n>	MON_PLB	I	Master n bus request
M_RNW	MASTER<n>	MON_PLB	I	Master n read not write
M_Size	MASTER<n>	MON_PLB	I	Master n transfer size
Sl_AddrAck	SLAVE<n>	MON_PLB		Slave address acknowledge
Sl_RdDAck	SLAVE<n>	MON_PLB		Slave read data acknowledge
Sl_RdWdAddr	SLAVE<n>	MON_PLB		Slave read word address
Sl_Rearbitrate	SLAVE<n>	MON_PLB		Slave rearbitrate bus indicator
Sl_SSize	SLAVE<n>	MON_PLB		Slave data bus port size indicator
Sl_Wait	SLAVE<n>	MON_PLB		Slave wait indicator
Sl_WrComp	SLAVE<n>	MON_PLB		Slave write transfer complete indicator
Sl_WrDAck	SLAVE<n>	MON_PLB		Slave write data acknowledge

ChipScope PLB IBA Parameters

To create a ChipScope PLB IBA uniquely tailored for your system and to optimize performance, specific features can be parameterized on the PLB IBA. Table 2 describes the features that can be parameterized. For a detailed description of the PLB IBA core, see the *ChipScope Pro Software and Cores User Guide* in the ChipScope installation.

The ChipScope PLB IBA peripheral supports multiple trigger units that connect to the PLB Control bus, Address bus, Data bus, individual Slave or Master buses and a generic trigger input. Each one of these trigger units can be enabled and parametrized independently. In the following table, C_<XYZ>_UNIT refers to any one of these units and the parameters associated with the unit. The table also lists all the trigger units and the parameter names used to enable each of them.

Table 2: **ChipScope PLB IBA Parameters**

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Number of Data Samples captured for every trigger match	C_NUM_DATA_SAMPLES	Integer (512*, 1024, 2048, 4096, 8192, 16384, 32768**, 65536**, 131072**) * except Virtex-5 ** Virtex-5	512 (1024 for Virtex-5)	integer
Enable the Trigger out signal iba_trig_out which will be asserted when IBA gets triggered	C_ENABLE_TRIGGER_OUT	Integer 1 = Enable Trigger out 0 = Disable Trigger out	1	integer
Target Family	C_FAMILY	Xilinx FPGA families	virtex4	strings
Disable RPM placement information in netlist	C_DISABLE_RPM	Integer 1 = RPM disable 0 = RPM enabled in netlist	0	integer
Disable SRL16 usage	C_DISABLE_SRL16S	Integer 1 = Disable 0 = Enable	0	Integer
Trigger on Rising or Falling edge of clock	C_RISING_CLOCK_EDGE	Integer (1 = Rising, 0 = Falling)	1	Integer
Enable Trigger Sequencer in the ILA	C_ENABLE_TRIGGER_SEQUENCER	Integer 1 = Enable 0 = Disable	1	Integer
Maximum number of Sequencer levels	C_MAX_SEQUENCER_LEVELS	Integer (1-16)	16	Integer
Enable Storage Qualification for ILA	C_ENABLE_STORAGE_QUALIFICATION	Integer 1 = Enable 0 = Disable	1	Integer
Number of Match Units enabled for <XYZ> Unit Ex : PLB Control Signals	C_<XYZ>_UNITS Ex : C_CONTROL_UNITS	Integer (0-16) 0 = Disable Unit 1-16 = Number of Match Units	0	integer
Counter Width for Match Unit <XYZ> Ex : PLB Control signals Match Unit	C_<XYZ>_UNIT_COUNTER_WIDTH Ex : C_CONTROL_UNIT_COUNTER_WIDTH	Integer (0-32) 0 - Disable Match Counter 1-32 - Match Counter Width(1)	0	integer
Match Tyoe for Match Unit <XYZ> Ex : PLB Control signals Match Unit	C_<XYZ>_UNIT_MATCH_TYPE Ex : C_CONTROL_UNIT_MATCH_TYPE	"basic", "basic with edges", "extended", "extended with edges", "range", "range with edges"(1)	"basic"(2)	string
PLB Control Unit	C_CONTROL_UNITS	Integer (0-16)	1	integer
PLB Address Unit	C_ADDR_UNITS	Integer (0-16)	1	integer
Generic Trigger Unit	C_GENERIC_TRIGGER_UNITS	Integer (0-16)	0	integer
Generic Trigger Input Width	C_GENERIC_TRIGGER_IN_WIDTH	Integer (allowable range 1-1024 when Generic Trigger Units are enabled)	0 (defaults to 8 when enabled)	integer

Table 2: **ChipScope PLB IBA Parameters *(Cont'd)***

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
PLB Write Data Unit	C_WRDATA_UNITS	Integer (0-16)	0	integer
PLB Read Data Unit	C_RDDATA_UNITS	Integer (0-16)	0	integer
PLB Master (0-16) Unit	C_MASTER<n>_UNITS	Integer (0-16)	0	integer
PLB Slave (0-16) Unit	C_SLAVE<n>_UNITS	Integer (0-16)	0	integer

1. Refer to the *ChipScope Pro Software and Cores User Guide*, in the ChipScope installation
2. CONTROL : basic with edges; ADDR, TRIGGER: extended with edges

Allowable Parameter Combinations

- The parameter C_GENERIC_TRIGGER_IN_WIDTH is valid only when the generic trigger input signal (not PLB-bus related) is enabled on the ChipScope PLB IBA by specifying the C_GENERIC_TRGGER_UNITS to be 1 or higher.
- Parameters C_<XYZ>_UNIT_COUNTER_WIDTH and C_<XYZ>_UNIT_MATCH_TYPE are valid only when the corresponding trigger unit is enabled by setting C_<XYZ>_UNITS to be 1 or higher.
- The Master and Slave trigger units that can be enabled using C_MASTER<n>_UNITS and C_SLAVE<n>_UNITS is determined by the number of master or slave PLB peripherals in the user's processor design. <n> refers to the position of a peripheral on the PLB bus (this is usually the same as the order in the user's MHS design).

For more information, refer to the *ChipScope Pro Software and Cores User Guide*, in the ChipScope installation.

Parameter - Port Dependencies

Table 3: **ChipScope PLB IBA Parameter - Port dependencies**

Port Name	Parameter dependency	Description
iba_trig_in	C_GENERIC_TRIGGER_UNITS C_GENERIC_TRIGGER_IN_WIDTH	The generic trigger input port and its width is determined by these two
iba_trig_out	C_ENABLE_TRIGGER_OUT	The trig_out port is enabled when this parameter is set to 1

Design Implementation

Design Tools

The ChipScope PLB IBA design consists mainly of a Tcl script. When the EDK platgen tool is run, this Tcl script gets called and the script internally calls the ChipScope Pro Core Generator tool in commandline mode and provides it an arguments file (.arg) to generate the ChipScope PLB IBA netlist. The Tcl script also generates a HDL wrapper to match the IBA ports based on the core parameters.

XST is the synthesis tool used for synthesizing the wrapper HDL generated for the ChipScope PLB IBA. The EDIF netlist outputs from XST and ChipScope Core Generator are then input to the Xilinx Foundation tool suite for actual device implementation.

Target Technology

The intended target technology is all Xilinx FPGAs.

Device Utilization and Performance Benchmarks

The device utilization varies widely based on the parameter combinations set by the user.

Restrictions

Maximum number of signals that can be monitored with a single IBA is 256 signals.

References

- More information on the ChipScope Pro software and cores is available in the *Software and Cores User Guide*, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studdio 11.1 online help, located at http://www.xilinx.com/documentation.
- Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the *Xilinx System Generator for DSP User Guide*, located at http://www.xilinx.com/documentation.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY.*

Ordering Information

The PLB IBA core is provided under the ISE Design Suite End-User License Agreement and can be generated using the Xilinx Embedded Development Kit (EDK) system 11.1 or higher. EDK is shipped with the Xilinx ISE Design Suite development software.

Revision History

Date	Version	Revision
01/16/2004	1.0	Release 6.1i (Initial Xilinx release).
08/30/2004	1.1	Release 6.3i.
10/31/2005	3.0	Release 8.1i.
09/25/2006	4.0	Release 9.1i.
12/10/2007	4.1	Release 9.2i.
04/25/2008	5.0	Release 10.1.
07/28/2008	5.1	Release 10.1, Service Pack 2 changes.
04/07/2009	6.0	Release 11.1.

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