

Summary

This CPRI™ Gateway Proof of Concept (PoC) platform demonstrates the features and techniques being discussed within the wireless industry and standards bodies for the Cloud-RAN (C-RAN) fronthaul architecture (IEEE P1914.1 (NGFI), IEEE P1914.3 (ROE) and 3GPP (RAN)).

To address the various standards and trends, Xilinx has produced a generic solution of a CPRI Gateway (CGW) to demonstrate a functional fronthaul solution that can form the basis of CGW designs and which can be used to test, modify and innovate customer solutions. The Xilinx® CGW contains the Vivado® IP and proof-of-concept source code, that can be modified and updated as standards evolve or for customers to differentiate their own solution. The Xilinx CGW has been demonstrated using Xilinx 7 series (28 nm) devices. The solution is now being ported and targeted for the newly released Zynq® UltraScale+™ (16 nm) architecture. This solution is based on the Zynq UltraScale+ ZCU102 development board.

Features

- Zynq UltraScale+ on the ZCU102 development board
- 10G Ethernet interface to Baseband (eNodeB/BBU)
- One CPRI interface link (2.45 Gb/s) to the radio side, with capability of adding additional links
- Timing and synchronization using either:
 - IEEE1588v2 (CGW as 1588 slave)
 - Free-running (non-1588 with CGW as master and baseband aligning to CGW Ethernet TX packets)
- SyncE receive clock recovery
- L1 offload
 - Downlink: Ethernet Payload decompression, IFFT, and Cyclic Prefix insertion
 - Uplink: Cyclic Prefix removal, Half Carrier shift, FFT, RACH, Ethernet Payload Compression
- The PoC uses NGFI style frame format
- 10 MHz LTE Bandwidth
- 2 antenna (default), 1 antenna (programmable)
- Test mode (to allow the CGW to be demonstrated without connection to additional equipment:
 - In this mode the CGW generates uplink packets with test payloads and is connected using Ethernet and CPRI optical loopbacks.
- The CGW is running PetaLinux and linuxptp (1588 daemon).

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Applications

The CPRI Gateway PoC design is targeted at wireless fronthaul systems and experimental testbeds for 5G wireless investigations and uses an architecture that is scalable for use with different network capacities and frame formats. A typical application is shown in [Figure 1](#).

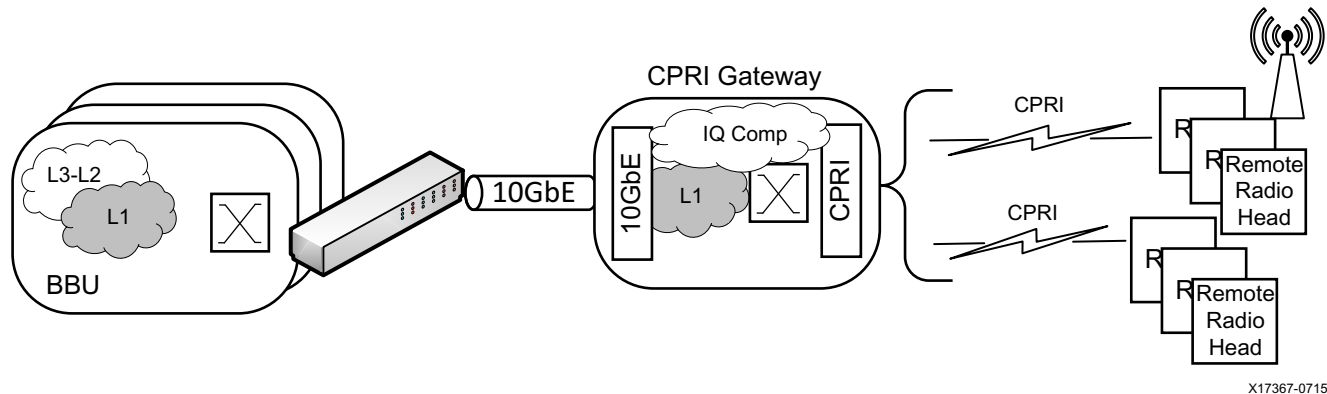
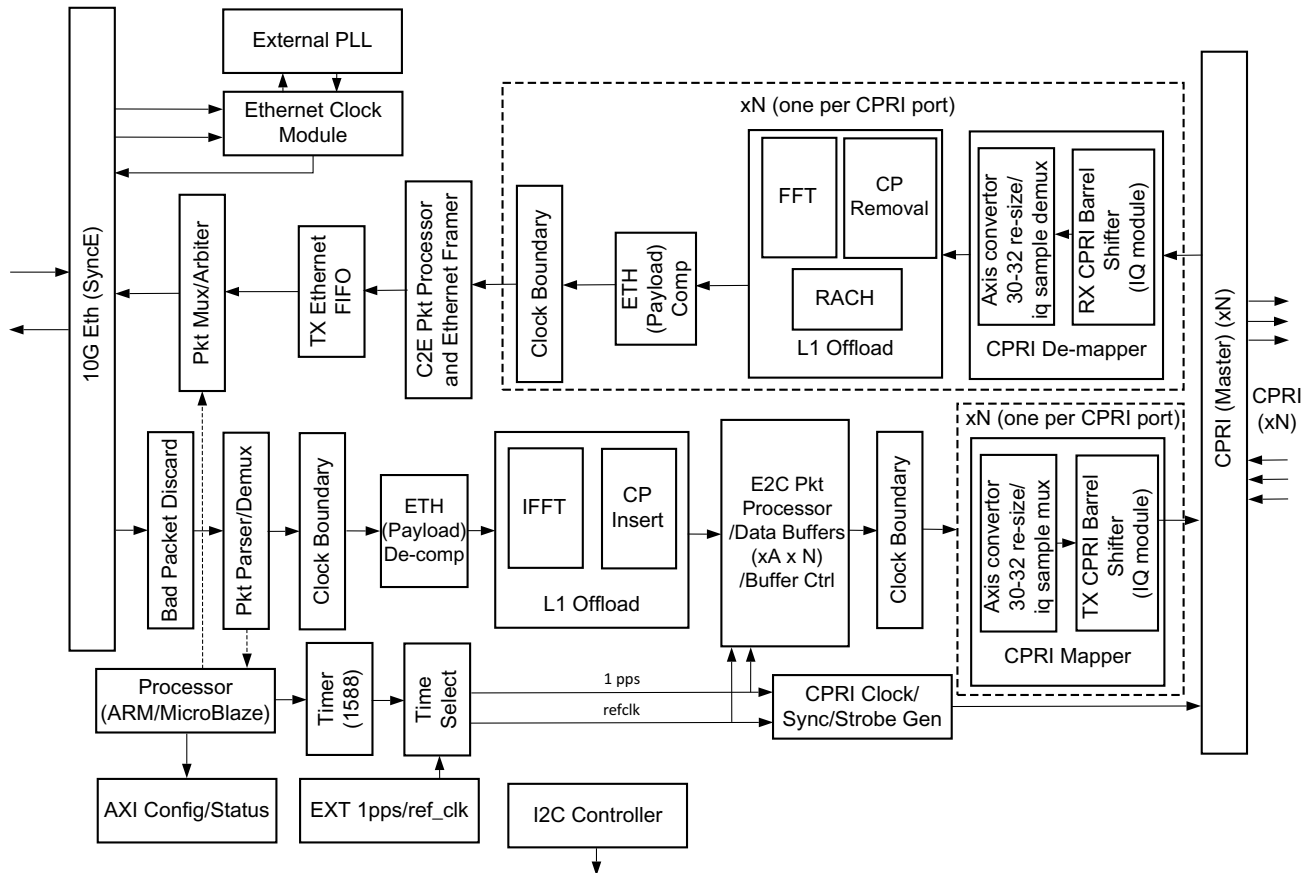


Figure 1: CPRI Gateway in a C-RAN Wireless System

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Architecture

The CPRI Gateway PoC is designed to allow complete flexibility in Radio-over-Ethernet frame format, with a programmable frame demultiplexer on the Ethernet ingress interface and a generic packet processor block operating in both CPRI-to-Ethernet and Ethernet-to-CPRI directions. Additional blocks provide frequency and timing synchronization to a variety of sources.



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Figure 2: Xilinx CPRI Gateway PoC Architecture

Hardware Demonstration

- The data path integrity can be demonstrated using the CPRI Gateway in test mode using optical loopbacks on the Ethernet and CPRI ports (see Figure 3).
- 1588 timing and synchronization can be demonstrated by connecting to customer equipment (an IEEE1588 master clock) and using an oscilloscope to monitor 1 pps outputs.
- Simultaneous datapath and 1588 operation might require a 10G switch or a timing master design (available from Xilinx) when connecting to customer equipment.

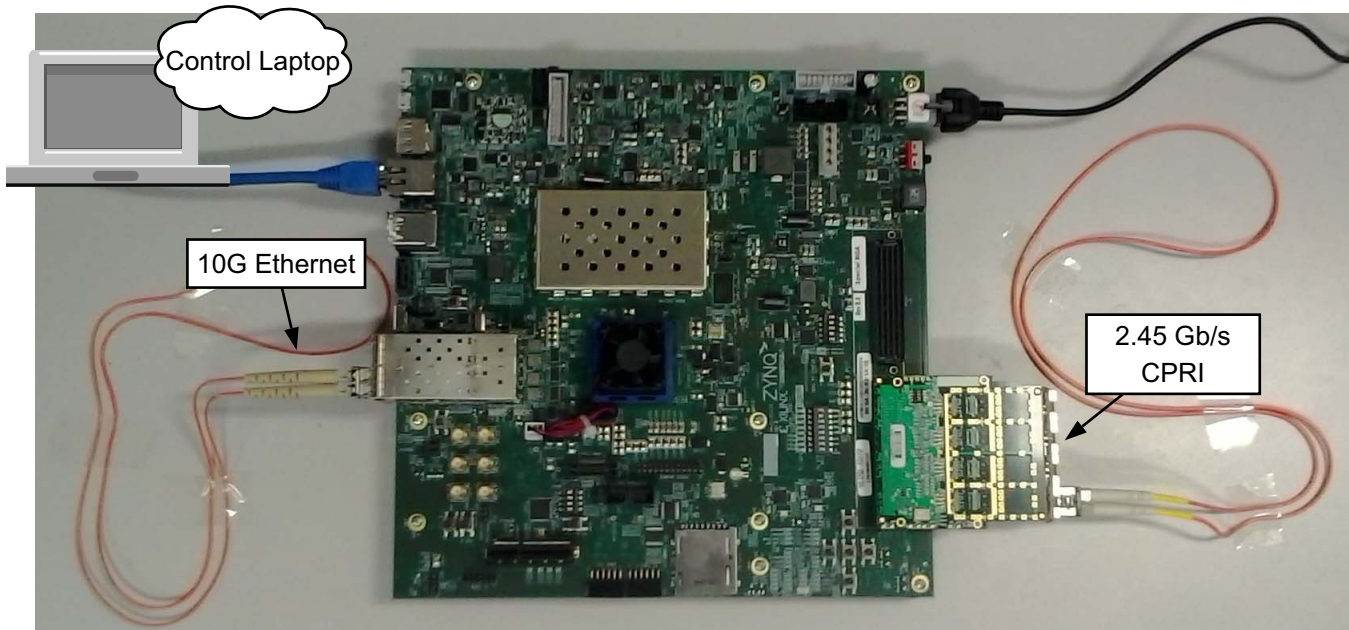


Figure 3: CPRI Gateway Hardware Demonstration

Deliverables

- Demonstration Deliverables: Black Box CGW for Customer Demo:
 - A BOOT.BIN file which can be run from an SD Card, for Xilinx Zynq UltraScale+ ZCU102 based CGW design
 - A GUI to run on a PC to view the CGW operating status registers
 - User Guide (step by step instructions on how to use demo)
- Evaluation Deliverables: CGW for Customer Demo, Evaluation, Modification And Innovation
 - Same deliverables as in the Black Box CGW plus:
 - Vivado Project containing CGW Design under NDA
 - User Guide (how to use the Vivado Project)
 - Simplified Architecture Guide
- Design Services for Further Customer Defined Requirements
 - Under NRE, NDA and MOU:
 - Customer defined deliverable and agreed timeline

Hardware Required (Black Box CGW Example)

- ZCU102
- FMS14 or FMS18
- 2 x SFP+ (10G - Avago AFBR-709ASMZ or equivalent)
- 2 x optical cables
- 1x USB mini (UART) + 1 x USB micro (JTAG)
- RJ45 cable
- SD Card
- PC (customer provided)

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
07/29/2016	1.0	Initial Xilinx release.

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