

Features

- Drop-in module for Virtex™, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-4, Spartan™-II, Spartan-III, and Spartan-3 FPGAs
- Generates ROMs, single/dual-port RAMs, and SRL16-based RAMs
- Supports data widths ranging from 1 to 1024 bits
- Supports depths ranging from 16 to 65,536 words for Virtex-II, Virtex-II Pro and Spartan-3 FPGAs, and ranging from 16 to 4096 words for all other FPGAs
- Optional registered output with variable pipelining
- Uses relationally placed macro (RPM) mapping and placement technology, for maximum and predictable performance
- Incorporates Xilinx Smart-IP™ technology for utmost parameterization and optimum implementation
- For use with v6.2i or higher of the Xilinx CORE Generator™ system

Functional Description

The distributed memory module is used to create memory structures using the Select-RAM. It can be used to create read-only memory (ROM), single-port random-access memory (RAM), pseudo dual-port RAM and SRL16-based RAM with data widths up to 1024 bits and depths up to 65536 words. Options are available for simple registering of inputs and outputs in addition to variable pipelining capabilities. Optional asynchronous and synchronous resets are available for the output registers. Optionally, the module can be generated as a relationally placed macro (RPM) or as unplaced logic.

For timing information, please see the Xilinx product specification for the specific architecture being targeted.

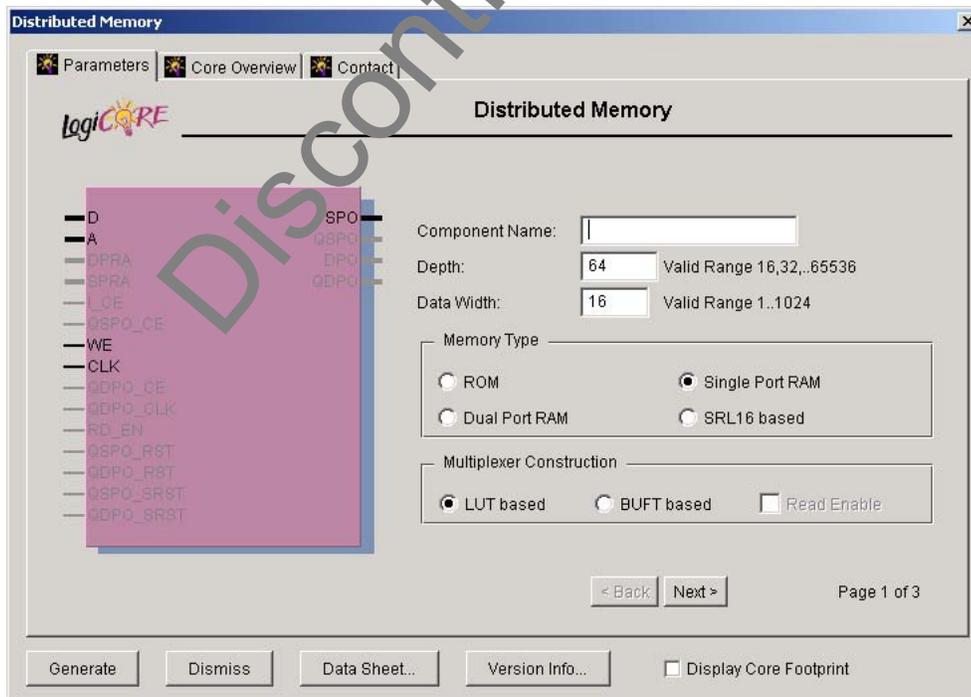


Figure 1: Distributed Memory Parameterization Screen 1

CORE Generator Parameters

The CORE Generator parameterization screens for this module are shown in [Figure 1](#), [Figure 2](#), and [Figure 3](#).

The parameters for Screen 1 are:

- **Component Name:** The component name is used as the base name of the output files generated for this module. Names must begin with a letter and must be composed from the following characters: a to z, 0 to 9 and “_”.
- **Depth:** Enter the required memory depth. The valid range is 16 to 65536 in steps of 16. The default value is 64. Note that the maximum depth is reduced to 4096 for all but the Virtex-II, Virtex-II Pro and Spartan-3 FPGAs.
- **Data Width:** Enter the width of the memory. The valid range is 1 to 1024. The default value is 16.
- **Memory Type:** Select the appropriate radio button for the types of memory required. The default setting is **Single-Port RAM**.
 - **ROM:** A schematic diagram showing the structure of the ROM modules is shown in [Figure 8](#). The address register is optional (controlled by the setting of the **Input Options** parameter). Output registering and pipelining are also optional (controlled by the setting of the **Output Options** parameter). The CLK is not required if no registers are present. The resets and clock enables are optional.
 - **Single-Port RAM:** A schematic diagram showing the structure of the single-port RAM modules is shown in [Figure 10](#). The address and data registers are optional (controlled by the setting of the **Input Options** parameter). Output registering and pipelining are also optional (controlled by the setting of the **Output Options** parameter). The resets and clock enables are optional.
 - **Dual-Port RAM:** A schematic diagram showing the structure of the dual-port RAM modules is shown in [Figure 11](#). The address and data registers are optional (controlled by the setting of the **Input Options** parameter). The dual-port read address register is optional (controlled by the setting of the **Dual-Port Address** parameter). Output registering and pipelining for both output ports are also optional (controlled by the setting of the **Output Options** parameter). When registered outputs are selected, the two output ports can be clocked by the same or different clock signals and can have the same or different clock enables (based on the settings chosen for the **Common Output Clock** and **Common Output CE** parameters). All resets and clock enables are optional.
 - **SRL16-based RAM:** A schematic diagram showing the structure of the SRL16-based ram module is shown in [Figure 9](#). The address and data registers are optional (controlled by the setting of the **Input Options** parameter). Output registering and pipelining are also optional (controlled by the setting of the **Output Options** parameter). The resets and clock enables are optional.
 - **Note:** The dual-port RAM implementations are based on using the Select RAM feature of the LUTs. In this mode, the LUTs behave as a pseudo dual-port memory. For details of the fundamental operation, refer to the Xilinx Product Specification for the specific architecture being targeted.
- **Multiplexer Construction:** For modules that use multiple memory primitives to create the required depth, multiplexing is required in the output paths. This can be performed with multiplexers built using look up tables (LUTs) or using the tristate buffer primitives (BUFTs). The BUFT option is not available with Spartan-3 implementations. If the multiplexer is constructed using BUFTs, the

output of the module cannot be registered, although a maximum of one pipeline stage is optionally available. The default setting is **LUT-Based**.

- **Read Enable:** This optional read-enable pin is available only when BUFT-based multiplexers are used.

The parameters for Screen 2 are:

- **Input Options:** Select the appropriate radio button for the types of inputs required. The action of setting this parameter to **Registered** will have different effects depending on the **Memory Type** selection:
 - **ROM:** An address register will be generated.
 - **Single-Port RAM, Dual-Port and SRL16-based RAM:** A register on the A[N:0] address input, a data input register and a WE register will be generated.

The default setting is **Non registered**.
- **Input Clock Enable:** This optional input is available when **Input Options** are set to **Registered** and **Memory Type** is not a **ROM**.
- **Qualify WE with I_CE:** This parameter is valid only for single-port RAM, dual-port RAM, and SRL16-based RAM with **Input Options** set to **Registered** and **Input Clock Enable** checked. When the checkbox is not checked, the WE register has no clock-enable control. When checked, the WE register has a clock enable that is driven by the I_CE input.

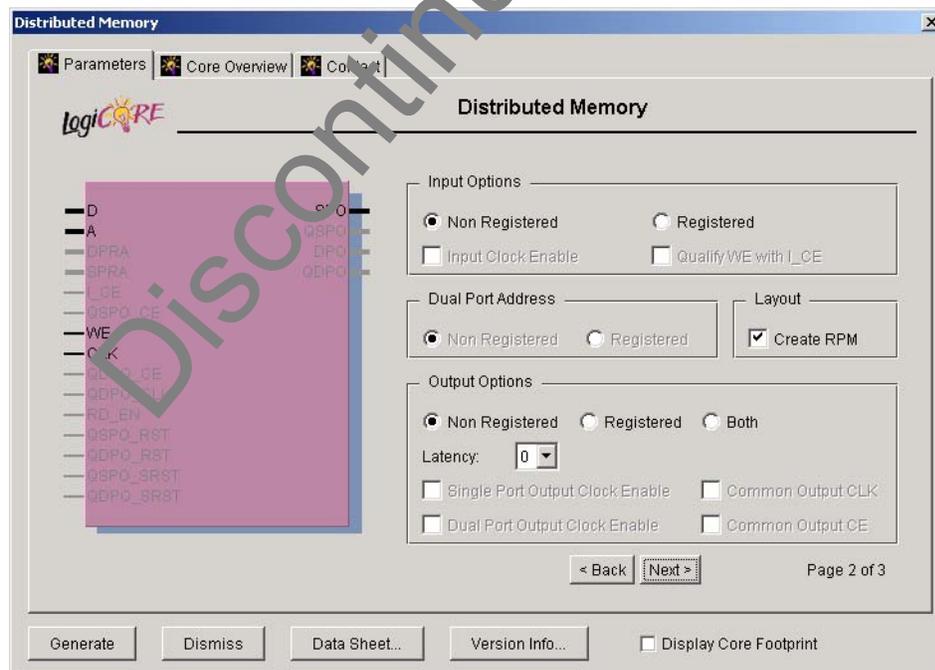


Figure 2: Distributed Memory Parameterized Screen 2

- **Output Options:** Select the appropriate radio button for the types of outputs required. The default setting is **Non registered**.
 - **Single Port Output Clock Enable:** This check box is enabled for registered output memory or for input registered ROM to provide this optional pin.
 - **Dual Port Output Clock Enable:** This checkbox is enabled only for output registered dual-port RAMs to provide this optional pin.
 - **Common Output Clock:** This checkbox is enabled only for registered dual-port RAMs. If not checked, the SPO registers will be clocked by the CLK input and the DPO registers will be clocked from the QDPO_CLK input. The default is checked, where all output registers are clocked from the CLK input.
 - **Common Output CE:** This checkbox is enabled only for registered dual-port RAMs and only if **Common Output Clock** and **Dual Port Output Clock Enable** is also checked. If **Common Output CE** is not checked, the SPO register clocks will be enabled by the QSPO_CE input and the DPO register clocks will be enabled from the QDPO_CE input. The default is checked, where all output register clocks are enabled by the QSPO_CE input.
 - **Latency:** This drop down box displays latency selections available for the current memory core with chosen parameters. Latency defines the amount of clock cycles between the address chosen, and the data stored at this address being output on the (registered) single port output; latency takes into account input and output registers and any additional pipelining. The default is to the minimum amount of pipelining.
- **Dual-Port Address:** This parameter is valid only for dual-port RAMs. It controls the presence or absence of a register on the DPRA[N:0] inputs. The default setting is **Non registered**.
- **Create RPM:** When this box is checked, the module will be generated with relative location attributes attached. The resulting placement of the module will be in a column with two bits per slice. The default setting is to create an RPM.

The parameters for Screen 3 are:

- **Initial Contents...:** The initial values of the memory elements can be set with the use of a Coefficients file (COE), by loading the ".coe" file using the **Load Coefficients...** button. The initial contents can be viewed by selecting the **Show Coefficients...** button. For a description of the COE file, refer to the section titled, "Specifying Memory Contents using a COE file." The contents of the COE file are converted to a memory initialization file (MIF) with the values in a binary format. This file describes the true memory contents that are used by the core and the simulation models. For a description of the memory initialization file, refer to the section entitled, "MIF File description."
 - **Default Data:** Enter the initial value to be stored in any memory location not specified by another means. When no value is entered, this field defaults to 0. Values can be entered in binary, decimal or hex format, as defined by the **Default Data Radix** entry.
 - **Default Data Radix:** Choose the radix of the **Default Data** value. Valid entries are 2, 10 and 16.
- **Reset Options**
 - **Reset QSPO:** This checkbox is enabled only when the core has a registered single-port output. If checked, an asynchronous single-port output reset pin will be available.
 - **Reset QDPO:** This checkbox is enabled only when the core has a registered dual-port output. If checked, an asynchronous dual-port output reset pin will be available.

- **Synchronous Reset QSPO:** This checkbox is enabled only when the core has a registered single-port output. If checked, a synchronous single-port output reset pin will be available.
- **Synchronous Reset QDPO:** This checkbox is enabled only when the core has a registered dual-port output. If checked, a synchronous dual-port output reset pin will be available.
- **CE Overrides Sync Controls:** This checkbox is enabled only when one of the synchronous reset options has been selected and an output clock enable has been selected. It forces the synchronous control signals to be disabled by the clock enable pin.
- **Sync Controls Overrides CE:** This checkbox is enabled only when one of the synchronous reset options has been selected and an output clock enable has been selected. It forces the synchronous control signals to override the state of the output clock enable signals.

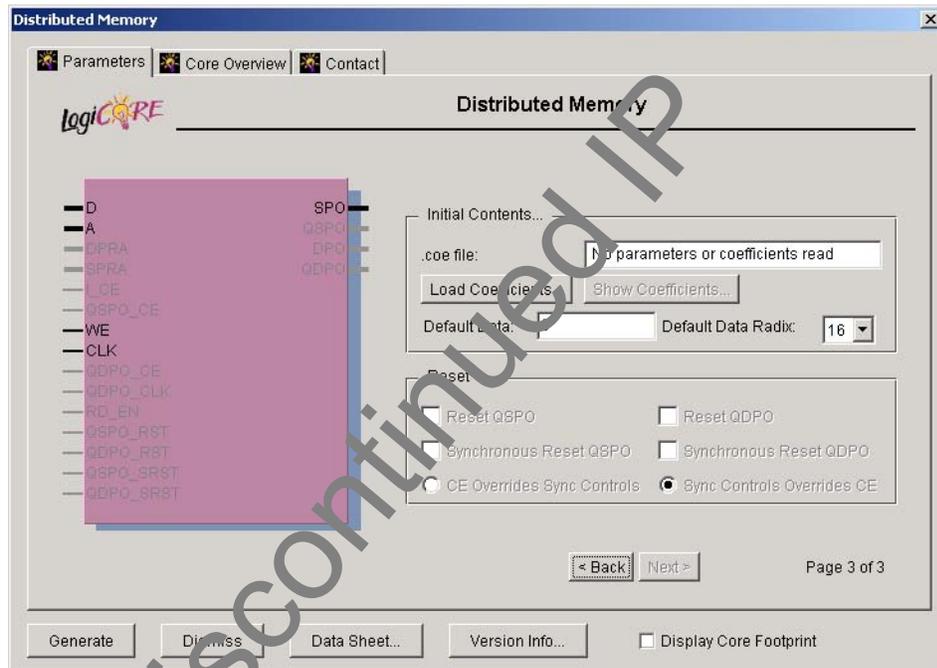


Figure 3: Distributed Memory Parameterization Screen 3

Pinout

Signal names are described in [Table 1](#) and are shown in [Figure 4](#), [Figure 5](#), [Figure 6](#), and [Figure 7](#).

Table 1: Core Signal Pinout

Name	Direction	Description
D[P:0]	Input	Data input to be written into the memory for single-port, dual-port and SRL16-based RAMs.
A[N:0]	Input	Address inputs. Only address input for ROMs and single-port RAMs. On SRL16-based RAMs, it defines the most significant bits (4 and up) of the memory locations written to. On dual-port memories, it defines memory location written to and memory location read out on the SPO[P:0] outputs.
SPRA[N:0]	Input	Single-Port Read Address. Port is present only on SRL16-based RAMs and defines memory location read out on the SPO[P:0] outputs.
DPRA[N:0]	Input	Dual-Port Read Address. Port is present only on dual-port RAMs and defines memory location read out on the DPO[P:0] outputs.
SPO[P:0]	Output	Non registered single-port output bus. Non registered data output bus for ROMs, single-port and SRL16-based RAMs. One of two non registered output buses on dual-port RAMs.
QSPO[P:0]	Output	Registered single-port output bus. Registered data output bus for ROMs, single-port and SRL16-based RAMs. One of two registered output buses on dual-port RAMs.
DPO[P:0]	Output	Non registered dual-port output bus, One of the non registered data output buses for dual-port RAMs. Data stored at the address location specified by DPRA[N:0] appears at this port.
QDPO[P:0]	Output	Registered dual-port output bus. One of two registered output buses on dual-port RAMs.
CLK	Input	Write clock and register clock for ROMs, single-port and SRL16-based RAMs. On dual-port RAMs signal is the write clock and register clock for single-port input and output registers.
QDPO_CLK	Input	On dual-port RAMs, signal is the write clock and register clock for dual-port RAM input and output registers
WE	Input	Write Enable
I_CE	Input	Input Clock Enable. Signal is present for RAMs which have registered inputs. The clock enable controls input data register, address register and WE register.
RD_EN	Input	Read Enable
QSPO_CE	Input	On ROMs, clock enable controls all input and output registers. On dual-port memories, controls output register and pipeline registers in QSPO path.

Table 1: Core Signal Pinout (Continued)

Name	Direction	Description
QDPO_CE	Input	Present only on dual-port RAMs. Controls output register and pipeline registers in QDPO path.
QSPO_RST	Input	Single-port registered output asynchronous reset.
QDPO_RST	Input	Available only on dual-port RAMs. Dual-port registered output asynchronous reset.
QSPO_SRST	Input	Single-port registered output synchronous reset
QDPO_SRST	Input	Available only on dual-port RAMs. Dual-port registered output synchronous reset

Note: All control inputs are active high. If an active low input is required for a particular control pin, an inverter must be placed in the path to the pin. The inverter is absorbed appropriately during mapping.

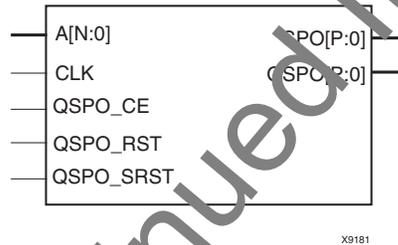


Figure 4: Core Schematic Symbol for ROMs

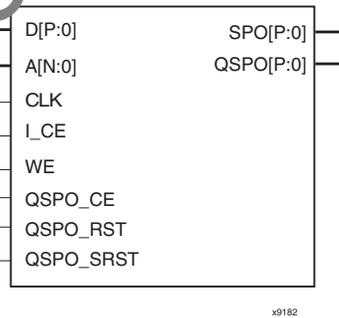


Figure 5: Core Schematic Symbol for Single Port RAM

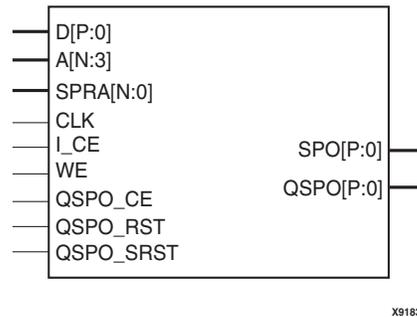


Figure 6: Core Schematic Symbol for SRL 16-based RAM

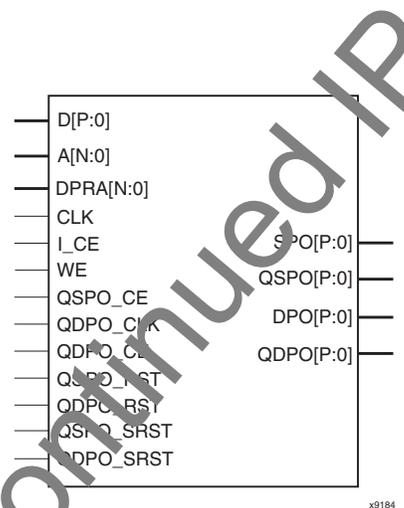


Figure 7: Core Schematic Symbol for Dual-Port RAMs

Specify Memory Contents Using a COE File

The initial contents of the memory can be defined using a text file known as a Coefficient (COE) File. COE files must have a “.coe” extension.

The COE file consists of two parameters similar to an XCO file, but the end of each line is determined with the use of a semicolon. The two parameters are:

- memory_initialization_vector:** Each row of memory elements are defined with a binary, decimal or hexadecimal number having equivalent binary value that represents whether an individual memory element along the width of the row is set to a ‘1’ or a ‘0’. Each row of memory initialization is separated by a comma or whitespace, up to the depth of the memory. Negative values are not allowed.
- memory_initialization_radix:** The radix of the initialization value is specified here, with the choices being 2, 10, or 16.

An example of a COE file is shown below:

```

; Sample Initialization file for a 16x32 RAM-based
; shift register
    
```

```
memory_initialization_radix = 16;
memory_initialization_vector = 23f4 0721 11ff ABel
0001 1 0A 0
23f4 0721 11ff ABel 0001 1 0A 0
23f4 721 11ff ABel 0001 1 A 0
23f4 721 11ff ABel 0001 1 A 0;
```

MIF File Description

The COE file provides a wrapper to allow the user to initialize memory contents. However, the MIF file holds the actual binary data that is used to initialize the memory in the core and simulation models. The MIF file consists of one line of text per memory location, the first line in the file corresponding to address 0, the second line corresponding to address 1, and so on. The text on each line must be the initialization value (MSB first) for the corresponding memory address in binary format, with exactly one binary digit per bit of the memory's width.

Parameter Values in the XCO File

Names of XCO file parameters and their parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case insensitive.

Table 2 shows the XCO file parameters and values, as well as summarizing the GUI defaults. The following is an example of the CSET parameters in an XCO file:

```
CSET component_name = abc123
CSET depth = 64
CSET data_width = 16
CSET memory_type = Single_Port_RAM
CSET multiplexer_construction = LUT_based
CSET read_enable = FALSE
CSET input_options = Non_Registered
CSET input_clock_enable = FALSE
CSET qualify_we_with_i_ce = FALSE
CSET dual_port_address = Non_Registered
CSET output_options = Non_Registered
CSET single_port_output_clock_enable = FALSE
CSET dual_port_output_clock_enable = FALSE
CSET latency = 0
CSET common_output_clk = FALSE
CSET common_output_ce = FALSE
CSET create_rpm = TRUE
CSET coefficient_file = a.coe
CSET default_data = 0
CSET default_data_radix = 16
CSET reset_qspo = FALSE
CSET reset_qdpo = FALSE
CSET sync_reset_qspo = FALSE
CSET sync_reset_qdpo = FALSE
CSET ce_overrides = sync_controls_overrides_ce
```

Table 2: XCO File Values and Default Values

Parameter	XCO File Values	Default GUI Setting
component_name	ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _	blank
depth	Integer in the range 16 to 65536 in steps of 16	64
data_width	Integer in the range 1 to 1024	16
memory_type	One of the following keywords: rom, single_port_ram, dual_port_ram, srl16_based	single_port_ram
multiplexer_construction	One of the following keywords: lut_based or buft_based	lut_based
read_enable	One of the following keywords: true, false	false
input_options	One of the following keywords: non_registered, registered	non_registered
input_clock_enable	One of the following keywords: true, false	false, true when input_options registered
qualify_we_with_i_ce	One of the following keywords: true, false	false
dual_port_address	One of the following keywords: non_registered, registered	non_registered
output_options	One of the following keywords: non_registered, registered, both	non_registered
single_port_output_clock_enable	One of the following keywords: true, false	false, true when output_options registered or both
dual_port_output_clock_enable	One of the following keywords: true, false	false, true when output_options registered or both
latency	Integer in the range of the possible values (displayed on GUI)	minimum latency value
common_output_clk	One of the following keywords: true, false	false
common_output_ce	One of the following keywords: true, false	false
create_rpm	One of the following keywords: true, false	true
coefficient_file	ASCII text starting with a letter and based upon the following character set: a...z, 0...9 and _, and must end with a ".coe" extension	blank
default_data	Numeric value in the radix specified by the default_data_radix keyword whose value does not exceed $2^{\text{DATA_WIDTH} - 1}$	0
default_data_radix	One of the following keywords: 2, 10, 16	16
reset_qspo	One of the following keywords: true, false	false
reset_qdpo	One of the following keywords: true, false	false

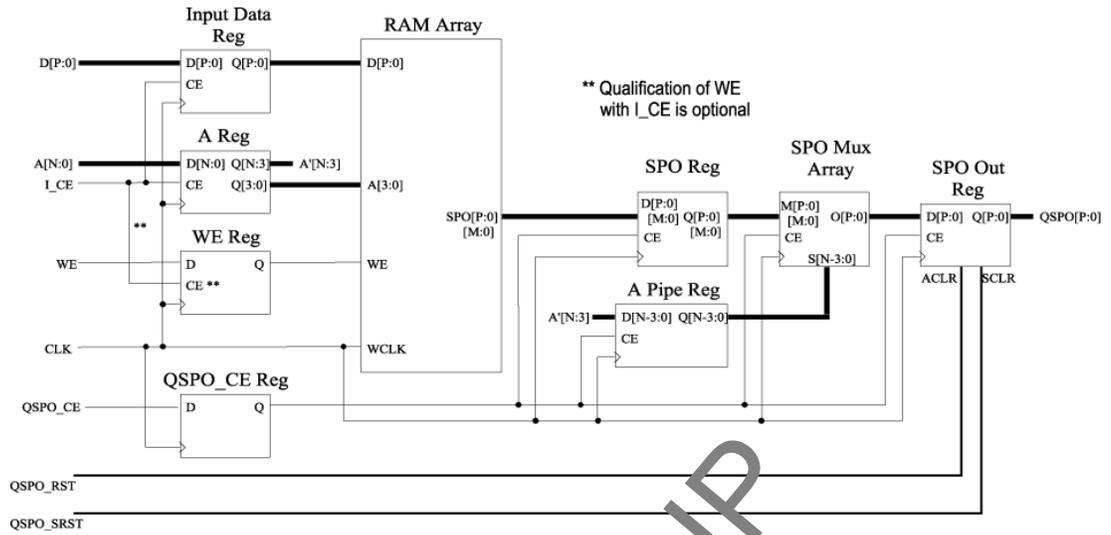


Figure 10: Schematic of a Single-Port RAM Module

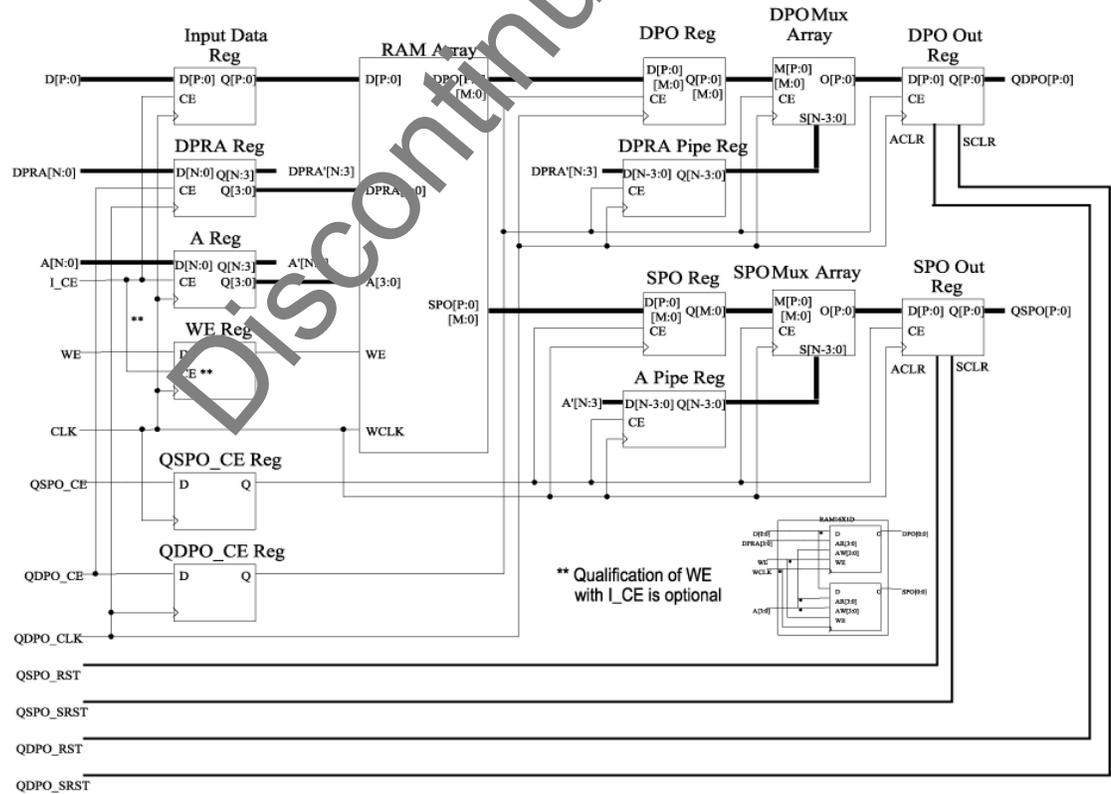


Figure 11: Schematic of a Dual-Port RAM Module

Core Resource Utilization

When designing distributed memories, the LUTs in the slices are used either as memory primitives or to construct multiplexers. The registers available in these slices are used for output registering and/or pipelining.

When input registering is requested, extra registers are required, one flip-flop per control bit (WE, QSPO_CE and QDPO_CE) and one flip-flop per bit of data and address (D[P:0], A[N:0] and DPRA[N:0]).

If both input registering and output registering are requested, extra registers are required to implement the A Pipe Register and (for dual-port RAMs only) the DPRA Pipe Register. This requires one additional flip-flop per bit of A[N:0] and (on dual-port RAMs only) DPRA[N:0].

For an accurate measure of the usage of primitives, slices, and CLBs for a particular point solution, check the Display Core Viewer after Generation checkbox in the CORE Generator GUI.

Ordering Information

This core may be downloaded from the Xilinx [IP Center](#) for use with the Xilinx CORE Generator system v7.1i and higher. The Xilinx CORE Generator system is bundled with Foundation Series Development software packages, at no additional charge.

To order Xilinx software, please visit the [Xilinx Xpresso Cafe](#) or contact your local Xilinx [sales representative](#).

Information on additional Xilinx LogiCORE modules is available on the Xilinx [IP Center](#).

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/13/02	1.0	Initial Xilinx release.
12/11/03	1.1	Updated document to support v7.0 of the core.
04/03/04	1.2	Updated document to support v7.1 of the core.
01/18/05	1.3	Deleted the blank timing diagram section (on page 10) from the document.
04/28/05	1.4	Updated the document to confirm to the current Xilinx data sheet template.