3GPP Downlink Chip Rate v1.0

XMP001 August 8, 2007 **Product Brief**

Introduction

The 3GPP Downlink Chip Rate core provides a Release 6 Compliant, Xilinx FPGA optimized solution for Femto-cell, Pico-cell and Macro-cell solutions.

Features

- Available for Virtex-4, Virtex-5, Spartan-3A DSP FPGAs
- Supports all FDD channels
  - Slot formatting
  - Scrambling, Spreading and Weighting
  - System timing (T_{CELL}, T_{DPCH}, etc.)
  - Multiple Sectors
  - Pilot generation
  - Pilot, TFCI, TPC symbol insertion
  - STTD Encoding
  - Fully Flexible architecture
- Fully optimized for speed and area
- Fully synchronous design with independent interface clocks
- For use with the Xilinx CORE Generator™ v 9.2i and higher

Functional Description

The 3GPP Downlink Chip Rate core provides a complete solution for Femto-cell, Pico-cell, and Macro-cell architectures. The architecture has been designed to provide efficient use of the FPGA while also offering a low bandwidth interface to an external DSP or processor to reduce system-level overhead. Timing critical operations are performed by the FPGA which also simplifies the software solution. See Figure 1.

This core provides the Physical Layer 1 slot formatting and chip rate processing functions. This includes the generation of the Pilots and STTD encoding which can often be a processor intensive function. The core also provides programmable System Timing where Sub-Slot based interrupts can be configured by an external DSP allowing logical Channel grouping to be made based on Channel Offset values.

All parameters and data are doubled buffered where necessary and internally synchronized to Slot or Frame boundaries as required by the System.

The interface to the core is OCP compatible and can be easily attached to any bus-based system. This allows multiple cores to be inferred, or alternatively multiple processors can be supported. The memory mapped interface allows for simple integration and validation within the system.

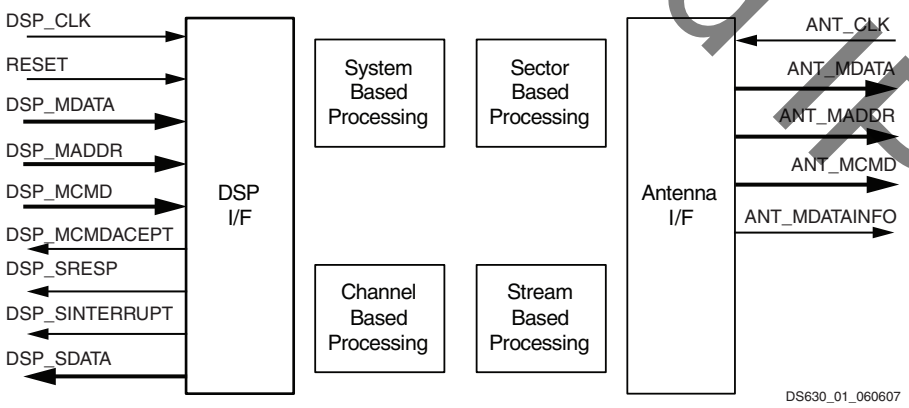

Figure 1: **Downlink Chip Rate Core**

Ordering Information

This Xilinx LogiCORE™ module is provided under the SignOnce IP Site License. A free evaluation version of the module is available.

Once purchased, the core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator v9.2i and higher. The Xilinx CORE Generator is bundled with the ISE™ Foundation software at no additional charge.

Contact your local Xilinx sales representative for pricing and availability on Xilinx LogiCORE modules and software. Information on additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release.