# Dual-Port Block Memory Core v6.3

## Features

- Drop-in module for Virtex™, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-4, Spartan™-II, Spartan-IIE, Spartan-3, and Spartan-3E FPGAs

- Supports all Virtex-II write mode options: Read-After-Write, Read-Before-Write, and No-Read-On-Write (Available only for Virtex-II, Spartan-3, and Spartan-3E implementations)

- Supports data widths from 1 to 256 bits

- Supports memory depths from 2 to 1M words depending on architecture selected

- Supports ROM functions, enabling simultaneous read operations from the same location

- Supports RAM functions, enabling simultaneous write operations to separate locations and simultaneous read operations from the same location

- Ports are independent of each other

- Supports asymmetric A and B port configurations

- Supports cores designed for area optimization or using a single SelectRAM+™ or SelectRAM™-II primitive

- Supports different pin polarities for control signals: clock, enable, write enable and output initialization pins

- Incorporates Xilinx Smart-IP™ technology for utmost parameterization and optimum implementation

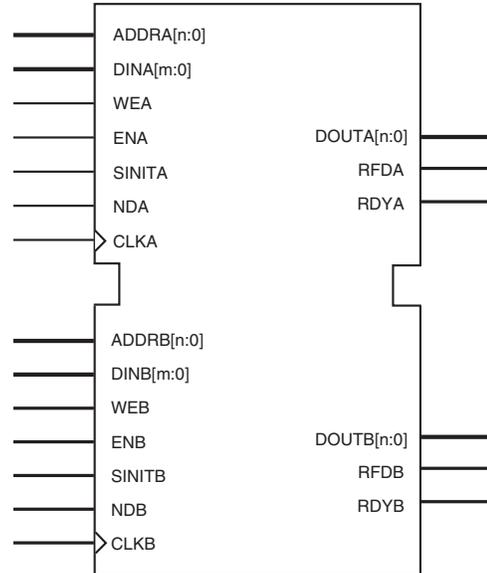- Available in the Xilinx CORE Generator™ system v7.1i SP4 and higher



*Figure 1:* **Core Schematic Symbol**

## Functional Description

The Dual-Port Block Memory module for Spartan-II and Virtex is composed of single or multiple 4 Kb blocks called Select-RAM+. The Dual-Port Block Memory module for Virtex-II, Virtex-II Pro, Virtex-4, and Spartan-3, on the other hand, is composed of single or multiple Virtex-II 18 Kb blocks (SelectRAM-II) enabling deeper and/or wider memory implementations. Both the SelectRAM+ and SelectRAM-II memories are True Dual-Port™ RAM, offering fast, discrete, and large blocks of memory in the Spartan-II and Virtex device families. Since Spartan-II and Virtex both use the 4 Kb SelectRAM+ blocks, any particular reference to a Virtex implementation also applies to a Spartan-II, Virtex-E, or Spartan-IIE implementation. Similarly, since Virtex-II, Virtex-II Pro, Virtex-4, and Spartan-3, use the 18 Kb SelectRAM-II blocks, any particular reference to a Virtex-II implementation also applies to a Virtex-II Pro, Virtex-4, or Spartan-3 implementation.

A memory module has two independent ports that enable shared access to a single memory space and are generated based on user-defined width and depth. Both ports are functionally identical, with each port providing read and write access to the memory. Simultaneous reads from the same memory location may occur, but all other simultaneous, reading-from, and writing-to the same memory location result in correct data being written into the memory, but invalid data being read.

The memory's Port A and Port B are configured to support user-defined data input and address widths. When both ports are disabled (ENA and ENB inactive) the memory contents and output ports remain unaltered. When either port is enabled (ENA or ENB asserted) all memory operations occur on the active edge of the clock input.

During a write operation (WEA or WEB asserted), the data presented at the port's data input is stored in memory at the location selected by the port's address input. During this operation, the data output port behaves differently for the Virtex and Virtex-II architectures.

The data output port of the Virtex-II implementation is dependent on one of three write mode options. Each of the options determines the behavior of the corresponding data output port when a write operation occurs.

The Virtex implementation supports a single write mode option: Read-After-Write, which causes the data being written to the addressed memory location to be transferred to the data output port when a write operation occurs.

During a read operation, the memory contents at the location selected by the address will appear at the module's output. When Synchronous Initialization (SINITA or SINITB) is active, the module's registered outputs are synchronously reset to zero for Virtex and to a user-defined value for Virtex-II. The Synchronous Initialization command has no effect on the contents of the memory or write operations. The enable, write enable, and synchronous initialization can also be specified as active high or active low.

## Pinout

Port names for the core module are shown in Figure 1 and defined in Table 1. The inclusion of some ports on the module is optional; exclusion of these ports will alter the function of the module. The optional ports are marked in Table 1 and described in more detail below.

### Clock - CLK[AIB]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the active edge of their corresponding CLK pin. The data bus has a clock-to-out time referenced to the CLK pin.

By default, the block memory operates synchronously to the rising edge of the clock. Users, however, have the option to perform all memory operations on the rising or the falling edge of the clock. Performing the memory operation on the falling edge of the clock will not use any extra resources.

*Table 1:* **Core Signal Pinout**

| Name | Direction | Description |
|------|-----------|-------------|
| DIN[A\|B]<n:0> (Optional) | Input | **Data Input**: Data to be written into memory via Port [A\|B]. |
| ADDR[A\|B]<m:0> | Input | **Address**: The memory location to which data will be written or read via Port [A\|B]. |
| WE[A\|B] (Optional) | Input | **Write Enable**: Control signal used to allow transfer of input data into memory via Port [A\|B]. |
| EN[A\|B] (Optional) | Input | **Enable**: Control signal used to enable memory accesses via read and write operations from Port [A\|B]. |
| SINIT[A\|B] (Optional) | Input | **Synchronous Initialization**: Control signal used to force the module's outputs to a predefined state. |
| CLK[A\|B] | Input | **Clock**: Clock input, all memory access is synchronous with the clock input. |
| ND[A\|B] (Optional) | Input | **New Data Port A**: Indicates that there is a new and valid address on Port ADDR[A\|B] (Active High). |
| DOUT[A\|B]<n:0> (Optional) | Output | **Data Output**: Synchronous output of memory. |
| RFD[A\|B] (Optional) | Output | **Ready for Data**: Indicates that the memory is ready to accept new data (Active High). |
| RDY[A\|B] (Optional) | Output | **Output Ready**: Indicates valid data on port DOUT [A\|B] (Active High). |

## Enable - EN[A\|B]

The enable pin affects the read, write, and SINIT functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory locations.

By default, the enable pin is active high. Users, however, have the option to configure the enable pin active high or active low. Configuring the enable pin active low will not use extra resources.

## Write Enable - WE[A\|B]

Activating the write enable pin allows the port to write to the memory locations. When active, the contents of the DIN bus is written to memory at the address pointed to by the ADDR bus. The output latches are loaded or not loaded according to the write configuration (write first, read first, no change). When inactive, a read operation occurs, and the contents of the memory locations referenced by the address bus reflect on the DOUT bus, regardless of the write mode selected.

By default, the write enable pin is active high. Users, however, have the option to configure the write enable pin active high or active low. Configuring the write enable pin active low will not use extra resources.

### Synchronous Initialization - SINIT[AIB]

The SINIT pin forces the data output ports to a SINIT value. For the Virtex implementation, the SINIT value is zero, and for the Virtex-II implementation the SINIT value is user-defined. The data output ports are each synchronously asserted to their respective SINIT value. This operation does not affect memory locations and does not disturb write operations on the other port. If the core is configured with an enable pin, the SINIT function is active only when the enable port is active.

By default the SINIT pin is active high. Users, however, have the option to configure the SINIT pin active high or active low. Configuring the write enable pin active low will not use extra resources.

### Address Bus - ADDR[AIB]<m:0>

The address bus selects the memory location that will be accessed during a read or write operation.

### Data-In Bus - DIN[AIB]<n:0>

The DIN buses provide the new data value to be written into the memory. Data input and output signals are always busses; that is, in a 1-bit width configuration, the data input signal is DIN[0] and the data output signal is DOUT[0].

### Data-Out Bus - DOUT[AIB]<n:0>

The DOUT buses reflect the contents of memory locations referenced by the address bus during a read operation.

During a write operation of a Virtex memory (write first configuration), the DOUT buses reflect the DIN buses.

During a write operation of a Virtex-II memory (write first or read first configuration), the DOUT buses reflect either the DIN buses or the stored value before write. During a write operation of a Virtex-II memory in no change mode, DOUT buses are not affected.

### New Data - ND[AIB]

ND indicates that there is a new and valid address on ADDR[A|B] port. It affects only the RDY port.

### Ready for Data - RFD[AIB]

RFD indicates that the memory is ready to accept new data. RFD[A|B] is always true, except when EN[A|B] is inactive.

### Output Ready (valid) - RDY[AIB]

Indicates valid output on port DOUT[A|B] relative to when ND is asserted. RDY[A|B] will lag ND[A|B] by the latency of

the block memory

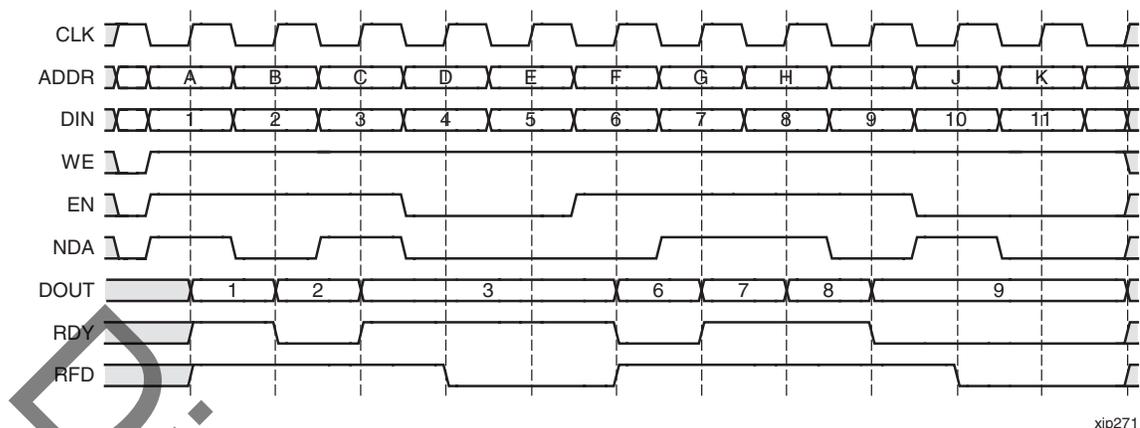Figure 2 shows the operation of the ND, RFD, and RDY handshaking signals.

*Figure 2:* **Handshaking Signals Operation (Write-First Mode)**

# CORE Generator Parameters

The main screen of the CORE Generator GUI includes the following parameter options:

- **Component Name**: Enter a name, up to 256 characters, for the output files generated for this module.

- **Port A Memory Size**

  - **Width A**: Select the data bit width. The width can be between 1 and 256.

  - **Depth A**: Select the number of words in memory. The value range is 2 to 1,048,576 (1M) depending on the architecture selected. Available depths will vary depending on the width entered for Port A; the absolute maximum number of words is 256K for the Virtex architecture and 1M for the Virtex-II architecture. Cores should not exceed the number of Block RAM primitives in the targeted device.

- **Port B Memory Size**

  - **Width B**: Select the data bit width. Available widths will vary depending on the width entered for port A. For the Virtex architecture, the available widths could be 1, 2, 4, 8 and 16 times larger than the width entered for port A. The available widths for the Virtex-II architecture could be 1, 2, 4, 8,16 and 32 times larger than the width entered for port A.

  - **Depth B**: Reports the depth of Port B. This value is calculated such that Port A and Port B have the same memory size. For the Virtex architecture, the depth could be 1, 2, 4, 8 and 16 times smaller than the depth entered for port A. The depth for the Virtex-II architecture could be 1, 2, 4, 8,16 and 32 times smaller than the depth entered for port A. The minimum depth for Port B is 2.

- **Port A Options**

  - **Configuration**

    · **Read and Write**: Configures Port A to have DINA and DOUTA ports allowing read and write access to the memory.

    · **Write Only**: Configures Port A to have a DINA port enabling this port to be used only for write access. Note that only one port can be configured to be Write Only.

    · **Read Only:** Configures Port A to have a DOUTA port enabling this port to be used for read only access.

- **Write Mode**: Select one for Virtex-II architecture. The default is Read-After-Write. The Virtex architecture supports only Read-After-Write.

- **Read-after-Write**: (Virtex-II, Virtex)

  · (1) No Inputs or Outputs Registered: The input data is transferred onto the DOUTA port on the active clock edge immediately following the assertion of the WEA input.

  · (2) With Inputs Registered Only: The input data is transferred onto the DOUTA port on the second active clock edge immediately following the assertion of the WEA input.

  · (3) With Outputs Registered Only: The input data is transferred onto the DOUTA port on the second active clock edge immediately following the assertion of the WEA input.

  · (4) With Inputs and Outputs Registered: The input data is transferred onto the DOUTA port on the third active clock edge immediately following the assertion of the WEA input.

- **Read-before-Write**: (Virtex-II Only)

  · No Inputs or Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the active clock edge immediately following the assertion of the WEA input.

  · With Inputs Registered Only: The current data in the addressed memory location is transferred onto the DOUTA port on the second active clock edge immediately following the assertion of the WEA input.

  · With Outputs Registered Only: The current data in the addressed memory location is transferred onto the DOUTA port on the second active clock edge immediately following the assertion of the WEA input.

  · With Inputs and Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTA port on the third active clock edge immediately following the assertion of the WEA input.

- **No-Read-on-Write**: (Virtex-II Only)

  · A read operation is not performed when WEA is asserted. The DOUTA port will contain the contents of the last read memory location.

- **Port B Options**

  - **Configuration**

    · **Read and Write**: Configures Port B to have DINB and DOUTB ports allowing read and write access to the memory.

    · **Write Only**: Configures Port B to have a DINB port enabling this port to be used only for write access. Note that only one port can be configured to be Write Only.

    · **Read Only**: Configures Port B to have a DOUTB port enabling this port to be used only for read access.

  - **Write Mode**: Select one for Virtex-II architecture. The default is Read-After-Write. The Virtex architecture supports only Read-After-Write.

  - **Read-after-Write**

    · No Inputs or Outputs Registered: The input data is transferred onto the DOUTB port on the active clock edge immediately following the assertion of the WEB input.

· With Inputs Registered Only: The input data is transferred onto the DOUTB port on the second active clock edge immediately following the assertion of the WEB input.

· With Outputs Registered: The input data is transferred onto the DOUTB port on the second active clock edge immediately following the assertion of the WEB input.

· With Inputs and Outputs Registered: The input data is transferred onto the DOUTB port on the third active clock edge immediately following the assertion of the WEB input.

- **Read-before-Write**

· No Inputs or Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the active clock edge immediately following the assertion of the WEB input.

· With Inputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the second active clock edge immediately following the assertion of the WEB input.

· With Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the second active clock edge immediately following the assertion of the WEB input.

· With Inputs and Outputs Registered: The current data in the addressed memory location is transferred onto the DOUTB port on the third active clock edge immediately following the assertion of the WEB input.

- **No-Read-on-Write**

· A read operation is not performed when WEB is asserted. The DOUTB port will contain the contents of the last read memory location.

The second screen of the CORE Generator GUI includes the following parameter selections:

• **Port A Design Options**

- **Optional Pins**

· **Enable Pin**: Check the box to include the enable ENA port on the module; uncheck the box to remove it.

· **Handshaking Pins**: Check the box to include the following ports; uncheck the box to remove them.

· **ND** [New Data]: Signals a new and valid memory address whenever active. This port has no effect on the memory read and write operations. ND is valid only when RFD is active.

· **RFD** [Ready For Data]: Indicates that the memory can accept new addresses. Always active when the memory is enabled.

· **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid. RDY will lag ND by the latency of the module.

- **Register Options**

· **Register Inputs**: Select to register ports DIN, ADDR, and WE before accessing block memory. See Figure 5.

- **Output Register Options**

· **Additional Output Pipe Stages**: Select "1" to enable an additional register on the output of the memory; select "0" to disable an additional register on the output of the memory. See Figure 5.

- **SINIT Pin**: Check box to add the synchronous port SINIT to the memory.

- The Virtex-4 architecture RAMB16 primitive contains embedded output registers. These registers can improve timing for high speed designs. In this core, the embedded registers will only be used when the memory is 1 primitive deep and the SINIT pin is not used. If either the SINIT pin is used or the memory is more than one primitive deep, these embedded registers will not be used. Instead, registers in the slice fabric will be used.

- **Pin Polarity**: Lets the user configure the polarities of the Port A control signals if the signals exist.

- **Active Clock Edge**: Select whether the memory operation occurs on the rising edge or falling edge of the clock.

- **Enable Pin:** Select whether the enable pin is active high or active low.

- **Write Enable Pin:** Select whether the write enable pin in active high or active low.

- **Initialization Pin:** Select whether the initialization pin is active high or active low.

The third screen of the CORE Generator includes the following parameter selections:

- **Port B Design Options**

  - **Optional Pins**

    - **Enable Pin:** Check the box to include the enable ENB port on the module; uncheck the box to remove it.

    - **Handshaking Pins:** Check the box to include the following ports; uncheck the box to remove them.

    - **ND** [New Data]: Signals a new and valid memory address whenever active. This port has no effect on the memory read and write operations. ND is valid only when RFD is active.

    - **RFD** [Ready For Data]: Indicates that the memory can accept new addresses. Always active when the memory is enabled.

    - **RDY** [Output is Ready]: Indicates to the user that the data on the output is valid. RDY will lag ND by the latency of the module.

  - **Register Options**

  - **Register Inputs**: Select to register ports DIN, ADDR, and WE before accessing block memory. See Figure 5.

  - **Output Register Options**

    - **Additional Output Pipe Stages**: Select "1" to enable an additional register on the output of the memory; select "0" to disable an additional register on the output of the memory. See Figure 5.

    - **SINIT Pin**: Check box to add the synchronous port SINIT to the memory.

    - The Virtex-4 architecture RAMB16 primitive contains embedded output registers. These registers can improve timing for high speed designs. In this core, the embedded registers will only be used when the memory is 1 primitive deep and the SINIT pin is not used. If either the SINIT pin is used or the memory is more than one primitive deep, these embedded registers will not be used. Instead, registers in the slice fabric will be used.

  - **Pin Polarity**: Lets the user configure the polarities of the Port B control signals if the signals exist.

    - **Active Clock Edge**: Select whether the memory operation occurs on the rising edge or falling edge of the clock.

- · **Enable Pin**: Select whether the enable pin is active high or active low.

- · **Write Enable Pin**: Select whether the write enable pin in active high or active low.

- · **Initialization Pin**: Select whether the initialization pin is active high or active low.

- **Primitive selection**: Determines whether the core is optimized for area or created using a single 4 Kb SelectRAM+ or 16 Kb SelectRAM-II block or primitive.

  - **Select primitive**: Choose a block or primitive to create the core.

    - · The primitives for the Virtex architecture are: 4kx1, 2kx2, 1kx4, 512x8 and 256x16.

    - · The primitives for the Virtex-II architecture are: 16kx1, 8kx2, 4kx4, 2kx9, 1kx18, and 512x36.

    - · The primitives for the Virtex-4 architecture are: 32kx1, 16kx1, 8kx2, 4kx4, 2kx9, 1kx18, and 512 x 36.

The fourth screen of the CORE Generator GUI includes the following parameter selections:

- **Simulation Model Options**: Deselect to enable warning messages in the simulation model. The default value is to disable warning messages in the simulation model.

- **Initial Contents**: Enter the parameter fields related to the data stored in the memory directly after device configuration. Note that these initial data must conform to the chosen Port A parameter fields.

  - · **Global Init Value**: Enter the value to be stored in any memory location not specified by another means. When no values are entered, this field defaults to 0. Value must be in Hex. This value must be smaller than Port A's largest word.

  - · **Load Init File**: Select if the initial contents of the memory are to be read from a *coe* file.

  - · **Load File**: Click to activate a browser window that lets the user select a coefficient or *coe* file containing the initial contents of the memory. (This is an ASCII file with a ".coe" extension.) For further information regarding the memory's initial contents, refer to the *Specifying Memory Contents* section.

- **Information Panel**: Lists the resulting configuration of the core.

  - **Address Width A**: Displays the number of address bits required for Port A for this configuration.

  - **Address Width B**: Displays the number of address bits required for Port B for this configuration.

  - **Blocks Used**: Displays the number of BlockRAM primitives needed to implement this configuration. It is recommended to verify that the required number of blocks does not exceed those available in the targeted device.

  - **Port A Read Pipeline Latency**: Displays the total latency of Port A from the point when a new address is presented to the memory to when it becomes a valid output. The total latency will be increased by one if the inputs are registered or if an additional output register is added. A latency of 1 is defined as follows: the read address is read in on the active edge of the clock and the resulting output is seen following that same active edge of the clock.

  - **Port B Read Pipeline Latency**: Displays the total latency of Port B from the point when a new address is presented to the memory to when it becomes a valid output. The total latency will be increased by one if the inputs are registered or if an additional output register is added. A latency of 1 is defined as follows: the read address is read in on the active edge of the clock and the resulting output is seen following that same active edge of the clock.
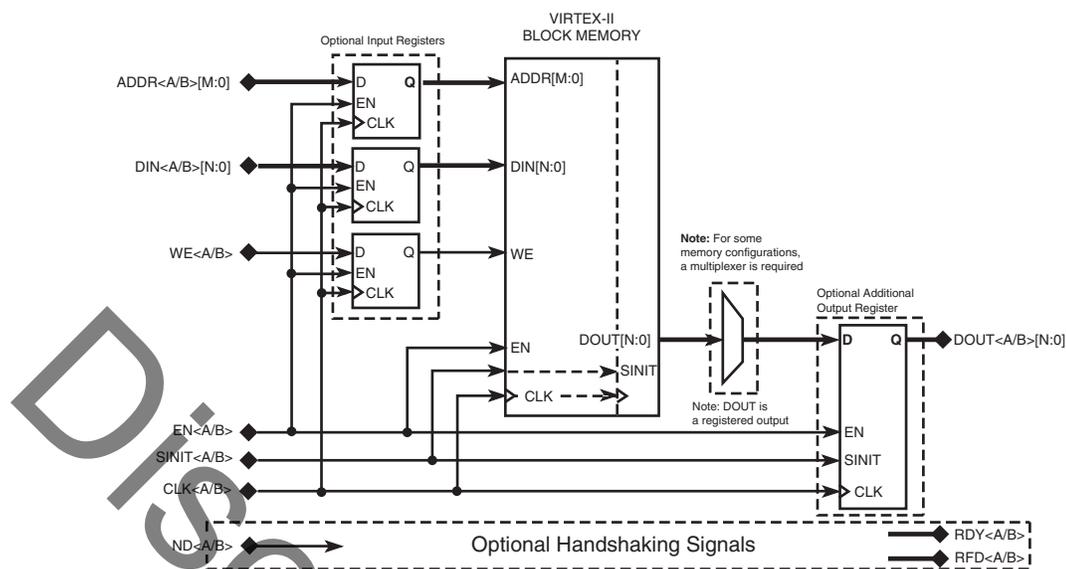
*Figure 3:* **Dual-Port Memory Block Diagram**

## Operating Modes

The Virtex-II block SelectRAM-II can maximize the utilization of the True Dual-Port memory at each clock edge by supporting three different write modes. Each port's write mode is independently configurable. The Read-Before-Write mode offers the flexibility of using the data output bus during a write operation on the same port. Output port behavior is determined by the configuration. This choice increases the effective bandwidth of the Block Memory. Note that the Virtex SelectRAM+ supports only the Read-After-Write mode.

### Read Operations

Read operations are synchronous to the rising edge of the clock. The data in the memory location selected by the address appears on the DOUT port after the active edge of the clock.

### Write Operations

Write operations are synchronous to the active edge of the clock. The data on the DIN port is written into the memory location selected by the address on the active edge of the clock when WE is active. The user can configure the memory in one of three ways to determine the behavior of the DOUT port during a write cycle. Each port's write mode is independently configurable. Note that the following timing diagrams and descriptions of the write modes assume that the memory has been configured without input registering and additional output registers.

### Write First or Read-After-Write Mode

In Write-First mode, data input is loaded simultaneously with a write operation on the DOUT port. As shown in Figure 4, the data input is stored in memory and mirrored on the output.

## Read First or Read-Before-Write Mode

In Read-First mode, data previously stored at the write address appears on the DOUT port. Data input is stored in memory and the prior contents of that location is driven on the output, during the same clock cycle (shown in Figure 5).
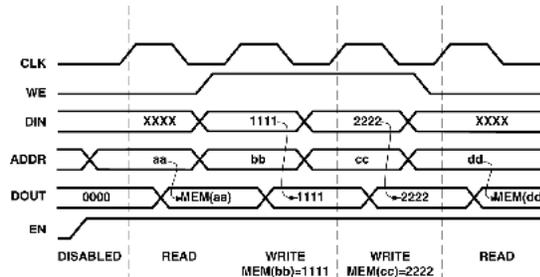
*Figure 4:* **Write First Mode Waveform**
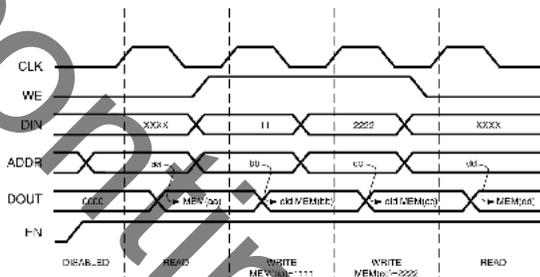
*Figure 5:* **Read First Mode Waveform**

## No Change or No Read-on-Write Mode

In No-Read-on-Write mode, the DOUT port remains unchanged during a write operation. As shown in Figure 6, data output is still the last read data and is unaffected by a write operation on the same port. Mode configuration is static. One of these three modes is set individually for each port by an attribute. The default mode is write first.

*Figure 6:* **No-Read-on-Write Mode Waveform**

## Conflict Resolution

The Virtex and Virtex-II block memory is True Dual-Port RAM that allows both ports to simultaneously access the same memory location. When one port writes to a given memory location, the other port must n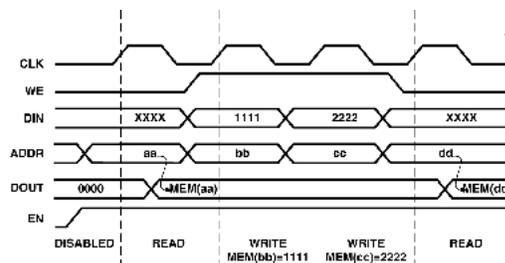ot address that memory location (for a write/read) within the clock-to-clock setup window. Note that conflicts do not cause any physical damage to BlockRAM cells. For more information on conflict resolution, refer to the *Virtex and Virtex-II Databook* available at the web site: *http://www.xilinx.com/partinfo/databook.htm*.

## Specifying Memory Contents

The initial memory contents can be assigned by specifying the desired information in a separate text file called a *coe* file. To select and load a coe file, click Load Init Values in the parameterization window; then choose the desired file from the dialog box. An example of a *coe* file for a 3 by 16 RAM is shown in Figure 6.

memory_initialization_radix=16;
memory_initialization_vector=123, 456, aaaa;

*Figure 7:* **Example COE File for Dual-Port Block RAM Version 3**

When specifying the initial contents for a memory in a *coe* file, the keywords MEMORY_INITIALIZATION_RADIX and MEMORY_INITIALIZATION_VECTOR can be used. The MEMORY_INITIALIZATION_VECTOR takes the form of a sequence of comma-separated values, one value per memory location, terminated by a semicolon. Any amount of white space, including new lines, can be included in the vector to enhance readability. The format of an individual value in the vector will depend on the MEMORY_INITIALIZATION_RADIX value, which can be 2, 10, or 16 (the default value is 10). The vector must be consistent with the MEMORY_INITIALIZATION_RADIX value and must fall within the range of 0 to $2^{DATA\_WIDTH}-1$. Values must not be negative. Note that the first entry in the coe file corresponds to the lowest block memory address.

If the initial contents for a memory is specified by a coe file, the initial values will be embedded in the EDIF netlist that is needed for implementation. To support HDL simulations, MIF files containing the initialization values are generated. These files must be copied to the active simulation directory for a successful simulation of a core.

# Parameter Values in the XCO File

Names of the XCO parameters and their parameter values are identical to the names and values shown in the GUI, except that underscore characters (_) are used instead of spaces. The text in an XCO file is case insensitive.

Tables 2 and 3 show the XCO file parameters and values, and summarize the GUI default values. The following is an example of the CSET parameters in an XCO file:

    CSET component_name = abc123
    CSET width_a = 16
    CSET width_b = 16
    CSET depth_a = 256
    CSET depth_b = 256
    CSET configuration_port_a = read_and_write
    CSET configuration_port_b = read_only
    CSET write_mode_port_a = read_before_writ
    CSET write_mode_port_b = read_only

```
CSET global_init_value = 456a
CSET load_init_file = true
CSET coefficient_file = example.coe
CSET port_a_enable_pin = false
CSET port_b_enable_pin = true
CSET port_a_handshaking_pins = true
CSET port_b_handshaking_pins = false
CSET port_a_register_inputs = true
CSET port_b_register_inputs = false
CSET port_a_additional_output_pipe_stages = 0
CSET port_b_additional_output_pipe_stages = 1
CSET port_a_init_pin = false
CSET port_b_init_pin = false
CSET port_a_init_value = 1234
CSET port_b_init_value = abcd
CSET primitive_selection = optimize_for_area
CSET select_primitive = 4kx1
CSET port_a_write_enable_polarity = active_high
CSET port_a_enable_pin_polarity = active_high
CSET port_a_initialization_pin_polarity = active_high
CSET port_a_active_clock_edge = rising_edge_triggered
CSET port_b_write_enable_polarity = active_high
CSET port_b_enable_pin_polarity = active_high
CSET port_b_initialization_pin_polarity = active_high
CSET port_b_active_clock_edge = rising_edge_triggered
```

## Core Resource Utilization

The number of Block RAM primitives required is dependent on the values of the data depth and width fields selected in the CORE Generator parameterization window.

For Virtex implementations, this value must be at least (width x depth)/4096; while for Virtex-II implementations this value must be at least (depth x width)/18432. Note that for many configurations, the number of Block RAMs will exceed this estimated value.

For some memory depths, extra logic is required to decode the address and multiplex the outputs from various primitives. Virtex, or Virtex-II CLB slices are used to provide this functionality. The number of slices required depends on the way that the depth is constructed from the primitives, the data width, and the implementation of any decoding or multiplexing.

For an accurate measure of the usage of primitives, slices, and CLBs for a particular point solution, check the **Display Core Viewer after Generation** check box in the CORE Generator system. For more information about the number of block RAMS in each device, see Tables 5, 6, 7, and 8.

*Table 2:* **Parameter File Information for Virtex**

| Parameter Name | XCO Filename Values | Default GUI Setting |
|---|---|---|
| component_name | ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| width_[A\|B] | Integer in the range of 1 to 256 | 16 |
| depth_[A\|B] | Integer in the range of 2 to 256K | 16 |
| configuration_port_ [A\|B] | One of the following keywords: read_and_write, read_only, write_only | read_and_write |
| write_mode_port_ [A\|B] | There is only one options for Spartan-II/Virtex architecture: read_after_write | read_after_write |
| global_init_value | A hex value in the range of 0 to $2^{width\_alb} - 1$ | 0 |
| load_init_file | One of the following keywords: true, false | false |
| coefficient_file | The name of the coe file in ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| port_[A\|B]_enable_pin | One of the following keywords: true, false | false |
| port_[A\|B]_handshaking_pins | One of the following keywords: true, false | false |
| port_[A\|B]_register_inputs | One of the following keywords: true, false | false |
| port_[A\|B]_additional _output_pipe_stages | Integer in the range of 0 to 1 | 0 |
| port_[A\|B]_init_pin | One of the following keywords: true, false | false |
| port_[A\|B]_init_value | 0 | 0 |
| primitive_selection | One of two values: optimize_for_area, select_primitive | optimize_for_area |
| select_primitive | 4kx1, 2kx2, 1kx4, 512x8, 256x16 | 4kx1 |
| port_a_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_initialization_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| port_b_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_initialization_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| disable_warning_messages | One of the following keywords: true, false | true |

*Table 3:* **Parameter File Information for Virtex-II**

| Parameter Name | XCO Filename Values | Default GUI Setting |
|---|---|---|
| component_name | ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| width_[A\|B] | Integer in the range of 1 to 256 | 16 |
| depth_[A\|B] | Integer in the range of 2 to 1M (256K for Spartan-3) | 16 |
| configuration_port_ [A\|B] | One of the following keywords: read_and_write, read_only, write_only | read_and_write |
| write_mode_port_ [A\|B] | One of the following keywords: read_before_write, read_after_write, no_read_on_write | read_after_write |
| global_init_value | A hex value in the range of 0 to $2^{width\_alb} - 1$ | 0 |
| load_init_file | One of the following keywords: true, false | false |
| coefficient_file | The name of the coe file in ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| port_[A\|B]_enable_pin | One of the following keywords: true, false | false |
| port_[A\|B]_handshaking_pins | One of the following keywords: true, false | false |
| port_[A\|B]_register_inputs | One of the following keywords: true, false | false |
| port_[A\|B]_additional _output_pipe_stages | Integer in the range of 0 to 1 | 0 |
| port_[A\|B]_init_pin | One of the following keywords: true, false | false |
| port_[A\|B]_init_value | A hex value in the range of 0 to $2^{width\_alb} - 1$ | 0 |
| primitive_selection | One of two values: optimize_for_area, select_primitive | optimize_for_area |
| select_primitive | 16kx1, 8kx2, 4kx4, 2kx9, 1kx18, 512x36 | 16kx1 |
| port_a_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_initialization_pin_polarity | One of two values: active_high, active_low | active_high |

*Table 3:* **Parameter File Information for Virtex-II** *(Continued)*

| Parameter Name | XCO Filename Values | Default GUI Setting |
|---|---|---|
| port_a_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| port_b_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_initialization_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| disable_warning_messages | One of the following keywords: true, false | true |

*Table 4:* **Parameter File Information for Virtex-4**

| Parameter Name | XCO Filename Values | Default GUI Setting |
|---|---|---|
| component_name | ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| width_[A\|B] | Integer in the range of 1 to 256 | 16 |
| depth_[A\|B] | Integer in the range of 2 to 1M (256K for Spartan-3) | 16 |
| configuration_port_ [A\|B] | One of the following keywords: read_and_write, read_only, write_only | read_and_write |
| write_mode_port_ [A\|B] | One of the following keywords: read_before_write, read_after_write, no_read_on_write | read_after_write |
| global_init_value | A hex value in the range of 0 to 2$^{width\_alb}$ - 1 | 0 |
| load_init_file | One of the following keywords: true, false | false |
| coefficient_file | The name of the coe file in ASCII text starting with a letter and based upon the following character set: a..z, 0..9 and _. | blank |
| port_[A\|B]_enable_pin | One of the following keywords: true, false | false |

*Table 4:* **Parameter File Information for Virtex-4** *(Continued)*

| Parameter Name | XCO Filename Values | Default GUI Setting |
|---|---|---|
| port_[A\|B]_handshaking_pins | One of the following keywords: true, false | false |
| port_[A\|B]_register_inputs | One of the following keywords: true, false | false |
| port_[A\|B]_additional _output_pipe_stages | Integer in the range of 0 to 1 | 0 |
| port_[A\|B]_init_pin | One of the following keywords: true, false | false |
| port_[A\|B]_init_value | A hex value in the range of 0 to $2^{width\_alb} - 1$ | 0 |
| primitive_selection | One of two values: optimize_for_area, select_primitive | optimize_for_area |
| select_primitive | 32xk1, 16kx1, 8kx2, 4kx4, 2kx9, 1kx18, 512x36 | 32kx1 |
| port_a_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_initialization_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_a_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| port_b_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_initialization_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_write_enable_pin_polarity | One of two values: active_high, active_low | active_high |
| port_b_active_clock_edge | One of two values: rising_edge_triggered, falling_edge_triggered | rising_edge_triggered |
| disable_warning_messages | One of the following keywords: true, false | true |

*Table 5:* **Spartan-II Device Block RAM Counts**

| Devices | # Blocks | Total Block (bits) |
|---------|----------|--------------------|
| XC2S15 | 4 | 16,384 |
| XC2S30 | 6 | 24,576 |
| XC2S50 | 8 | 32,768 |
| XC2S100 | 10 | 40,960 |
| XC2S150 | 12 | 49,152 |
| XC2S200 | 14 | 57,344 |

*Table 6:* **Virtex Device Block RAM Counts**

| Devices | # Blocks | Total Block (bits) |
|---------|----------|--------------------|
| XCV50 | 8 | 32,768 |
| XCV100 | 10 | 40,960 |
| XCV150 | 12 | 49,152 |
| XCV200 | 14 | 57,344 |
| XCV300 | 16 | 65,536 |
| XCV400 | 20 | 81,920 |
| XCV600 | 24 | 98,304 |
| XCV800 | 28 | 114,688 |
| XCV1000 | 32 | 131,072 |

*Table 7:* **Virtex-E Device Block RAM Counts**

| Devices | # Blocks | Total Block (bits) |
|---------|----------|--------------------|
| XCV50E | 16 | 65,536 |
| XCV100E | 20 | 81,920 |
| XCV200E | 28 | 114,688 |
| XCV300E | 32 | 131,072 |
| XCV400E | 40 | 163,840 |
| XCV600E | 72 | 294,912 |
| XCV1000E | 96 | 393,216 |
| XCV1600E | 144 | 589,824 |
| XCV2000E | 160 | 655,360 |
| XCV2600E | 184 | 753,664 |
| XCV3200E | 208 | 851,968 |
| XCV405E | 140 | 573,440 |
| XCV812E | 280 | 1,146,880 |

*Table 8:* **Virtex-II Device Block RAM Counts**

| Devices | # Blocks | Total Block (Kb) |
|---|---|---|
| XC2V40 | 4 | 73,728 |
| XC2V80 | 8 | 147,456 |
| XC2V250 | 24 | 432,238 |
| XC2V500 | 32 | 589,824 |
| XC2V1000 | 40 | 737,280 |
| XC2V1500 | 48 | 884,736 |
| XC2V2000 | 56 | 1,032,129 |
| XC2V3000 | 96 | 1,769,472 |
| XC2V4000 | 120 | 2,211,840 |
| XC2V6000 | 144 | 2,654,208 |
| XC2V8000 | 168 | 3,096,576 |

*Table 9:* **Virtex-II Pro Device Block RAM Counts**

| Devices | # Blocks | Total Block (Kb) |
|---|---|---|
| XC2VP2 | 12 | 221,184 |
| XC2VP4 | 28 | 516,096 |
| XC2VP7 | 44 | 811,008 |
| XC2VP20 | 88 | 1,622,016 |
| XC2VPX20 | 88 | 1,622,016 |
| XC2VP30 | 136 | 2,506,752 |
| XC2VP40 | 192 | 3,358,944 |
| XC2VP50 | 232 | 4,276,224 |
| XC2VP70 | 328 | 6,045,696 |
| XC2VPX70 | 308 | 5,677,056 |
| XC2VP100 | 444 | 8,183,808 |
| XC2VP125 | 556 | 10,248,132 |

*Table 10:* **Spartan-IIE Device Block RAM Counts**

| Devices | # Blocks | Total Block (Kb) |
|---------|----------|------------------|
| XC2S50E | 8 | 32,768 |
| XC2S100E | 10 | 40,960 |
| XC2S150E | 12 | 49,152 |
| XC2S200E | 14 | 57,344 |
| XC2S300E | 16 | 66,536 |
| XC2S400E | 40 | 163,840 |
| XC2S600E | 72 | 294,912 |

*Table 11:* **Spartan-3 Device Block RAM Counts**

| Devices | # Blocks | Total Block (Kb) |
|---------|----------|------------------|
| XC3S50 | 4 | 73,728 |
| XC3S200 | 12 | 221,184 |
| XC3S400 | 16 | 294,912 |
| XC3S1000 | 24 | 442,368 |
| XC3S1500 | 32 | 589,824 |
| XC3S2000 | 40 | 737,280 |
| XC3S4000 | 96 | 1,769,472 |
| XC3S5000 | 104 | 1,916,928 |

## Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator system v7.1i and higher. The CORE Generator system is included with the ISE Foundation software at no additional charge.

To order Xilinx software, please visit the Xilinx Silicon Xpresso Cafe or contact your local Xilinx sales representative.

Information on additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

## Revision History

| Date | Version | Revision |
|------|---------|----------|
| 5/21/04 | 1.1 | Added support for Virtex-4 and v6.2i of Xilinx Core Generator system. Updated data sheet to reflect new corporate template. |
| 04/28/05 | 1.2 | Added support for Spartan-3E and Xilinx software v7.1i. |
| 8/31/05 | 1.3 | Background GUI updates. |