

Introduction

The LogiCORE™ IP Digital Pre-Distortion (DPD) IP negates the non-linear effects of a power amplifier (PA) when transmitting a wide-band signal. DPD allows a PA to achieve greater efficiency by operating at a higher output power while maintaining spectral compliance, and reducing system capital and operational expenditure.

Features

- Algorithm:
 - DPD correction with up to 40 dB of adjacent channel leakage ratio (ACLR) improvement
- Physical Configuration Parameters
 - Selection of phase options for datapath implementation allowing a resource/sample rate trade-off
 - Selection of one, two, four or eight transmit antennas
 - Smaller filter and capture depth options for low cost solutions like micro Remote Radio Head (RRU), Distributed Antenna System (DAS) and low power PA applications.
 - Independent control of filter memory depth, capture memory depth and acceleration levels allowing for resource versus performance trade-off
- Software
 - Added support for SMP mode under Linux Operating System.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	Zynq®-7000 and Zynq UltraScale+
Supported User Interfaces	AXI4, AXI4-Lite, AXI4-Stream.
Resources	See the <i>Digital Pre-Distortion v8.0 Product Guide</i>
Provided with Core	
Design Files	Local Vivado® repository
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	See Constraining the core section in <i>Digital Pre-Distortion v8.0 Product Guide</i> (PG076) (registration required)
Simulation Model	Not Provided
Supported S/W	Executable and linkable format files are now packaged along with DFE Subsystem XRF2 Reference Design which needs to be downloaded separately.
Tested Design Flows ⁽²⁾	
Design Entry	Vivado Design Suite 2016.3
Simulation	Not supported
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

See Digital Pre-Distortion v8.0 Product Guide (PG076) for more detailed feature information.

Additional Documentation and Supporting Materials

A product guide and additional supporting materials (Advanced Debug Interface and accompanying user guide documentation) are available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/dpd_evaluation/index.htm.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the Digital Pre-Distortion [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

The DPD v8.0 core is available as an evaluation version which operates for several hours, depending on the clock frequency. The data output is set to zero after the evaluation period ends. The host interface reports EVAL_LICENSE_TIMEOUT status value when the hardware times out.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/09/2016	8.0	<ul style="list-style-type: none">Requirement changed to Vivado 2016.3 tools.
06/30/2016	8.0	EA: Xilinx Confidential Draft. <ul style="list-style-type: none">Added support for Zynq UltraScale+ MPSoC devices.Requirement changed to Vivado 2016.2 tools.
09/30/2015	7.1	<ul style="list-style-type: none">Added two features to the IP Facts table.Updated the Licensing and Ordering Information and Support sections.
12/15/2014	7.0	<ul style="list-style-type: none">Synchronize document version with core versionUpdated for Introduction and Features sections.Added IP Fact Table.
10/16/12	2.0	Updated for ISE® Design Suite 14.3.
08/15/11	1.1	Updated to include web registration information.
06/22/11	1.0	Initial Xilinx release. ISE Design Suite 13.2. Previous version of this Product Brief is XMP143.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.