LogiCORE IP Digital Pre-Distortion v8.0

PB006 December 9, 2016 **Product Brief**

Introduction

The LogiCORE™ IP Digital Pre-Distortion (DPD) IP negates the non-linear effects of a power amplifier (PA) when transmitting a wide-band signal. DPD allows a PA to achieve greater efficiency by operating at a higher output power while maintaining spectral compliance, and reducing system capital and operational expenditure.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq®-7000 and Zynq UltraScale+
Supported User Interfaces	AXI4, AXI4-Lite, AXI4-Stream.
Resources	See the *Digital Pre-Distortion v8.0 Product Guide*
Provided with Core	
Design Files	Local Vivado® repository
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	See Constraining the core section in *Digital Pre-Distortion v8.0 Product Guide*(PG076) (registration required)
Simulation Model	Not Provided
Supported S/W	Executable and linkable format files are now packaged along with DFE Subsystem XRF2 Reference Design which needs to be downloaded separately.
Tested Design Flows[2]	
Design Entry	Vivado Design Suite 2016.3
Simulation	Not supported
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Features

- Algorithm:
  - DPD correction with up to 40 dB of adjacent channel leakage ratio (ACLR) improvement
- Physical Configuration Parameters
  - Selection of phase options for datapath implementation allowing a resource/sample rate trade-off
  - Selection of one, two, four or eight transmit antennas
  - Smaller filter and capture depth options for low cost solutions like micro Remote Radio Head (RRU), Distributed Antenna System (DAS) and low power PA applications.
  - Independent control of filter memory depth, capture memory depth and acceleration levels allowing for resource versus performance trade-off
- Software
  - Added support for SMP mode under Linux Operating System.

See Digital Pre-Distortion v8.0 Product Guide (PG076) for more detailed feature information.

Additional Documentation and Supporting Materials

A product guide and additional supporting materials (Advanced Debug Interface and accompanying user guide documentation) are available for this core. Access to this material can be requested by clicking on this registration link: www.xilinx.com/member/dpd_evaluation/index.htm.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the Digital Pre-Distortion product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

The DPD v8.0 core is available as an evaluation version which operates for several hours, depending on the clock frequency. The data output is set to zero after the evaluation period ends. The host interface reports EVAL_LICENSE_TIMEOUT status value when the hardware times out.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/09/2016	8.0	• Requirement changed to Vivado 2016.3 tools.
06/30/2016	8.0	**EA**: Xilinx Confidential Draft. • Added support for Zynq UltraScale+ MPSoC devices. • Requirement changed to Vivado 2016.2 tools.
09/30/2015	7.1	• Added two features to the IP Facts table. • Updated the Licensing and Ordering Information and Support sections.
12/15/2014	7.0	• Synchronize document version with core version • Updated for Introduction and Features sections. • Added IP Fact Table.
10/16/12	2.0	Updated for ISE® Design Suite 14.3.
08/15/11	1.1	Updated to include web registration information.
06/22/11	1.0	Initial Xilinx release. ISE Design Suite 13.2. Previous version of this Product Brief is XMP143.

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