Introduction

The 7 series FPGAs memory interface solutions cores provide high-performance connections to DDR3 SDRAM and QDR II+ SRAM. For information on QDR II+ SRAM, see QDR II+ SRAM, page 3.

DDR3 SDRAM

This section discusses the features, applications, and functional description of 7 series FPGA memory interface solutions in DDR3 SDRAMs.

DDR3 SDRAM Features

- Component support for interface widths up to 72 bits
- 1 and 2 Gb density device support
- 8-bank support
- x8 and x16 device support
- 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 72 bits)
- 8-word burst support
- Support for 5 to 14 cycles of column-address strobe (CAS) latency (CL)
- On-die termination (ODT) support
- Support for 5 to 10 cycles of CAS write latency (CWL)
- ZQ calibration – initial and periodic (configurable)
- Write leveling support for DDR3 (fly-by routing topology required for DDR3 component designs)
- JEDEC-compliant DDR3 initialization support
- Source code delivery in Verilog
- 4:1 memory to FPGA logic interface clock ratio
- ECC support

Notes:

1. Refer to DS182, 7 Series FPGAs Data Sheet: DC and Switching Characteristics, for performance information.

- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received
Applications

Typical applications for the 7 series FPGA memory interface solutions include:

- DDR3 SDRAM interfaces

Figure 1 shows a high-level block diagram of the 7 series FPGA memory interface solution connecting a user design to a DDR3 SDRAM device. The physical layer (PHY) side of the design is connected to the DDR3 SDRAM device via FPGA I/O blocks (IOBs), and the user interface (UI) side is connected to the user design via FPGA logic. Refer to UG586, 7 Series FPGAs Memory Interface Solutions User Guide for more details regarding the design.

![Figure 1: DDR3 SDRAM Memory Interface Solution](DS176_01_00010)

Functional Description

As shown in Figure 1, the top-level functional blocks of the 7 series FPGAs memory interface solution include:

- The UI block:
  - Presents the user interface to a user design
  - Provides a simple and user-friendly alternative to the native interface
  - Buffers read and write data
  - Reorders read return data to match the request order
  - Presents a flat address space and translates it to the addressing required by the SDRAM

- The memory controller (MC) block:
  - Receives requests from the user design
  - Reorders requests to minimize dead states for maximum SDRAM performance
  - Manages SDRAM row/bank configuration
  - Performs high-level SDRAM management such as refresh and activate/precharge

- The PHY block:
  - Interfaces with the MC block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa
  - Translates and synchronizes control and data over various clock domains
  - Initializes the SDRAM
  - Performs write leveling for DDR3 (fly-by routing topology required for component designs)
  - Performs calibration to center align capture clocks with read data
Figure 1 also shows a user design connecting to the memory interface. An example user design is provided with the core. Refer to UG586, 7 Series FPGAs Memory Interface Solutions User Guide for more details regarding the design.

**AXI4 Slave Interface Features**

These features are optional and selectable using the MIG GUI:

- AXI4 slave-compliant memory-mapped interface
- 1:1 clock rate to the controller
- AXI4 interface data widths can be 128, 256, or 512 bits to correspond with memory data widths of 16, 32, or 64 bits
- Support for memory data width of 72 bits with ECC enabled
- Parameterized address width support
- Support for incremental (INCR) burst up to 256 data beats
- WRAP burst support

**QDR II+ SRAM**

This section discusses the features, applications, and functional description of 7 series FPGA memory interface solutions in QDR II+ SRAMs.

**Features**

- QDR II+ SRAM device support
- x18 and x36 memory width support
- Configurable data bus widths (x18, x36) using three I/O banks
- 4-word burst support
- Source code delivery in Verilog
- 2:1 memory to FPGA logic interface clock ratio
- 2.0-cycle and 2.5-cycle read latency support
- Fixed latency mode support

**Applications**

QDR II+ SRAMs are the latest generation of QDR SRAM devices that offer high-speed data transfers on separate read and write buses on the rising and falling edges of the clock. These memory devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers
Figure 2 shows a high-level block diagram of the 7 series FPGA memory interface solution connecting a user design to a QDR II+ SRAM device.

![Figure 2: QDR II+ SRAM Memory Interface Core](image)

**Functional Description**

As shown in Figure 2, the top-level functional block is composed of a PHY that interfaces to the user and to the QDR II+ SRAM device. The PHY block:

- Translates simple user read and write commands to conform to QDR II+ SRAM protocol
- Enables the user to provide up to one read and one write transaction per clock cycle for maximum throughput
- Performs calibration to center align clocks with data
- Returns data to the user with a corresponding valid signal
- Translates and synchronizes over various clock domains
- Implements an optimized half-frequency design that eliminates the need for a memory controller

For more details regarding the design, refer to UG586, 7 Series FPGA Memory Interface Solutions User Guide provided with the core.

**General Specifications**

Refer to the 7 Series FPGAs Memory Interface Solutions User Guide for more details regarding specific banking, pin location, and internal clock resource requirements for all cores.

**Verification**

The 7 series FPGAs memory interface solutions cores have been verified in simulation. Verification tests include:

- Initialization sequence
- Read calibration
- Memory read operation
- Memory write operation
- Row/bank management
- Write leveling
Additional Resources

This material provides additional information related to this data sheet:

1. JEDEC Standard JESD79-3E: DDR3 SDRAM, JEDEC Solid State Technology Association
   http://www.jedec.org

Ordering Information

The Memory Interface Generator (MIG) is included at no additional charge with the Xilinx ISE® Design Suite software and is provided under the terms of the Xilinx End User License Agreement. The memory cores are generated using the Xilinx CORE Generator software, which is a standard component of the Xilinx ISE software. For more information, visit the MIG product page.

Revision History

The following table shows the revision history for this document:

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Description of Revisions</th>
</tr>
</thead>
<tbody>
<tr>
<td>03/01/11</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
</tbody>
</table>

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