Data-Side OCM BRAM (DSBRAM) Interface Controller (v3.00c)

DS447 June 24, 2009 **Product Specification**

Introduction

The Data-Side OCM BRAM (DSBRAM) Interface Controller connects a BRAM Block to the data-side on-chip memory (DSOCM) bus in a PowerPC® 405-based embedded systems processor. For information about the DSOCM controller interface, see the *PowerPC 405 Processor Block Reference Guide*.

The DSBRAM (v3.00c) Interface Controller core is used with the Data Side OCM Bus v10 (v2.00b).

Features

- Supports byte, half-word, and word transfers
- Configurable address decoding for use on multi-slave DSOCM buses
- Configurable permanent BRAM enable for improved performance

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Virtex®-4 FX	
Version of Core	dsbram_if_cntrl	v3.00c
Resources Used		
	Min	Max
Slices	N/A	N.A.
LUTs	0	9 [1]
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	N/A	
Design Tool Requirements		
Xilinx® Implementation Tools	ISE® v11.1 software	
Verification	N/A	
Simulation	Mentor Graphics ModelSim v6.4b and above	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Note: Address decoding logic when configured for multi-slave use. Less logic required for larger address range

Functional Description

The block diagram and signals for the Data-Side OCM (DSBRAM) Interface Controller are shown in Figure 1. The signal names for the core are listed and described in Table 1.

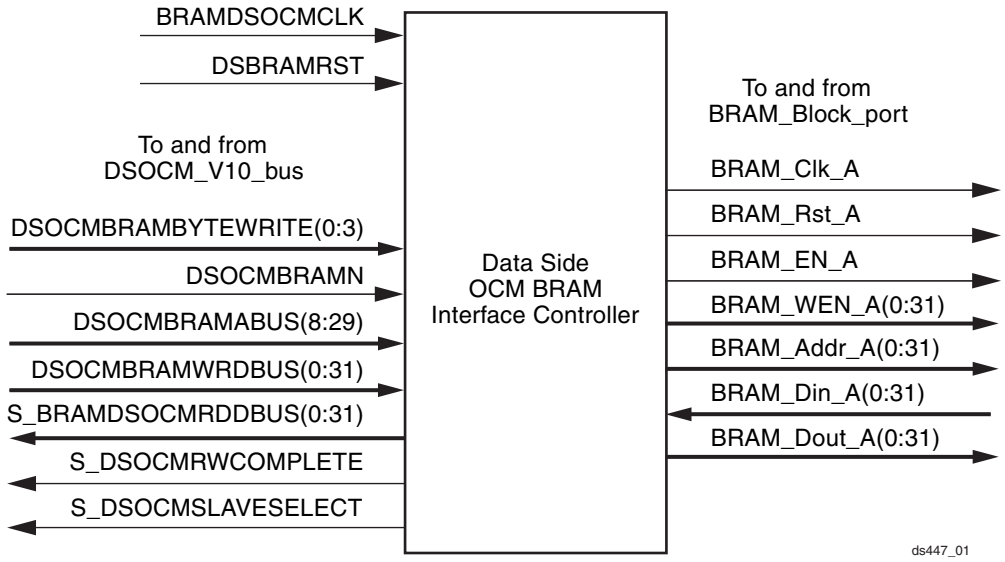

Figure 1: Data Side OCM BRAM Interface Controller Block Diagram

Data Side OCM BRAM Interface Controller I/O Signals

Table 1: **Data Side OCM BRAM Interface Controller I/O Signals**

Signal Name	Interface	I/O	Description
BRAMDSOCMCLK	DSOCM	I	This signal is passed to the BRAM_Clk_A output, which can be used as clock to the BRAM.
DSBRAMRST	DSOCM	I	This signal is passed to the BRAM_Rst_A output, which can be used as reset to the BRAM. (Active High)
DSOCMBRAMBYTEWRITE (0:3)	DSOCM	I	DSBRAM Byte Enable from PowerPC405 processor
DSOCMBRAMEN	DSOCM	I	DSBRAM Enable from PowerPC405 processor
DSOCMBRAMABUS(8:29) [1]	DSOCM	I	DSBRAM Address Bus from PowerPC405 processor
DSOCMBRAMWRDBUS (0:31)	DSOCM	I	DSBRAM Write Data Bus from PowerPC405 processor
S_BRAMDSOCMRDDBUS (0:31)	DSOCM	O	DSBRAM Read Data Bus to PowerPC405 processor
S_DSOCMRWCOMPLETE	DSOCM	O	Handshake signal for variable latency access in Virtex-4 devices.
S_DSOCMSLAVESELECT	DSOCM	O	Data valid signal used to qualify read-data from the controller in a multi-slave system (C_RANGECHECK=1)
BRAM_Rst_A	BRAM	O	BRAM Reset (Port A)
BRAM_Clk_A	BRAM	O	BRAM Clock (Port A)

Table 1: **Data Side OCM BRAM Interface Controller I/O Signals *(Cont'd)***

Signal Name	Interface	I/O	Description
BRAM_EN_A	BRAM	O	BRAM Enable (Port A)
BRAM_WEN_A(0:3)	BRAM	O	BRAM Write Enable (Port A)
BRAM_Addr_A(0:31)	BRAM	O	BRAM Address (Port A)
BRAM_Din_A(0:31)	BRAM	I	BRAM Data Input (Port A)
BRAM_Dout_A(0:31)	BRAM	O	BRAM Data Output (Port A)

Note:

1. Bits 0 through 7 are controlled by the parameter C_DSARCVALUE on the Data Side OCM Bus core.

Data Side OCM BRAM Interface Controller Parameters.

Table 2: **DSBRAM Interface Controller Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_BASEADDR	DSBRAM Base Address. Automatically calculated by the EDK tools. The most significant 8 bits of the Base Address correspond to the DSOCM Address Range Compare Value (C_DSARCVALUE) parameter of the Data Side OCM Bus core.	Valid Address Range [1]	0xFFFFFFFF [2]	std_logic_vector (0 to 31)
C_HIGHADDR	DSBRAM HIGH Address. Automatically calculated by the EDK tools.	Valid Address Range [1]	0x00000000 [2]	std_logic_vector (0 to 31)
C_BRAM_EN	Constant enable of BRAM. Improves BRAM access time while increasing static power dissipation when set to 1.	0, 1	0	integer
C_RANGE CHECK	Enable address range checking. When used on a multi-slave data-side OCM bus, this parameter must be set to 1. It enforces strict address range checking for the address space declared for this controller. On a single slave bus, the parameter can be set to 0 to save logic, however this will result in a wrap-around effect when data-side OCM addresses outside the defined range are used: data accessed on address 0 is the same as that accessed on address 2^n, for a memory controller of 2^n bytes.	0, 1	0	integer

Note:

1. The range specified by C_BASEADDR and C_HIGHADDR must be a complete, contiguous power-of-two range, with a maximum size of 16MB. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1. The 16 MB address space overlaps that of the Processor Local Bus (PLB) and cannot be used by PLB peripherals. All peripherals must reside in the same 16 MB space.
2. Default value specified for C_BASEADDR and C_HIGHADDR is used to ensure that an actual value is set; if the value is not set, a compiler error is generated.

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations.

Parameter - Port Dependencies

There are no dependencies between ports and parameters.

Data Side OCM BRAM Interface Controller Register Descriptions

There are no registers on the core.

Data Side OCM BRAM Interface Controller Interrupt Descriptions

There are no interrupt signals on the core.

Design Implementation

Design Tools

The Data Side OCM BRAM Interface Controller design is handwritten.

XST is the synthesis tool used for this device.

Target Technology

The target technology is a Virtex-4 FX FPGA.

Device Utilization and Performance Benchmarks

Not available.

Specification Exceptions

Not applicable.

Reference Documents

UG018 *PowerPC 405 Processor Block Reference Guide*

DS480 *Data Side OCM Bus Data Sheet*

DS444 *Block RAM Block Data Sheet*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/16/04	1.0	Initial Xilinx release.
8/13/04	1.1	Updated for EDK 6.3. Reviewed and corrected trademark usage and supported device family list.
9/21/04	1.2	Updated to new format for EDK 6.3 SP1
7/26/05	1.3	Converted to new DS template; incorporated CR206184.
1/23/2007	1.4	Cleaned up range-check (addr_qual) logic.
4/24/09	1.5	Replaced references to supported device families and tool name(s) with hyperlink to PDF file; converted to current DS template.
6/24/09	1.6	Incorporated CR521083; created v3.00c; added supported device families and tools in LogiCORE facts table.

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