LogiCORE IP GMII to RGMII (v1.00a)

PB014 October 16, 2012 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP Gigabit Media Independent Interface (GMII) to Reduced Gigabit Media Independent Interface (RGMII) design provides the RGMII between RGMII-compliant Ethernet physical media devices (PHY) and the Gigabit Ethernet controller in the Zynq™-7000 devices. This core can be used in all three modes of operation (10/100/1000 Mb/s). The Management Data Input/Output (MDIO) interface is used to determine the speed of operation. This core is capable enough to switch dynamically between different speed modes of 10/100/1000 Mb/s.

Features

- Tri-speed (10/100/1000 Mb/s) operation
- Half and Full Duplex operation
- MDIO interface to set operating speed by Ethernet Media Access Controller (MAC)

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000(2)
Supported User Interfaces	GMII
Provided with Core	
Documentation	Product Brief
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	ISE: UCF
Simulation Model	Not Provided
Supported S/W Driver(3)	N/A
Tested Design Flows(4)	
Design Entry	ISE Design Suite v14.3
Simulation	Not Provided
Synthesis	Xilinx Synthesis Technology (XST)
Support	
Provided by Xilinx@ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see the Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. Standalone driver details can be found in the EDK or SDK installation directory. (<install_directory>/doc/usenglish/xilinx_drivers.htm). Linux OS and driver support information is available from http://wiki.xilinx.com.
4. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

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Applications

The GMII to RGMII IP is designed for use with Zynq-7000 devices. The Gigabit Ethernet Modules in the Zynq AP SoC provide an RGMII interface through the Multiplexed I/O (MIO) pins and a GMII interface through the EMIO interface to route through the programmable logic. The GMII to RGMII IP can be used to provide an RGMII interface using the PL. For more information on the Zynq-7000 Gigabit Ethernet Controller, see the *Zynq-7000 All Programmable SoC Technical Reference Manual*.

I/O Signals

Table 1: **I/O Signals**

Signal Name	I/O	Description
tx_reset	Input	Reset in TX domain
rx_reset	Input	Reset in RX domain
clkin	Input	200 MHz clock input to the MMCM for generating 250 MHz, 50 MHz. and 5 MHz clocks
gmii_tx_clk	Output	Transmit clock output from GMII to RGMII IP to Zynq-7000 PS
gmii_txd	Input	Transmit data from MAC
gmii_tx_en	Input	Data Enable control signal from MAC
gmii_tx_er	Input	Error control signal from MAC
gmii_crs	Output	Carrier sense signal (only for half duplex mode)
gmii_col	Output	Collision signal (only for half duplex mode)
gmii_rx_clk	Output	Receive clock output from GMII to RGMII IP to Zynq-7000 PS
gmii_rxd	Output	Received data from PHY
gmii_rx_dv	Output	Data Valid control signal from PHY
gmii_rx_er	Output	Error control signal from PHY
rgmii_txd	Output	Transmit data to PHY
rgmii_tx_ctl	Output	Control signal to PHY
rgmii_txc	Output	Clock to PHY
rgmii_rxd	Input	Received data from PHY
rgmii_rx_ctl	Input	Control signal from PHY
rgmii_rxc	Input	Clock from PHY
link_status	Output	Link status from the in-band control signal
clock_speed	Output	Clock speed from the in-band control signal
duplex_status	Output	Duplex status from the in-band control signal
MDIO_I	Input	Input signal coming from Zynq-7000 Gigabit Ethernet Controller of Zynq-7000 PS
MDIO_O	Input	Input signal coming from the External PHY
MDIO_MDC	Input	MDIO clock
speed_mode[1:0]	Output	Speed mode of the MAC to the clock generator. 00 = 10 Mb/s 01 = 100 Mb/s 10 = 1 Gb/s 11 = Reserved

Ports and Interfaces

Figure 1 shows the ports and interfaces for GMII to RGMII core.

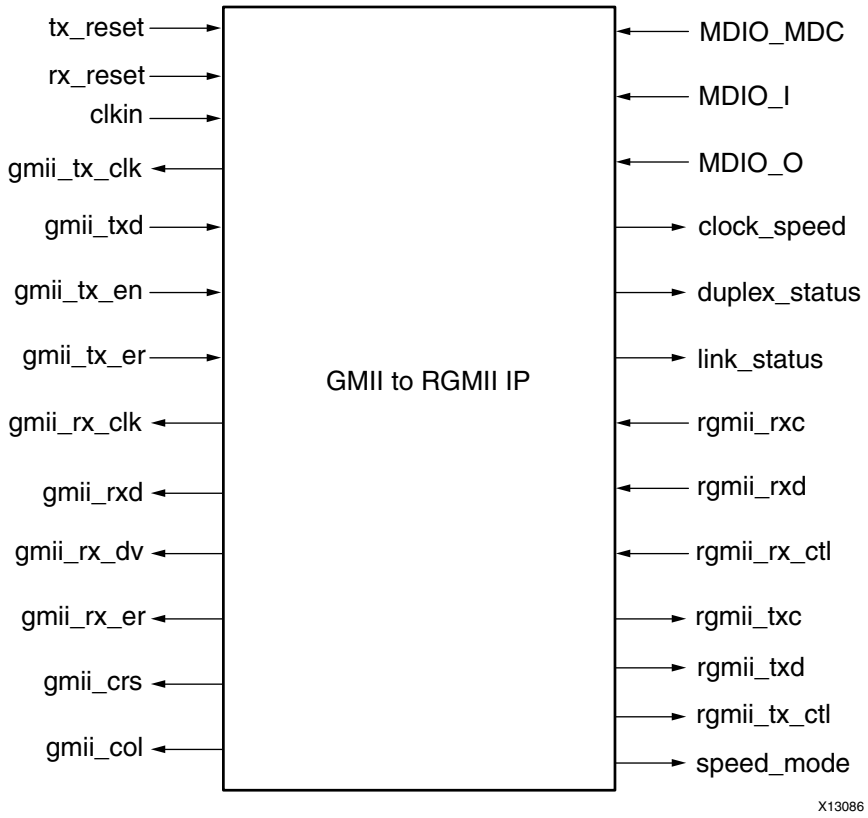

Figure 1: **GMII to RGMII Core Ports and Interfaces**

Clocking Diagrams

GMII to RGMII IP has a built-in clock generator for providing 2.5 MHz, 25 MHz, and 125 MHz frequency clocks for 10 Mb/s, 100 Mb/s, and 1 Gb/s speed of operations respectively. The clock generator uses a MMCM and two BUFGMUXs to switch between three different clock frequencies for the three different speed modes of the Ethernet MAC. The `speed_mode(0)` and `speed_mode(1)` signals are used as selection pins of BUFGMUX0 and BUFGMUX1 respectively as shown in Figure 2.

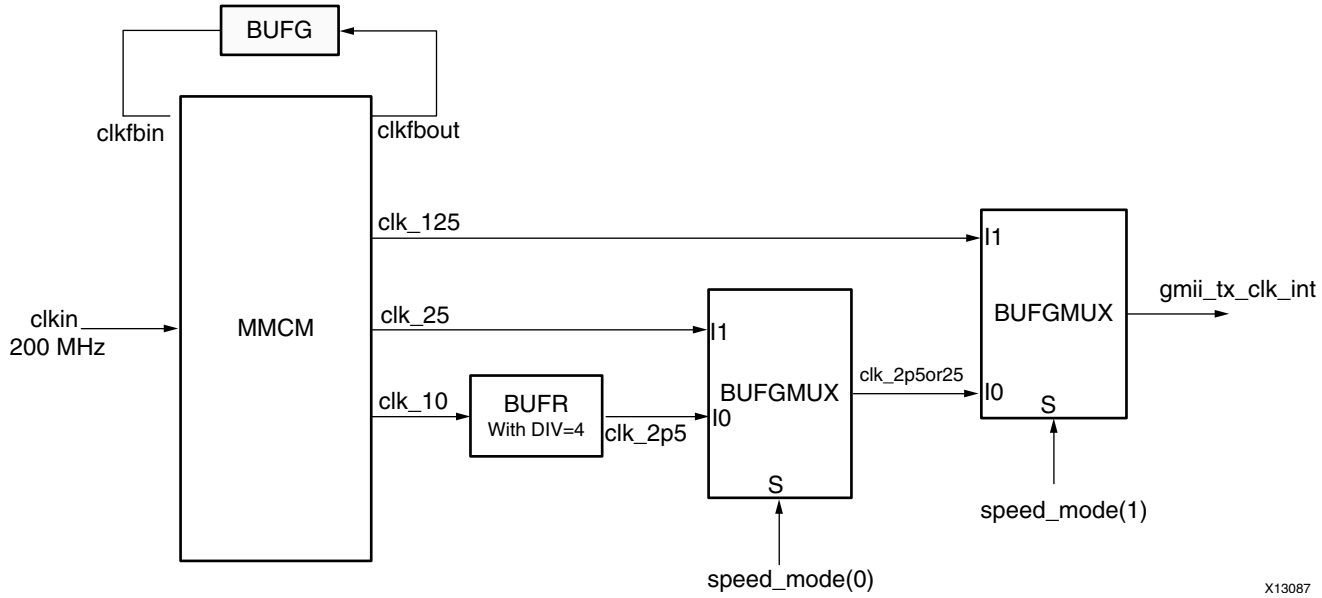

Figure 2: **Clock Generator**

Figure 3 shows the output (`gmii_tx_clk_int`) of BUFGMUX2 and it is used to provide the `gmii_tx_clk` clock to GEM. The `rgmii_txc` clock is generated from `gmii_tx_clk_int` using ODDR and the `rgmii_rxc` clock is driven through BUFR and BUGs to provide `gmii_rx_clk` clock to GEM.

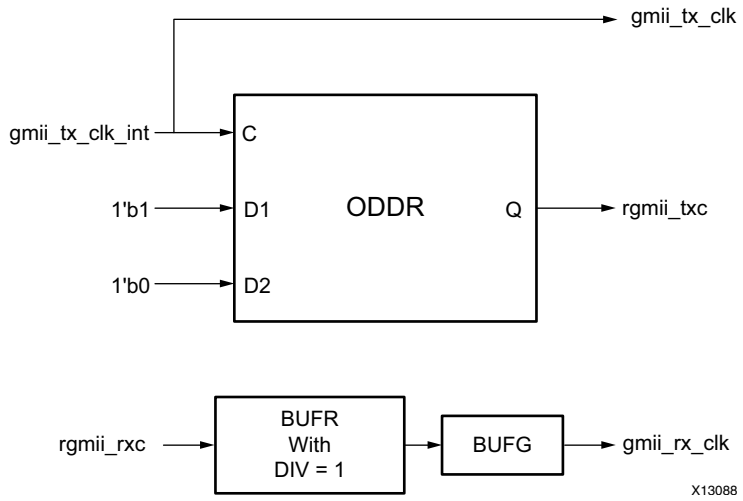

Figure 3: **Clocking Diagram**

Functional Description

Figure 4 illustrates the connection of the Gigabit Ethernet Controller in the Zynq-7000 PS to the GMII to RGMII IP. An additional I/O Buffer must be provided to drive the MDIO interface to pins.

Note: The MDIO interface is necessary for the operation of the core because the auto-negotiated speed of operation from the PHY is communicated to the Ethernet MAC via MDIO.

A clock input of 200 MHz must be provided which is used both as an input to the clock generator and a reference clock to the IDELAY control elements.

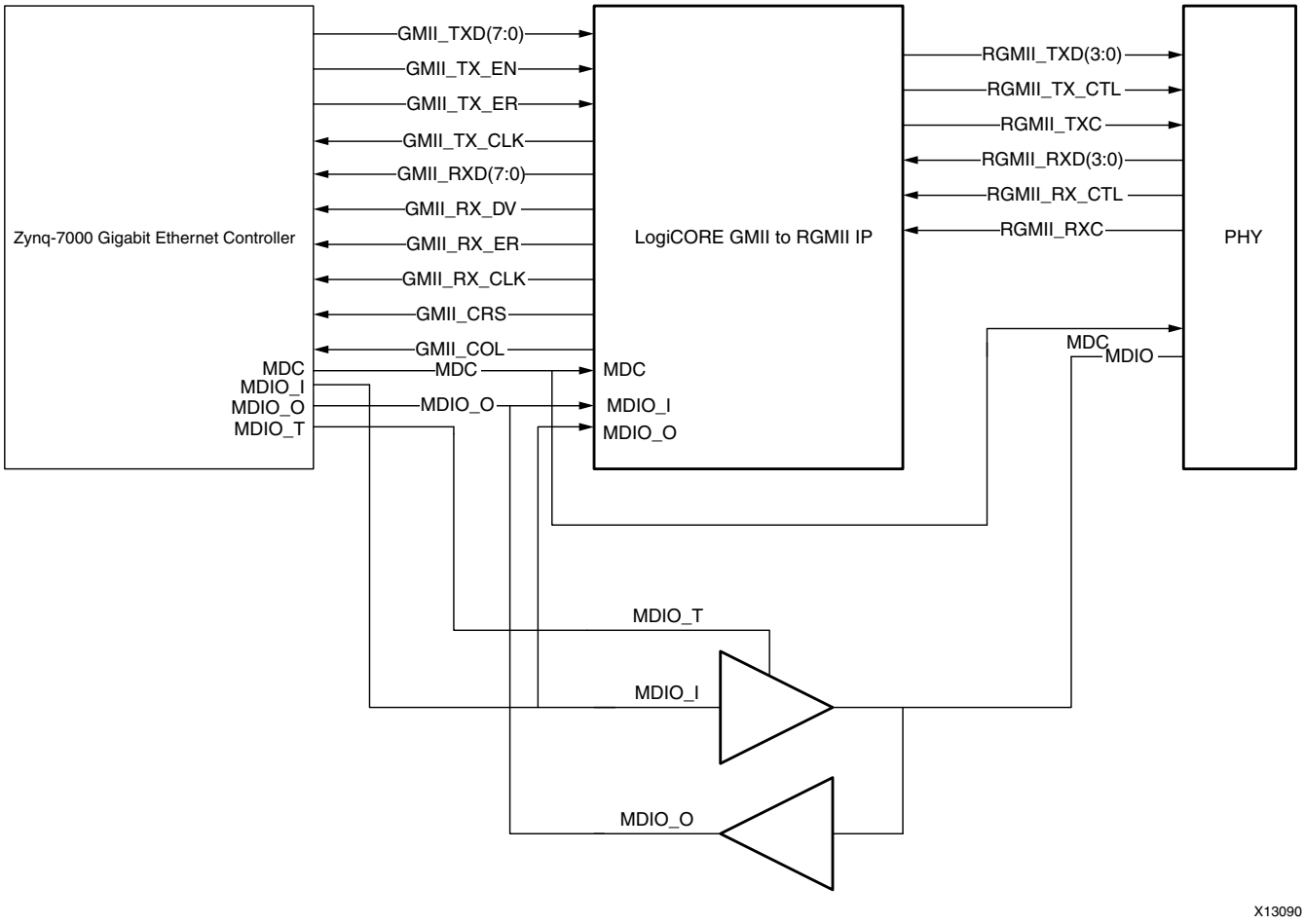

Figure 4: **Connecting Zynq-7000 Gigabit Ethernet Controller to the GMII to RGMII IP**

GMII to RGMII IP uses the MDIO interface to detect the speed to set the appropriate data width and clock frequencies. The 10/100 Mb/s modes uses only 4 out of the 8 data bits and 1000 Mb/s mode uses all 8 data bits. MDC is the management clock coming from GigE. `MDIO_I` and `MDIO_O` are input signals driven from the Zynq GigE and the external PHY respectively.

GMII to RGMII Parameters

Table 2 shows the features that are parameterizable in the GMII to RGMII IP. This allows users to obtain a customized GMII to RGMII design for their system.

Table 2: **GMII to RGMII Parameters**

Name	Description	Default Values	Allowable Values
C_HALFDUP	To enable half duplex mode	0	0 = Full duplex 1 = Half duplex
C_PHYAD	To set the PHY address	00111	00000 to 11111

Design Implementation

Design Tools

The Xilinx Synthesis Tool is used to synthesize the GMII to RGMII core.

Design Constraints

The GMII to RGMII IP requires design constraints to guarantee performance. These constraints should be placed in an UCF at the top-level of the design. The example of the constraint text shown in Figure 5 is based on the port names of the GMII to RGMII core. If these ports are mapped to FPGA pin names that are different, then the FPGA pin names should be submitted for the port names in the following example.

Note: The pin names should also be updated.

```
NET   "CLK_P" LOC = "D18" |   IOSTANDARD  = LVDS_25 ; # Bank: 35 - Byte:
NET   "CLK_N" LOC = "C19" |   IOSTANDARD  = LVDS_25 ; # Bank: 35 - Byte:
NET "CLK" TNM_NET = TNM_sys_clk;
TIMESPEC "TS_clk" = PERIOD "TNM_sys_clk" 5 ns;


NET ENET1_RST                LOC = A18     | IOSTANDARD  = LVCMOS18 ;   # BANK 35
NET ENET1_MDIO               LOC = AB15    | IOSTANDARD  = LVCMOS18 ;    # BANK 33
NET ENET1_MDIO_MDC           LOC = Y13     | IOSTANDARD  = LVCMOS18 ;

NET ENET1_RGMII_TX_CTL       LOC = U16     | IOSTANDARD  = LVCMOS18  | SLEW = FAST | DRIVE = 24 ;
NET ENET1_RGMII_TX_CLK       LOC = AB19    | IOSTANDARD  = LVCMOS18  | SLEW = FAST ;
NET ENET1_RGMII_TXD[0]       LOC = AB14    | IOSTANDARD  = LVCMOS18  | SLEW = FAST | DRIVE = 24 ;
NET ENET1_RGMII_TXD[1]       LOC = U15     | IOSTANDARD  = LVCMOS18  | SLEW = FAST | DRIVE = 24 ;
NET ENET1_RGMII_TXD[2]       LOC = AB20    | IOSTANDARD  = LVCMOS18  | SLEW = FAST | DRIVE = 24 ;
NET ENET1_RGMII_TXD[3]       LOC = V13     | IOSTANDARD  = LVCMOS18  | SLEW = FAST | DRIVE = 24 ;

NET ENET1_RGMII_RX_CLK       LOC = W15     | IOSTANDARD  = LVCMOS18 ;
NET ENET1_RGMII_RX_CTL       LOC = AB16    | IOSTANDARD  = LVCMOS18 ;
NET ENET1_RGMII_RXD[0]       LOC = W13     | IOSTANDARD  = LVCMOS18 ;
NET ENET1_RGMII_RXD[1]       LOC = AA16    | IOSTANDARD  = LVCMOS18 ;
NET ENET1_RGMII_RXD[2]       LOC = Y15     | IOSTANDARD  = LVCMOS18 ;
NET ENET1_RGMII_RXD[3]       LOC = U17     | IOSTANDARD  = LVCMOS18 ;


OFFSET = IN 1 ns valid 3 ns BEFORE "ENET1_RGMII_RX_CLK" RISING;
OFFSET = IN 1 ns valid 3 ns BEFORE "ENET1_RGMII_RX_CLK" FALLING;

NET ENET1_RGMII_RX_CLK TNM_NET = "CLK_ENET1_RX";
TIMESPEC "TS_CLK_ENET1_RX" = PERIOD "CLK_ENET1_RX" 8000 ps HIGH 50.00%;


INST "*delay_rgmii_rx_ctl"      IDELAY_VALUE  =  16;
INST "*delay_rgmii_rxd*"        IDELAY_VALUE  =  16;
INST "*delay_rgmii_rx_ctl"      IODELAY_GROUP = "grp1";
INST "*delay_rgmii_rxd*"        IODELAY_GROUP = "grp1";
INST "*dlyctrl"                 IODELAY_GROUP = "grp1"
```

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Figure 5: **Timing Constraints**

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IDS Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
10/16/12	1.0	Initial Xilinx release.

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