200G IEEE 802.3bs Reed-Solomon Forward Error Correction v2.0

PB066 (v2.0) January 7, 2021 **LogiCORE IP Product Brief**

Introduction

The Xilinx® LogiCORE™ 200G IEEE 802.3bs Reed-Solomon Forward Error Correction IP core implements the Reed-Solomon Forward Error Correction (RS-FEC) functions within the Physical Coding Sublayer (PCS) for 200GBASE-R PHYs as described in Clause 119 of *IEEE Standard for Ethernet* (IEEE Std 802.3-2018).

Additional Information

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: https://www.xilinx.com/member/200g-rs-fec.html.

Features

- IEEE Std. 802.3-2018 TX and RX
- Support for 200G Ethernet FEC
  - Option to use Virtex® UltraScale+™ GTM transceivers for significant resource reduction
  - Low latency soft IP implementation
- Dynamic latency reporting
- Configuration and status bus
- Supports RS(544,514) KP4 encode and decode
- Supports symbol error statistics (including per-lane statistics)

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Versal™, UltraScale™, UltraScale+™[2]
Supported User Interfaces	AXI4-Stream
Resources	For details about performance and resource use, see `ieee802d3-200g-rs-fec.html`.
Provided with Core	
Design Files	Encrypted RTL
Example Design	N/A
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows[3]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado® Design Suite
Support	
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

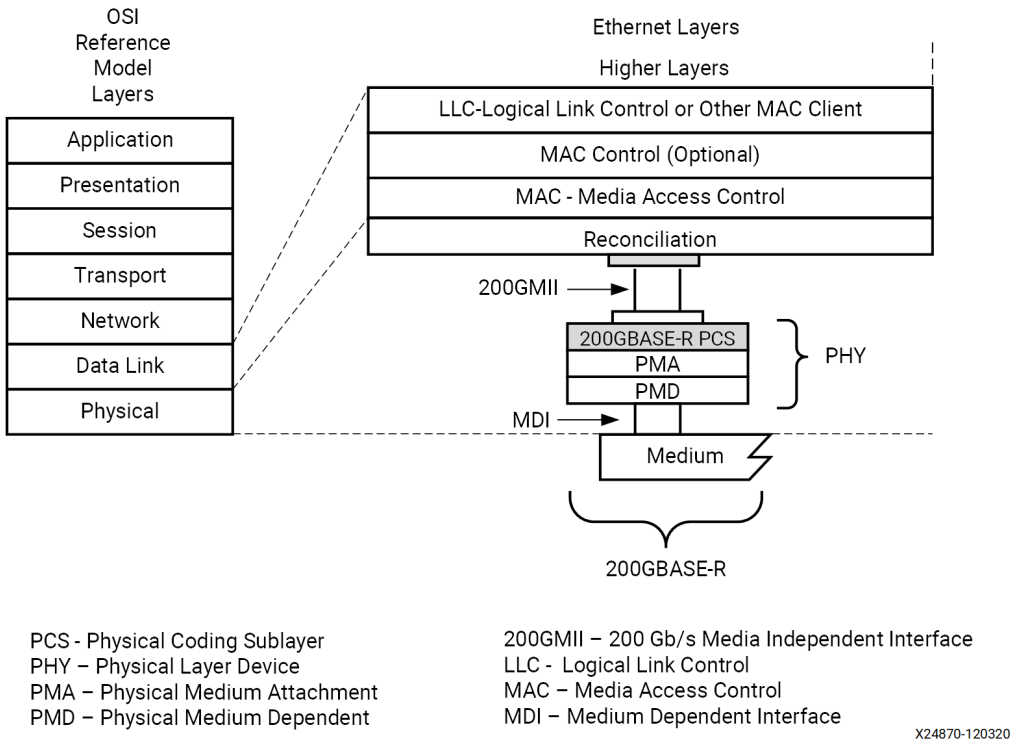
1. For a complete list of supported devices, see the Vivado® IP catalog.
2. -1 speed grades are not supported for these devices.
3. For the supported versions of third-party tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Core Overview

The 200G IEEE 802.3bs RS-FEC core implements the Reed-Solomon Forward Error Correction (RS-FEC) functions which are part of the 200GBASE-R PCS layer, as described in IEEE 802.3bs and shown shaded in the following figure.

Figure 1: **Architectural Position of 200G Ethernet PCS Layer**



The 200G IEEE 802.3bs RS-FEC core provides FEC encoding and decoding functions using the FPGA logic fabric. This 'soft logic' implementation is available in all supported device families.

Applications

The use of RS-FEC is mandatory for all 200G Ethernet ports that adhere to the IEEE Standard for Ethernet 802.3-2018. The 200G IEEE 802.3bs RS-FEC core can be used to provide forward error correction for any 200G Ethernet PHY, as commonly used in applications such as Ethernet switches, IP routers, data center switches, and communications equipment.

Unsupported Features

The following features of the standard are not supported in the core:

- Scrambling/Descrambling, transcoding and alignment marker mapping/demapping
- AXI status/control interface
- Full FEC bypass or correction bypass modes

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the 200G IEEE 802.3bs RS-FEC product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
01/07/2021 Version 2.0	
Initial release.	N/A

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