

## Introduction

The Xilinx® LogiCORE™ 200G IEEE 802.3bs Reed-Solomon Forward Error Correction IP core implements the Reed-Solomon Forward Error Correction (RS-FEC) functions within the Physical Coding Sublayer (PCS) for 200GBASE-R PHYs as described in Clause 119 of *IEEE Standard for Ethernet* ([IEEE Std 802.3-2018](https://www.ieee.org/standards/publications/802.3-2018)).

## Additional Information

A full product guide is available for this core. Access to this material can be requested by clicking on this registration link: <https://www.xilinx.com/member/200g-rs-fec.html>.

## Features

- IEEE Std. 802.3-2018 TX and RX
- Support for 200G Ethernet FEC
  - Option to use Virtex® UltraScale+™ GTM transceivers for significant resource reduction
  - Low latency soft IP implementation
- Dynamic latency reporting
- Configuration and status bus
- Supports RS(544,514) KP4 encode and decode
- Supports symbol error statistics (including per-lane statistics)

## IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family <sup>1</sup>	Versal™, UltraScale™, UltraScale+™ <sup>2</sup>
Supported User Interfaces	AXI4-Stream
Resources	For details about performance and resource use, see <a href="#">ieee802d3-200g-rs-fec.html</a> .
Provided with Core	
Design Files	Encrypted RTL
Example Design	N/A
Test Bench	Not Provided
Constraints File	Xilinx Constraints File
Simulation Model	Encrypted Verilog
Supported S/W Driver	N/A
Tested Design Flows <sup>3</sup>	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the <a href="#">Xilinx Design Tools: Release Notes Guide</a> .
Synthesis	Vivado® Design Suite
Support	
All Vivado IP Change Logs	Master Vivado IP Change Logs: <a href="#">72775</a>
<a href="#">Xilinx Support web page</a>	

**Notes:**

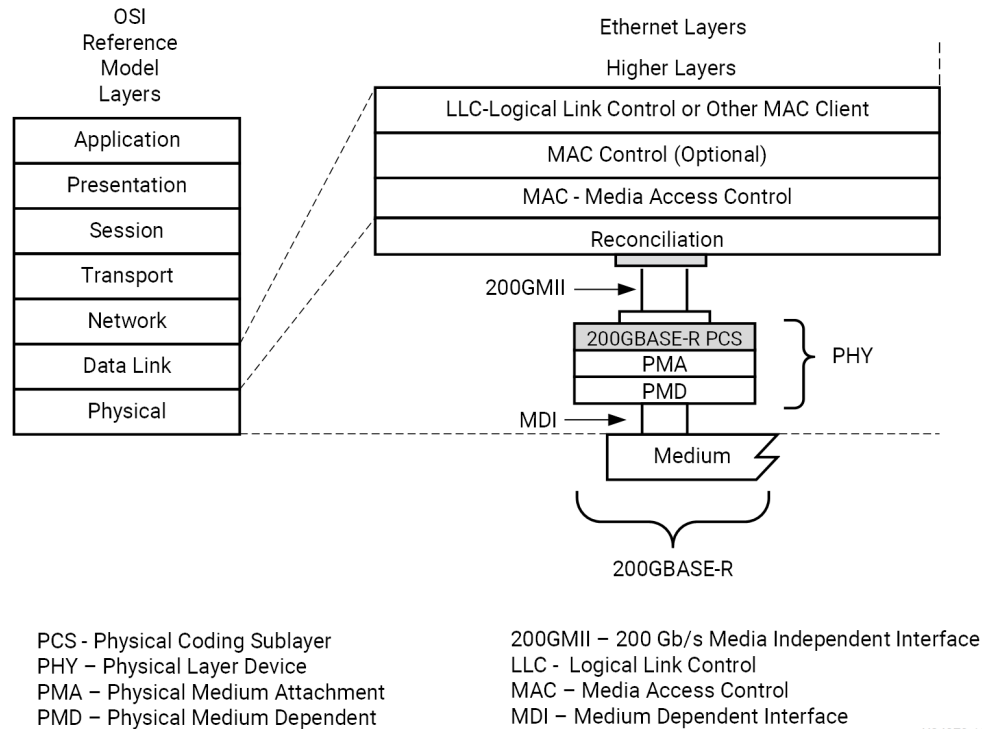
1. For a complete list of supported devices, see the Vivado® IP catalog.
2. -1 speed grades are not supported for these devices.
3. For the supported versions of third-party tools, see the [Xilinx Design Tools: Release Notes Guide](#).

## Overview

### Core Overview

The 200G IEEE 802.3bs RS-FEC core implements the Reed-Solomon Forward Error Correction (RS-FEC) functions which are part of the 200GBASE-R PCS layer, as described in IEEE 802.3bs and shown shaded in the following figure.

**Figure 1: Architectural Position of 200G Ethernet PCS Layer**



The 200G IEEE 802.3bs RS-FEC core provides FEC encoding and decoding functions using the FPGA logic fabric. This 'soft logic' implementation is available in all supported device families.

## Applications

The use of RS-FEC is mandatory for all 200G Ethernet ports that adhere to the IEEE Standard for Ethernet 802.3-2018. The 200G IEEE 802.3bs RS-FEC core can be used to provide forward error correction for any 200G Ethernet PHY, as commonly used in applications such as Ethernet switches, IP routers, data center switches, and communications equipment.

## Unsupported Features

The following features of the standard are not supported in the core:

- Scrambling/Descrambling, transcoding and alignment marker mapping/demapping
- AXI status/control interface
- Full FEC bypass or correction bypass modes

## Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the [product licensing web page](#). Evaluation licenses and hardware timeout licenses might be available for this core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

**Note:** To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the 200G IEEE 802.3bs RS-FEC [product web page](#).

Information about other Xilinx® LogiCORE™ IP modules is available at the [Xilinx Intellectual Property](#) page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

## License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write\_bitstream (Tcl command)



---

**IMPORTANT!** IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

---

## Technical Support

Xilinx provides technical support on the [Xilinx Community Forums](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the [Xilinx Community Forums](#).

## Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help** → **Documentation and Tutorials**.
- On Windows, select **Start** → **All Programs** → **Xilinx Design Tools** → **DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

**Note:** For more information on DocNav, see the [Documentation Navigator](#) page on the Xilinx website.

## Revision History

The following table shows the revision history for this document.

Section	Revision Summary
01/07/2021 Version 2.0	
Initial release.	N/A

## Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal>

[www.xilinx.com/legal.htm#tos](http://www.xilinx.com/legal.htm#tos); IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <https://www.xilinx.com/legal.htm#tos>.

## **AUTOMOTIVE APPLICATIONS DISCLAIMER**

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

## **Copyright**

© Copyright 2021 Xilinx, Inc. Xilinx, the Xilinx logo, Alveo, Artix, Kintex, Spartan, Versal, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.