Instruction-Side OCM BRAM (ISBRAM) Interface Controller (v3.00c)

DS446 June 24, 2009 **Product Specification**

Introduction

The ISBRAM_IF_CNTLR connects the BRAM_Block to the instruction-side on-chip memory (ISOCM) bus in a PowerPC® 405 based embedded systems processor. For information about the ISOCM controller interface, see the *PowerPC 405 Processor Block Reference Guide*.

The v3.00c ISBRAM_IF_CNTRL core is used with the v2.00b ISOCM_V10 bus.

Features

- Debug access via DCR
- Configurable permanent BRAM enable for improved performance

LogiCore™ IP Facts		
Core Specifics		
Supported Device Family	Virtex®-4 FX	
Version of Core	isbram_if_cntrl	v3.00c
Resources Used		
	Min	Max
Slices	N/A	N.A
LUTs	0	18(1)
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Description	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	N/A	
Design Tool Requirements		
Xilinx® Implementation Tools	ISE® v11.1 software	
Verification	N/A	
Simulation	Mentor Graphics ModelSim v6.4b and above	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

1. Address decoding logic when configured for multi-slave use. Less logic required for larger address range

Functional Description

The input/output signals of the Instruction-Side OCM BRAM interface controller are shown in Figure 1 and listed and described in Table 1.

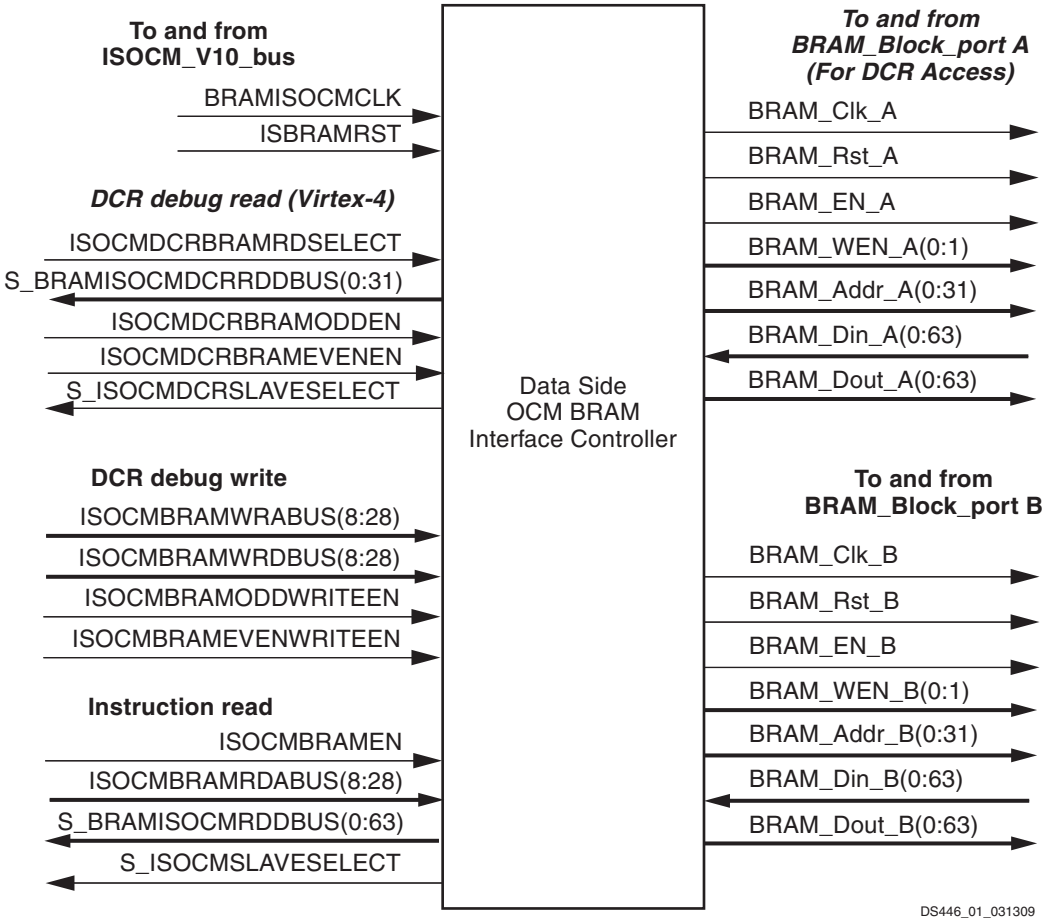

Figure 1: **Instruction Side OCM BRAM Interface Controller Block Diagram**

ISOCM BRAM Interface Controller I/O Signals

Table 1: **ISOCM BRAM Interface Controller I/O Signals**

Signal Name	Interface	I/O	Description
BRAMISOCMCLK	ISOCM	I	This signal is passed to BRAM_Clk_A and BRAM_Clk_B outputs.
ISBRAMRST	ISOCM	I	This signal is passed to BRAM_Rst_A and BRAM_Rst_B outputs, which can be used as reset to the BRAM. (Active High)
ISOCMDCRBRAMRD SELECT	ISOCM	I	Virtex-4 device only. Select signal determining if Odd or Even word is returned on read. Controlled by ISINIT(29)
ISOCMDCRBRAMODDEN	ISOCM	I	Virtex-4 device only. ISBRAM Odd Word BRAM Enable from a PowerPC 405 processor. DCR read using ISINIT(29)
ISOCMDCRBRAMEVENEN	ISOCM	I	Virtex-4 device only. ISBRAM Even Word BRAM Enable from a PowerPC 405 processor. DCR read using ISINIT(29)
S_ISOCMDCRSLAVE SELECT	ISOCM	O	Virtex-4 device only. Read-data valid to qualify DCR read-data from the controller on a multi-slave bus (C_RANGECHECK=1)
S_BRAMISOCMDCR RDDBUS(0:31)	ISOCM	O	Virtex-4 device only. Read data for DCR read to ISFILL
ISOCMBRAMODD WRITEEN	ISOCM	I	ISBRAM Odd Word Write Enable from a PowerPC 405 processor. DCR write using ISINIT(29)
ISOCMBRAMEVEN WRITEEN	ISOCM	I	ISBRAM Oven Word Write Enable from a PowerPC 405 processor. DCR write using ISINIT(29)
ISOCMBRAMWRA BUS(8:28)	ISOCM	I	ISBRAM Write Address Bus from a PowerPC 405 processor. DCR read/write using ISINIT(8:28)
ISOCMBRAMWRDBUS (0:31)	ISOCM	I	ISBRAM Write Data Bus from a PowerPC 405 processor. DCR write using ISFILL
ISOCMBRAMEN	ISOCM	I	ISBRAM Enable from a PowerPC 405 processor
ISOCMBRAMRDABUS (8:28)(1)	ISOCM	I	ISBRAM Read Address Bus from a PowerPC 405 processor
S_ISOCMSLAVESELECT	ISOCM	O	Read-data valid to qualify read-data from the controller on a multi-slave bus (C_RANGECHECK=1)
S_BRAMISOCMRDD BUS(0:63)	ISOCM	O	ISBRAM Read Data Bus to a PowerPC 405 processor
BRAM_Rst_A	BRAM	O	BRAM Reset (Port A). Used for DCR debug accesses.
BRAM_Clk_A	BRAM	O	BRAM Clock (Port A). Used for DCR debug accesses.
BRAM_EN_A	BRAM	O	BRAM Enable (Port A). Used for DCR debug accesses.
BRAM_WEN_A(0:1)	BRAM	O	BRAM Write Enable (Port A). Used for DCR debug accesses.
BRAM_Addr_A(0:31)	BRAM	O	BRAM Address (Port A). Used for DCR debug accesses.
BRAM_Din_A(0:63)	BRAM	I	BRAM Data Input (Port A). Used for DCR debug accesses.
BRAM_Dout_A(0:63)	BRAM	O	BRAM Data Output (Port A). Used for DCR debug accesses.
BRAM_Rst_B	BRAM	O	BRAM Reset (Port B). Used for instruction read access.
BRAM_Clk_B	BRAM	O	BRAM Clock (Port B). Used for instruction read access.

Table 1: **ISOCM BRAM Interface Controller I/O Signals *(Cont'd)***

Signal Name	Interface	I/O	Description
BRAM_EN_B	BRAM	O	BRAM Enable (Port B). Used for instruction read access.
BRAM_WEN_B(0:1)	BRAM	O	BRAM Write Enable (Port B). Used for instruction read access.
BRAM_Addr_B(0:31)	BRAM	O	BRAM Address (Port B). Used for instruction read access.
BRAM_Din_B(0:63)	BRAM	I	BRAM Data Input (Port B). Used for instruction read access.
BRAM_Dout_B(0:63)	BRAM	O	BRAM Data Output (Port B). Used for instruction read access.

1. Bits 0 through 7 are controlled by the parameter C_ISARCVALUE on the Instruction Side OCM Bus core.

Instruction Side OCM BRAM Interface Controller Parameters

Table 2: **Instruction Side OCM BRAM Interface Controller Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_BASEADDR	ISBRAM Base Address. Automatically calculated by the EDK tools. The most significant 8 bits of the Base Address correspond to the ISOCM Address Range Compare Value (C_ISARCVALUE) parameter of the Instruction Side OCM Bus core	Valid Address Range (1)	0xFFFFFFFF (2)	std_logic_vector
C_HIGHADDR	ISBRAM High Address. Automatically calculated by the EDK tools.	Valid Address Range (1)	0x00000000 2	std_logic_vector
C_BRAM_EN	Constant enable of BRAM. Improves BRAM access time while increasing static power dissipation when set to 1.	0, 1	0	integer
C_RANGECHECK	Enable address range checking. When used on a multi-slave instruction-side OCM bus, this parameter must be set to 1. It enforces strict address range checking for the address space declared for this controller. On a single slave bus, the parameter can be set to 0 to save logic, however this will result in a wrap-around effect when instruction-side OCM addresses outside the defined range are used: data accessed on address 0 is the same as that accessed on address 2^n, for a memory controller of 2^n bytes.	0, 1	0	integer

1. The range specified by C_BASEADDR and C_HIGHADDR must be a complete, contiguous power-of-two range, with a maximum size of 16MB. The 16 MB address space overlaps that of the Processor Local Bus (PLB) and cannot be used by PLB peripherals. All peripherals must reside in the same 16 MB space.
2. Default value specified for C_BASEADDRand C_HIGHADDR is used to ensure that an actual value is set; if the value is not set, a compiler error is generated. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations.

Parameter - Port Dependencies

There are no dependencies between ports and parameters.

Register Descriptions

There are no registers on the core.

Interrupt Descriptions

There are no interrupt signals on the core.

Design Implementation

Design Tools

The Instruction Side OCM BRAM Interface Controller design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Instruction Side OCM BRAM Interface Controller.

Target Technology

The target technology is a Virtex-4 FX FPGA.

Device Utilization and Performance Benchmarks

Not available.

Specification Exceptions

Not applicable.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

1. UG018 *PowerPC 405 Processor Block Reference Guide*
2. DS479 *Instruction Side OCM Bus v1.0 Data Sheet*
3. DS444 *Block RAM (BRAM) Block Data Sheet*

Revision History

Date	Version	Revision
6/16/04	1.0	Initial Xilinx release.
8/18/04	1.1	Updated for EDK 6.3. Updated trademarks and supported device family listing.
9/21/04	1.2	Converted to new format for Gmm SP1
8/5/05	1.3	Converted to new DS template; updated Fig 1 to graphic standards.
1/23/07	1.4	Cleaned up range-check (addr_qual) logic.
4/24/09	1.5	Replaced references to supported device families and tool name(s) with hyperlink to PDF file; converted to current DS template.
6/24/09	1.6	Incorporated CR521083; created v3.00c; added supported device families and tools in LogiCORE facts table.

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