Introduction

The Low Density Parity Check (LDPC) soft IP core supports LDPC decoding and encoding. The LDPC codes used are highly configurable, and the specific code used can be specified on a codeword-by-codeword basis.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/ldpc-enc-dec.html

Features

- LDPC decode or encode of a range of customer specified Quasi-cyclic (QC) codes, including 5G NR codes
- Throughput\(^{(1)}\) up to:
  - 1.78 Gb/s for LDPC decode @ 8 iterations
  - 12.5 Gb/s for LDPC encode
- High bandwidth AXI4-Stream interfaces

1. See performance in the Product Guide for clock frequency of 400 MHz. Throughput depends on the codes and how they are mixed and the actual clock frequency on the device.

---

Notes:
1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
Overview

Forward Error Correction (FEC) codes such as Low Density Parity Check (LDPC) codes provide a means to control errors in data transmissions over unreliable or noisy communication channels. The LDPC Encoder/Decoder core provides an optimized block for encoding and soft-decision decoding of these codes. Custom and standardized LDPC codes are supported through the ability to specify the parity check matrix either through configuration or over an AXI4-Lite bus. A block diagram of the LDPC Encoder/Decoder core is shown in Figure 1.

Figure 1: LDPC Encoder/Decoder Core Block Diagram
Feature Summary

The LDPC Encoder/Decoder core is a highly flexible soft-decision LDPC decoder and encoder with the following features:

- Highly configurable codes
  - A range of quasi-cyclic codes can be configured using a bitstream or over an AXI4-Lite interface
  - Code parameter memory can be shared across up to 128 codes
  - Codes can be selected on a block-by-block basis
  - 5G support mode where tables are pre-loaded
- Normalized min-sum or offset min-sum decoding algorithm
  - Normalization factor programmable (from 0.0625 to 1 in steps of 0.0625) for layers
  - Offset factor can be specified per block (from 0.25 to 3.75 in steps of 0.25)
- Number of iterations between 1 and 63
  - Specified for each block using the AXI4-Stream control interface
- Early termination
  - Specified for each block to be none, one, or both of the following:
    - Parity check passes
    - No change in hard information or parity bits since last iteration
- When configured as a decoder, soft or hard outputs
  - Specified for each block to include information and optional parity
  - 6-bit soft log-likelihood ratio (LLR) input (8-bit interface, 2 fractional bits, with external saturation before input to symmetric range -7.75 to +7.75 assumed) and 8-bit output
- In- or out-of-order execution of blocks, with user specified ID field to identify blocks
- Encoder and Decoder variants, with optional support for improved throughput when the LDPC code sub-matrix size is small.
- Optional final parity check to provide parity pass/fail for final output
- Optional initialization of codes from device configuration, avoiding download using AXI4-Lite interface
- Interfaces
  - Wide data interfaces on input and output
  - Ability to specify number of LLR values on either a block-by-block basis or transfer basis
  - Separate inputs to specify control parameters and receive status output on a block-by-block basis
Applications

The LDPC Encoder/Decoder core is intended for use in applications requiring LDPC encode/decode, such as 5G wireless, backhaul, and DOCSIS 3.1 cable modems.

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core or subsystem. Contact your local Xilinx sales representative for information about pricing and availability.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>04/04/2018</td>
<td>2.0</td>
<td>Updated to align with Product Guide (PG281) updates.</td>
</tr>
<tr>
<td>10/04/2017</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
</tbody>
</table>
Please Read: Important Legal Notices

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS “XA” IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE (“SAFETY APPLICATION”) UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD (“SAFETY DESIGN”). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.