Lossless Compression v1.0

LogiCORE IP Product Guide

Vivado Design Suite

PG387 (v1.0) December 17, 2020

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Introduction

The Xilinx® LogiCORE™ Lossless Compression is a soft IP that provides decompression functions for lossless compression algorithms such as GZIP/ZLIB. These algorithms adhere to the RFC standard specification. This IP supports AXI4-Stream input and output interfaces.

Features

- Supports GZIP/ZLIB Decompression function as per RFC 1950/1951/1952
- Supports dynamic Huffman, static Huffman and uncompressed blocks as mentioned in RFC 1950
- Configurable History Window size
- Supports AXI4-Stream Interface
- Configurable input data width

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Versal™ ACAP, UltraScale+™, and UltraScale™
Supported User Interfaces	AXI4-Stream
Resources	Performance and Resource Use web page
Provided withCore	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of third-party tools, see the Xilinx Design Tools: Release Notes Guide.

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Chapter 2

Overview

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

- **Hardware, IP, and Platform Development:** Creating the PL IP blocks for the hardware platform, creating PL kernels, subsystem functional simulation, and evaluating the Vivado® timing, resource use, and power closure. Also involves developing the hardware platform for system integration. Topics in this document that apply to this design process include:
  - Port Descriptions
  - Clocking
  - Resets
  - Customizing and Generating the Core

Core Overview

Over the recent years, the data that is required to be stored is increasing exponentially. Data centers are expanding and evolving with new storage technologies to store the large amount of data. Data centers use Compression as one of the critical applications to store such large amount of data. Most importantly Lossless Compression applications are used in the data centers to avoid any kind of loss of information. Lossless Compression IP is designed to meet the demand for such needs along with providing high performance that can be seamlessly integrated into these systems.

The core supports GZIP/ZLIB Decompression functions. The major components of the core are LZ77 Decompression engine and Huffman tree builder block.

Applications

You can use the Lossless Compression IP in several storage and network applications such as in-line compression. In storage applications such as block compression, you can configure the Lossless Compression IP for a specific block size.

Unsupported Features

This version of the core does not support Compression function.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

***Note*:** To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the Lossless Compression product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

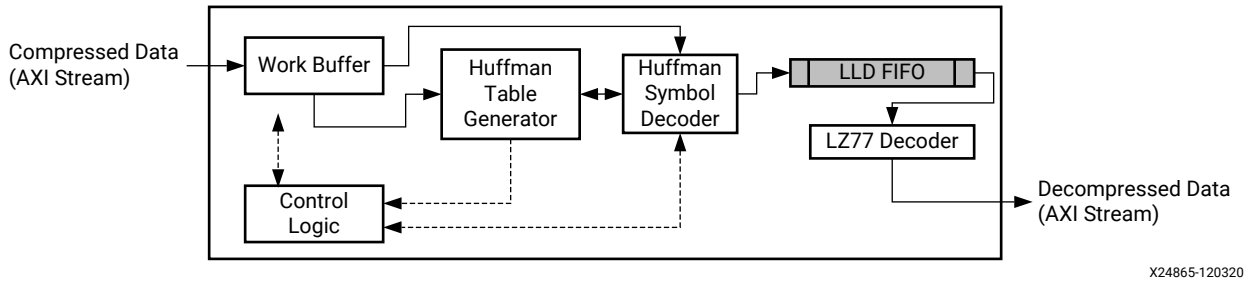
- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Product Specification

The functional block diagram of the core is shown in the following figure.

Figure 2: **Core Block Diagram**



Standards

This core adheres to the following standards:

- RFC-1950
- RFC-1951
- RFC-1952

***Note*:** This core does all the things mentioned in the RFC that a compliant decompressor must do, except for CRC32 and ADLER32 checks in case of GZIP and ZLIB compressed files respectively.

Performance and Resource Use

For full details about performance and resource use, visit the Performance and Resource Use web page.

Maximum Frequencies

The core is tested for all configurations at 250 MHz.

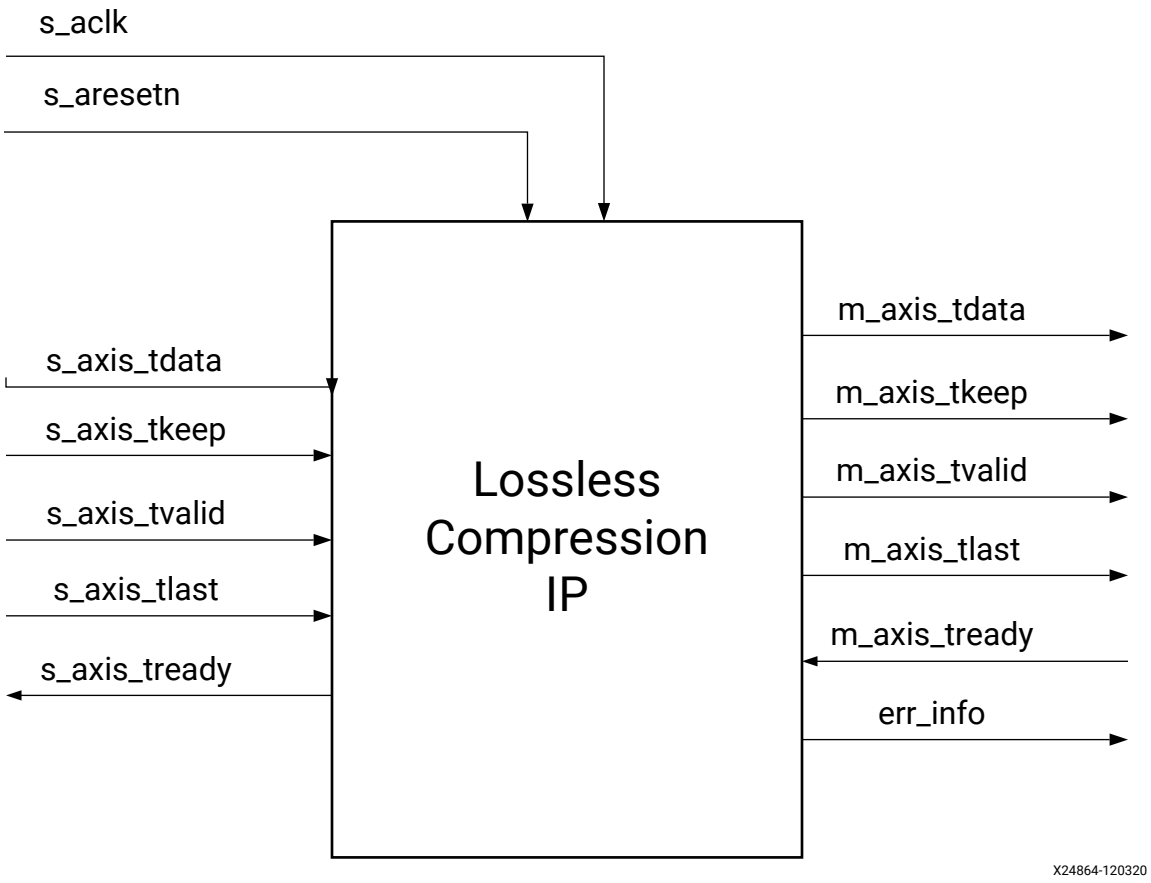
Throughput

For the Decompression function, the core does not have a constant output throughput. It varies depending on the compressed file.

Port Descriptions

The core interfaces are shown in the following figure:

Figure 3: **Core Ports**



Interface Ports

Table 1: **Lossless Compression IP Ports**

Port Name	I/O	Clock	Description
s_aclk	I	s_aclk	Clock signal for the core.
s_aresetn	I	s_aclk	Active-Low reset signal for the core.

Table 1: **Lossless Compression IP Ports** *(cont'd)*

Port Name	I/O	Clock	Description
s_axis_tdata	I	s_aclk	Input AXI4-Stream data.
s_axis_tkeep	I	s_aclk	Input AXI4-Stream signal. Indicates the bytes in the data that are valid.
s_axis_tvalid	I	s_aclk	Input AXI4-Stream data valid signal.
s_axis_tlast	I	s_aclk	Input AXI4-Stream signal. Indicates the last beat of the current packet.
s_axis_tready	O	s_aclk	Output AXI4-Stream signal. Indicates that the core is ready to consume another beat of data.
m_axis_tdata	O	s_aclk	Output AXI4-Stream data.
m_axis_tkeep	O	s_aclk	Output AXI4-Stream signal. Indicates the bytes in the data that are valid.
m_axis_tvalid	O	s_aclk	Output AXI4-Stream data valid signal.
m_axis_tlast	O	s_aclk	Output AXI4-Stream signal. Indicates the last beat of the current packet.
m_axis_tready	I	s_aclk	Input AXI4-Stream signal. Indicates that the core is ready to consume another beat of data.
err_info	O	s_aclk	This is a 2-bit port indicating error in the file header part of the compressed file passed to the IP. Bit-0 : There can be error in any part of the file header. Bit-1: This bit will go high whenever the starting part of the header is having neither GZIP nor ZLIB format.

Designing with the Core

This section includes guidelines and additional information to facilitate designing with the core.

Clocking

This core runs on a single clock through the port named s_aclk. The core is tested to meet timing at 250 MHz when measured at the IP level. Meeting the same frequency when the core is inserted into a system is subject to the system design, device congestion, and the usage of timing best practices, and other factors.

Resets

This core includes an active-Low synchronous reset signal. There are no specific requirements for reset assertion of the core.

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

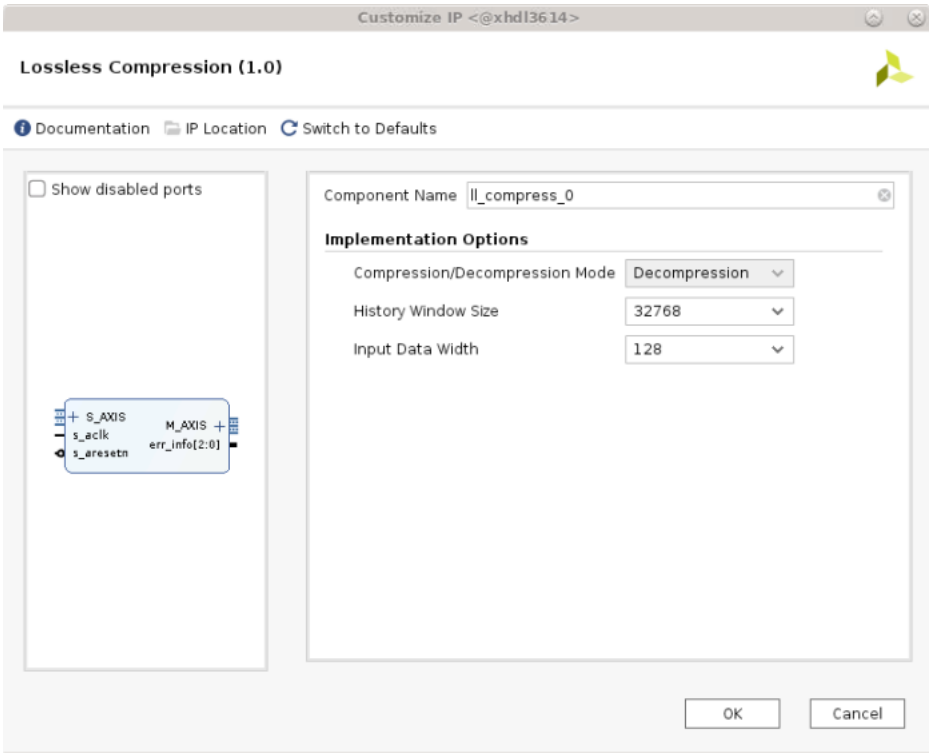
For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Parameter Tab

The Lossless Compression parameter tab is shown as following.

Figure 6: **Lossless Compression Parameter Tab**



- **Compression/Decompression Mode:** Only Decompression mode is supported currently.
- **History Window Size:** Select the suitable History Window Size from the drop-down options. Possible options for this parameter are 32768, 16384, 8192, 4096. Use the same or higher History Window Size that the input file is compressed with. If the user does not know the History Window Size used in compressing the file, use the default value of 32768.
- **Input Data Width:** Choose the suitable Input Data Width from the drop-down options. Possible options for this parameter are 512, 256, 128, 64, 32. We recommend to use the default 128-bit input data width option for optimal resource and performance.

***Note*:** Output Data Width of the Lossless Compression IP is fixed to 256-bit.

User Parameters

The following table shows the relationship between the fields in the Vivado® IDE and the user parameters (which can be viewed in the Tcl Console).

Table 2: **User Parameters**

Vivado IDE Parameter	User Parameter	Default Value
Compression/Decompression Mode	COMP_MODE	Decompression
History Window Size	HISTORY_WINDOW_SIZE	32768
Input Data Width	DIN_WIDTH	128

Notes:

1. Parameter values are listed in the table where the Vivado IDE parameter value differs from the user parameter value. Such values are shown in this table as indented below the associated parameter.
2. The parameter is disabled in GUI and you cannot change this value. This is because the Compression function is not supported in this version of the core.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Appendix B

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
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- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Debug Tools

There are many tools available to address Lossless Compression design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Simulation Debug

The signal `err_info` indicates error in the GZIP/ZLIB compressed file format. If any of the bits go high, this indicates that there is an error in the header section of the GZIP/ZLIB compressed file. If you get this error, you can reset the core and run it again with the modified compressed file. For more information on GZIP/ZLIB compressed file formats, see these links RFC-1950, RFC-1951, RFC-1952.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
12/17/2020 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

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