LogiCORE IP Local Memory Bus (LMB) v2.00b

Product Guide

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Table of Contents

SECTION I: SUMMARY

Introduction

The LMB V10 module is used as the LMB interconnect for Xilinx® FPGA-based embedded processor systems. The LMB is a fast, local bus for connecting the MicroBlaze™ processor instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).

Features

- Efficient, single master bus (requires no arbiter)
- Separate read and write data buses
- Low FPGA resource utilization

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq™-7000[2], Kintex™-7, Virtex®-7, Artix™-7, Virtex-6, Spartan-6, Virtex-5, Virtex®-4, Spartan®-3, Spartan-3E, Spartan-3A/3AN/3A DSP
Supported User Interfaces	LMB
Resources	N/A
Provided with Core	
Design Files	ISE: VHDL Vivado: RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	VHDL Behavioral
Supported S/W Driver	N/A
Tested Design Flows[3]	
Design Entry	ISE Design Suite v14.3 Vivado Design Suite v2012.3
Simulation	Mentor Graphics ModelSim Vivado Simulator
Synthesis	Xilinx Synthesis Technology (XST) Vivado Synthesis[4]
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete list of supported derivative devices, see Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
4. Supports only 7 series devices.

Overview

Functional Description

A MicroBlaze™ processor system using two LMB V10 modules is shown in Figure 1-1. This system shows the use of both I and D side LMB buses connecting to a dual-ported BRAM Block through separate LMB BRAM interface controllers.

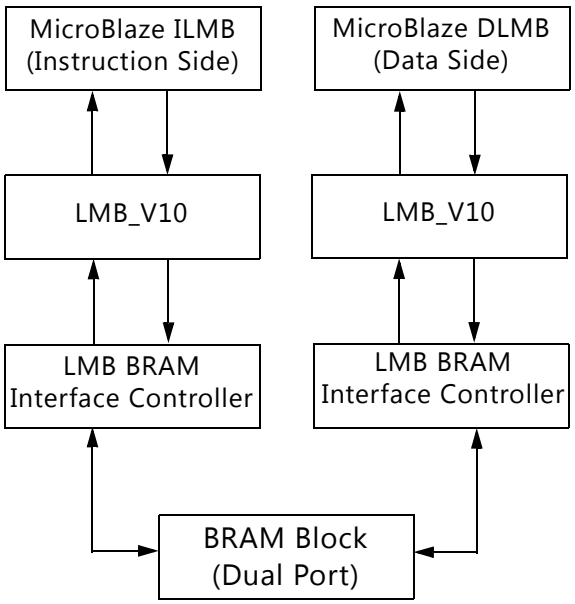

Figure 1-1: **MicroBlaze Processor System Using Two LMB V10 Modules**

Feature Summary

The LMB V10 module is used as the LMB interconnect for embedded processor systems. The LMB is a fast, local bus for connecting the MicroBlaze processor instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).

Licensing and Ordering Information

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado™ Design Suite and ISE® Design Suite Embedded Edition tools under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

The LogiCORE IP Local Memory Bus (LMB) implements the Processor Local Bus. The LMB is a synchronous bus used primarily to access on-chip block RAM. It uses a minimum number of control signals and a simple protocol to ensure that local block RAM are accessed in a single clock cycle. All LMB signals are active-High. See the *MicroBlaze Processor Reference Guide* [Ref 2], Local Memory Bus (LMB) Interface Description, for a detailed definition of the bus.

Performance

The frequency and latency of the Local Memory Bus are optimized for use with MicroBlaze™. This means that the frequency targets are aligned to MicroBlaze targets as well as the 1 cycle latency optimized for MicroBlaze instruction and data access.

Maximum Frequencies

Table 2-1 lists clock frequencies for the target families. The maximum achievable clock frequency can vary. The maximum achievable clock frequency and all resource counts can be affected by the tool flow, other tool options, additional logic in the FPGA, different versions of the Xilinx tools, and other factors.

Table 2-1: **Maximum Frequencies**

Architecture	Speed grade	Max Frequency
Spartan®-6	-4	195
Virtex®-6	-3	300
Artix™-7	-3	225
Kintex™-7	-3	320
Virtex-7	-3	320

The configuration for reaching these numbers has a single LMB master interface and interfaces to a single block RAM.

Latency

Data read from block RAM is available the clock cycle after the address strobe is asserted. Data write is performed the clock cycle after the address strobe is asserted.

Throughput

The nominal throughput is one read or write access every clock cycle.

Port Descriptions

The I/O ports for the LMB V10 module are listed in Table 2-2.

Table 2-2: **LMB V10 Module I/O Ports**

Port Name	MSB:LSB	I/O	Description
LMB_CLK		I	LMB Clock
SYS_Rst		I	External System Reset
LMB_Rst		O	LMB Reset
M_ABus	0:C_LMB_AWIDTH-1	I	Master Address Bus
M_ReadStrobe		I	Master Read Strobe
M_WriteStrobe		I	Master Write Strobe
M_AddrStrobe		I	Master Address Strobe
M_DBus	0:C_LMB_DWIDTH-1	I	Master Data Bus
M_BE	0:C_LMB_DWIDTH/8-1	I	Master Byte Enables
Sl_DBus	0:C_LMB_DWIDTH*C_LMB_NUM_SLAVES-1	I	Slave Data Bus
Sl_Ready	0:C_LMB_NUM_SLAVES-1	I	Slave Data Ready
Sl_Wait	0:C_LMB_NUM_SLAVES-1	I	Slave Data Wait
Sl_UE	0:C_LMB_NUM_SLAVES-1	I	Slave Uncorrectable Data Error
Sl_CE	0:C_LMB_NUM_SLAVES-1	I	Slave Correctable Data Error
LMB_ABus	0:C_LMB_AWIDTH-1	O	LMB Address Bus
LMB_ReadStrobe		O	LMB Read Strobe
LMB_WriteStrobe		O	LMB Write Strobe
LMB_AddrStrobe		O	LMB Address Strobe
LMB_ReadDBus	0:C_LMB_DWIDTH-1	O	LMB Read Data Bus
LMB_WriteDBus	0:C_LMB_DWIDTH-1	O	LMB Write Data Bus
LMB_Ready		O	LMB Data Ready
LMB_Wait		O	LMB Data Wait

Table 2-2: **LMB V10 Module I/O Ports *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
LMB_UE		O	LMB Uncorrectable Data Error
LMB_CE		O	LMB Correctable Data Error
LMB_BE	0:C_LMB_DWIDTH/8-1	O	LMB Byte Enables

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

In a typical MicroBlaze™ system the Local Memory Bus v10 is typically connected as in Figure 3-1.

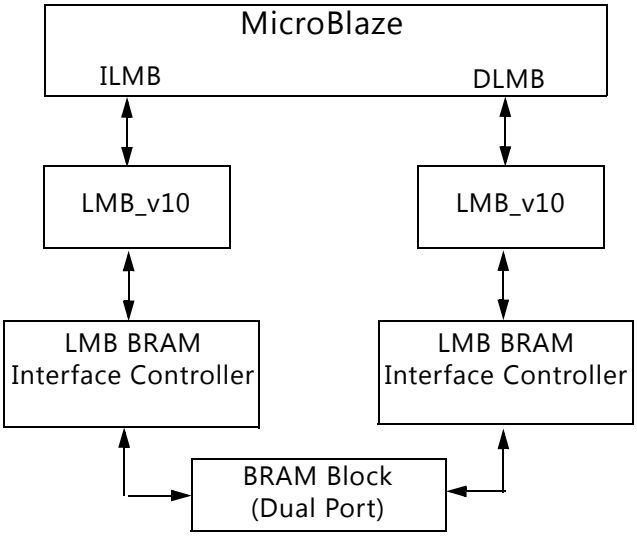

Figure 3-1: **Typical MicroBlaze System**

For additional examples, and a description of how Error Correcting Codes (ECC) is used with the Local Memory Bus, see the *LogiCORE IP LMB BRAM Interface Controller* [Ref 3].

Clocking

The Local Memory Bus is fully synchronous with all clocked elements clocked with the `LMB_Clk`.

Resets

The `LMB_Rst` is the master reset input signal for the Local Memory Bus.

Protocol Description

See the LMB Interface Description timing diagrams in the *MicroBlaze Processor Reference Guide* [Ref 2].

SECTION II: VIVADO DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado™ Design Suite environment.

GUI

The Local Memory Bus parameters are included on a single configuration page.

The LMB parameter configuration screen is shown in Figure 4-1.

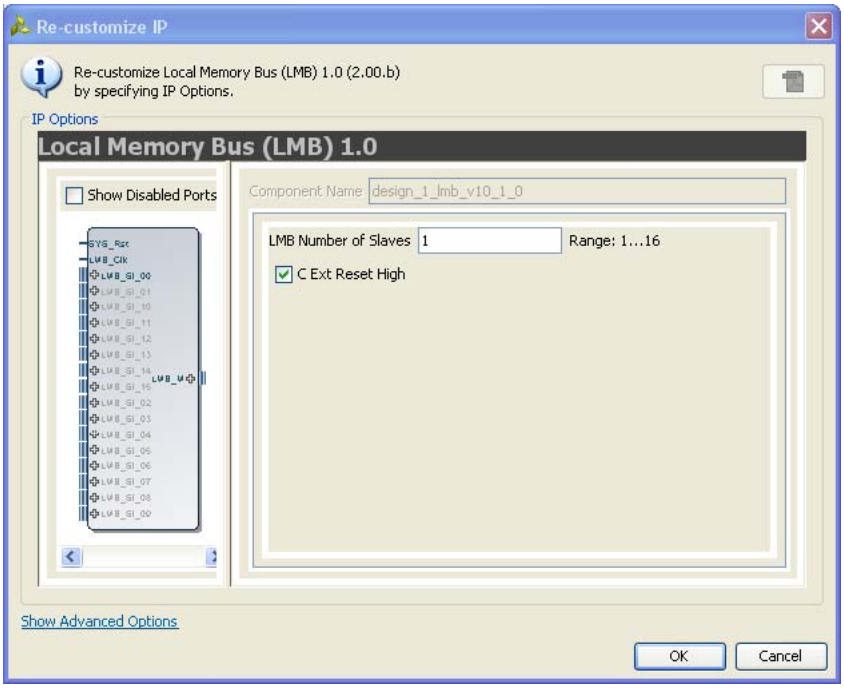

Figure 4-1: **LMB Parameter Page**

- **LMB Number of Slaves** - Sets the number of ports available to connect to MicroBlaze™.
- **C Ext Reset High** - Defines that `LMB_Rst` is active-High.

GUI Parameters

LMB Memory Bus Parameters

Table 4-1: **LMB_V10 Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_LMB_NUM_SLAVES	Number of LMB Slaves	1–16	4	integer
C_LMB_AWIDTH	LMB Address Bus Width	32	32	integer
C_LMB_DWIDTH	LMB Data Bus Width	32	32	integer
C_EXT_RESET_HIGH	Level of external reset	0 = Active-Low reset 1 = Active-High reset	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

The LMB V10 module parameter-port dependencies are listed in Table 4-2.

Table 4-2: **Parameter-Port Dependencies**

Parameter Name	Ports (Port width depends on parameter)
C_LMB_NUM_SLAVES	SI_DBus, SI_Ready. SI_Wait, SI_UE, SI_CE
C_LMB_AWIDTH	M_ABus, LMB_ABus
C_LMB_DWIDTH	M_DBus, M_BE, SI_DWIDTH, LMB_ReadDBus, LMB_WriteDBus, LMB_BE
C_EXT_RESET_HIGH	none

Constraining the Core

This chapter contains information about constraining the core in the Vivado™ Design Suite environment.

Required Constraints

There are no required constraints for this core.

Device, Package, and Speed Grade Selections

There are no Device, Package or Speed Grade requirements for this core.

Clock Frequencies

There are no specific clock frequency requirements for this core.

Clock Management

The Local Memory Bus is fully synchronous with all clocked elements clocked by the `LMB_Clk` input.

To operate properly when connected to MicroBlaze™, the `LMB_Clk` must be the same as MicroBlaze clock.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

SECTION III: ISE DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the ISE® Design Suite environment.

GUI

The Local Memory Bus parameters are included on a single configuration tab.

The LMB parameter System tab is shown in Figure 6-1.

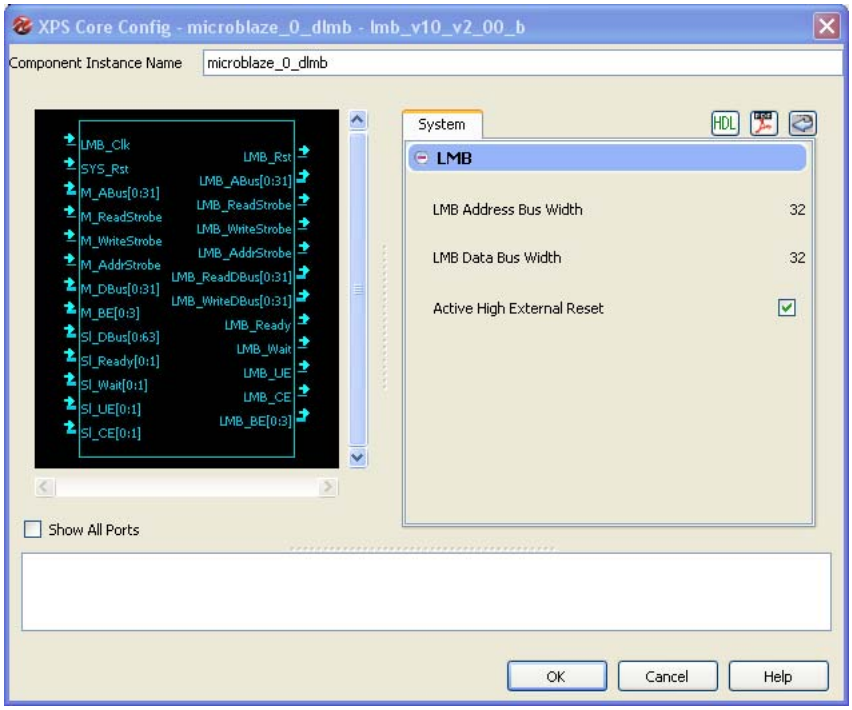

Figure 6-1: **System Parameter Tab**

- **LMB Address Bus Width** - Shows the LMB address bus width (fixed to 32).
- **LMB Data Bus Width** - Shows the LMB address bus width (fixed to 32).
- **Active High External Reset** - Defines that `LMB_Rst` is active-High.

Parameters

See SECTION II: VIVADO DESIGN SUITE, Chapter 4, Customizing and Generating the Core.

Design Implementation

The LMB V10 module design is hand written. The NGC netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Constraining the Core

See SECTION II: VIVADO DESIGN SUITE,Chapter 5, Constraining the Core.

SECTION IV: APPENDICES

Migrating

Debugging

Additional Resources

Appendix A

Migrating

This appendix describes migrating from older versions of the IP to the current IP release.

For information on migrating to the Vivado™ Design Suite, see the *Vivado Design Suite Migration Methodology Guide* [Ref 4].

Debugging

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Appendix C

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

1. Vivado™ Design Suite user documentation
2. MicroBlaze Processor Reference Guide (UG081)
3. LogiCORE IP LMB BRAM Interface Controller product guide (PG061)
4. Vivado™ Design Suite Migration Methodology Guide (UG911)

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/16/12	1.0	Initial Xilinx release. This Product Guide is derived from DS445. Vivado support added for 2012.3.

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