LogiCORE IP LTE RACH Detector v2.0

XMP041 (v2.0) April 2, 2014 **Product Brief**

Introduction

The Xilinx LogiCORE™ IP LTE RACH Detector core decodes PRACH data encoded according to the 3GPP TS 36.211 v9.0 (2009-12) Physical Channels and Modulation specification.

Additional Documentation

A full product guide is available for this core. Access to this material may be requested by clicking on this registration link:
www.xilinx.com/member/lte_rach_detector_eval/index.htm

Features

- Channel detection for 3GPP TS 36.211 v9.0.0 (2009-12)
- Supports Formats 0-4
- Supports up to 64 roots
- Supports up to 4 antennas
- Supports Multiplexing in Frequency, for up to 6 frequency channels
- Supports 5, 10, 15 and 20 MHz Bandwidth.
- C model available for the core
- Fully optimized for speed and area
- Fully synchronous design using a single clock

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	UltraScale™ Architecture, Zynq®-7000 All Programmable SoC, 7 Series
Supported User Interfaces	Native(2)
Provided with Core	
Documentation	Product Brief Product Guide
Design Files	VHDL and Netlist(3)
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	C Model(3)
Tested Design Tools(4)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. Interface similar to AXI and can be connected to an AXI4-Stream Interface.
3. Design files and C model available on the product page on Xilinx.com at http://www.xilinx.com/products/intellectual-property/EF-DI-RACH-LTE.htm
4. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The LTE RACH detector core provides a RACH detection solution for the 3GPP TS 36.211 v9.0.0 (2009-12) specification. The LTE RACH detector searches through the received antenna samples and correlates against one or more (up to 64) RACH preamble sequences. The sequences are generated from Zadoff-Chu sequences, as defined in section 5.7 of 3GPP TS 36.211 v9.0.0 (2009-12).

At the eNode-B, the correlation results from the RACH detector are used to detect UE access attempts and compute/update UE transmission timing advance to ensure that the signals received from all UEs are time synchronized within the cyclic prefix (CP).

The RACH detector core performs a cyclic correlation for each Zadoff-Chu root it is configured to detect. This identifies all of the peaks resulting from each cyclic shifted copy of the root.

The architecture has been designed to provide efficient use of the FPGA. All processing-intensive and timing-critical operations are performed by the FPGA. The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

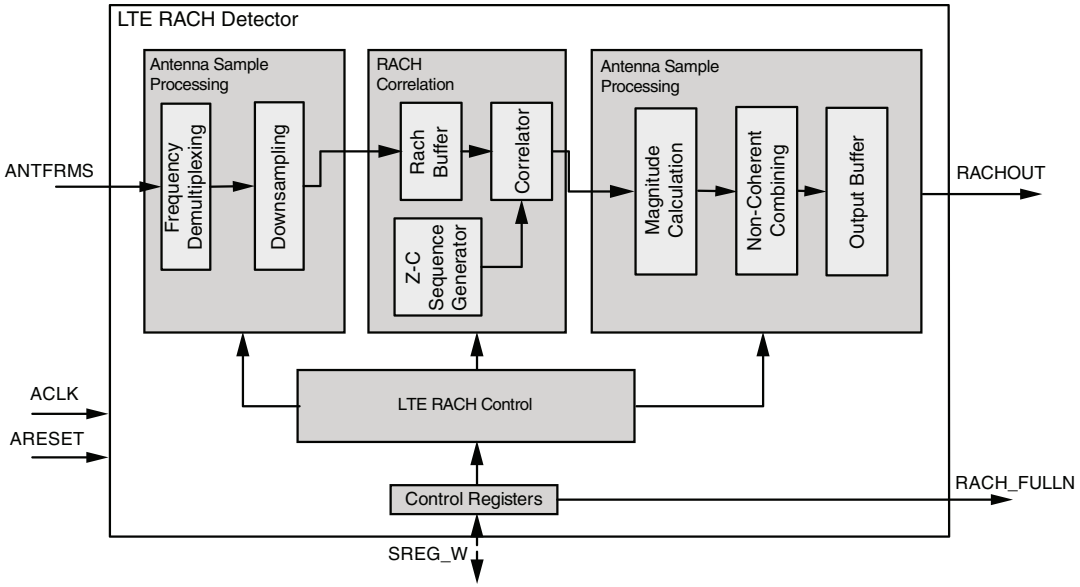

Figure 1: **internal Structure of the LTE RACH Detector Core**

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Licensing and Ordering Information

The LTE RACH detector core is provided under the SignOnce IP Site License and can be generated using the Xilinx Vivado Design Suite.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE RACH Detector product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/02/2014	2.0	Characterization data link added to PG130.
12/18/2013	2.0	Added UltraScale™ architecture support.
03/20/2013	2.0	Updated for Vivado tools.
08/15/2011	1.2	Updated to include web registration information.
06/22/2011	1.1	Added new family support; ISE Design Suite 13.2.
04/19/2010	1.0	Initial Xilinx release.

Please Read: Important Legal Notices