MCH OPB Double Data Rate (DDR) Synchronous DRAM (SDRAM) Controller

DS496 November 15, 2005

Product Specification

Introduction

The Xilinx Multi-CHannel (MCH) On-chip Peripheral Bus (OPB) Double Data Rate Synchronous DRAM (SDRAM) controller for Xilinx FPGAs provides a DDR SDRAM controller which connects to the OPB and multiple channel interfaces and provides the control interface for DDR SDRAMs. It is assumed that the reader is familiar with DDR SDRAM and MicroBlaze.

Features

The Xilinx MCH OPB DDR SDRAM Controller is a soft IP core designed for Xilinx FPGAs and contains the following features:

- Parameterizable number of channel (MCH) interfaces that can be configured with the Xilinx Cachelink (XCL) protocol (see "Reference Documents" on page 36)
- Optional OPB interface
- Performs device initialization sequence upon power-up and reset conditions for ~200uS. Provides a parameter to adjust this time for simulation purposes only.
- Performs auto-refresh cycles
- Supports DDR SDRAM self refresh mode
- Supports CAS latencies of 2 or 3 set by a design parameter
- Supports target word first XCL cacheline transactions of 1, 4, 8, and 16 words
- Supports 16, 32 and 64-bits DDR data widths set by a design parameter
- Supports indeterminate burst length
- Provides big-endian connections to memory devices. See Connecting to Memory for details on memory connections
- Supports multiple (up to 4) DDR memory banks
- Allows DDR SDRAM open row management set by a design parameter
- Supports capability to separate DDR clock domain from the MCH/OPB bus clock domain set by a design parameter for the following frequency combinations (for supported simulation values, see Table 9,10, and 11):
  - MCH/OPB clock: 50 MHz & DDR clock: 100 MHz
  - MCH/OPB clock: 66 MHz & DDR clock: 133 MHz

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Virtex-II, Virtex-II Pro, Virtex-4, Spartan™-3	
Version of Core	mch_opb_ddr	v1.00b
Resources Used		
	Min	Max
Slices	Please refer to Table 9 on page 33, Table 10 on page 34, and Table 11 on page 35.	
LUTs		
FFs		
Block RAMs		
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 7.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.8b or later	
Synthesis	XST 7.1i or later	
Support		
Support provided by Xilinx, Inc.		

MCH OPB DDR SDRAM Controller Design Parameters

To allow the user to obtain a MCH OPB DDR SDRAM Controller that is uniquely tailored for their system, certain features are parameterizable in the MCH OPB DDR SDRAM Controller design. This allows the user to have a design that only utilizes the resources required by their system and runs at the best possible performance. The features that are parameterizable in the MCH OPB DDR SDRAM Controller are shown in Table 1.

Table 1: **MCH OPB DDR SDRAM Controller Design Parameters**

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
DDR SDRAM Controller Features	G1	Target FPGA family	C_FAMILY	virtex2, virtex2p, spartan3, virtex4	virtex2p	string
	G2	Include support for registered DIMM	C_REG_DIMM	0 = DDR device is not registered DIMM 1 = DDR device is registered DIMM	0	integer
	G3	Supported number of DDR SDRAM memory banks(1)	C_NUM_BANKS_MEM	1 - 4	1	integer
	G4	Number of generated DDR clock pairs	C_NUM_CLK_PAIRS	1 - 4	1	integer
	G5	Include logic to support asynchronous DDR SDRAM clock from OPB bus clock	C_DDR_ASYNC_SUPPORT	0 = don't include support 1 = include logic to support asynchronous DDR SDRAM clock	0	integer
	G6	Include support for extra set up time on certain DDR control signals(2)	C_EXTRA_TSU	0 = don't include support 1 = include logic to support extra setup time	0	integer
	G7	Allow DDR SDRAM open row management capability	C_USE_OPEN_ROW_MNGT	0 = don't allow open row management 1 = use open row management	0	integer
	G8	For improved frequency performance, include DDR pipeline stage	C_INCLUDE_DDR_PIPE	0 = don't include 1 = include extra DDR pipeline stage	1	integer
	G9	Include OPB Slave Interface	C_INCLUDE_OPB_IPIF	0 = don't include OPB IPIF 1 = include OPB IPIF	1	integer

Table 1: **MCH OPB DDR SDRAM Controller Design Parameters *(Continued)***

Grouping / Number	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
	G10	Include logic to support OPB bursts	C_INCLUDE_OPB_BURST_SUPPORT	0 = don't include logic to support OPB bursts 1 = include logic to support OPB bursts	0	integer
	G11	Arbitration mode between OPB and MCH interfaces	C_PRIORITY_MODE	0 = fixed priority mode	0	integer
	G12	Data bus width for MCH and OPB (if included in design)	C_MCH_OPB_DWIDTH	32	32	integer
	G13	Address bus width for MCH and OPB (if included in design)	C_MCH_OPB_AWIDTH	32	32	integer
	G14	Clock period (ps)	C_MCH_OPB_CLK_PERIOD_PS			integer
DDR SDRAM Device Features	G15	Load Mode Register command cycle time (ps)	C_DDR_TMRD		15000	integer
	G16	Write Recovery Time (ps)	C_DDR_TWR		15000	integer
	G17	Write-to-Read Command Delay (Tck)	C_DDR_TWTR		1	integer
	G18	Delay after ACTIVE command before PRECHARGE command (ps)	C_DDR_TRAS		40000	integer
	G19	Delay after ACTIVE command before another ACTIVE or AUTOREFRESH command (ps)	C_DDR_TRC		65000	integer
	G20	Delay after AUTOREFRESH before another command (ps)	C_DDR_TRFC		75000	integer
	G21	Delay after ACTIVE command before READ/WRITE command (ps)	C_DDR_TRCD		20000	integer

Table 1: **MCH OPB DDR SDRAM Controller Design Parameters *(Continued)***

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
	G22	Delay after ACTIVE command for a row before an ACTIVE command for another row (ps)	C_DDR_TRRD		15000	integer
	G23	Delay after a PRECHARGE command (ps)	C_DDR_TRP		20000	integer
	G24	Average periodic refresh command interval (ps)	C_DDR_TREFI		7800000	integer
	G25	Self refresh exit delay before issuing an ACTIVE command	C_DDR_TXSR		80000	integer
	G26	CAS Latency	C_DDR_CAS_LAT	2,3	2	integer
DDR SDRAM Device Features (cont.)	G27	Cumulative data width of DDR devices	C_DDR_DWIDTH	16, 32, 64	16	integer
	G28	DDR address width	C_DDR_AWIDTH	See note(3)	13	integer
	G29	DDR column address width	C_DDR_COL_AWIDTH	See note(3)	9	integer
	G30	DDR bank address width	C_DDR_BANK_AWIDTH	See note(3)	2	integer
Address Space	G31	Base Address for Memory Bank x (x = 0 to 3)	C_MEMx_BASEADDR	Valid address(4,5)		std_logic_vector
	G32	High Address for Memory Bank x (x = 0 to 3)	C_MEMx_HIGHADDR	Valid address(4,5)		std_logic_vector
Simulation Only	G39	DDR Initialization time for simulation(6)	C_SIM_INIT_TIME_PS	Minimum 200 clock periods	2000000000	integer

Table 1: **MCH OPB DDR SDRAM Controller Design Parameters *(Continued)***

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
MCH Interface		Number of MCH channels	C_NUM_CHANNELS	1-4	2	integer
		MCH protocol (7,8)	C_MCHx_PROTOCOL	0 = XCL protocol (see "Reference Documents" on page 36)	0	integer
		Depth of MCH access buffer (7,9)	C_MCHx_ACCESSBUF_DEPTH	4, 8, 16	16	integer
		Depth of MCH readdata buffer (7,10)	C_MCHx_RDDATABUF_DEPTH	0, 4, 8, 16	16	integer
		Cacheline size (in number of 32-bit words) (7)	C_XCLx_LINESIZE	1, 4, 8, 16	4	integer
		Write transfer type(7,11)	C_XCLx_WRITE_XFER	0 = no write transfers 1 = single transfers only 2 = cacheline transfers only	1	integer
		Include timeout counter	C_INCLUDE_TIMEOUT_CNTR	0 = don't include an acknowledge timeout counter	0	integer
		Number of clocks to wait for transfer acknowledge from the DDR controller before issuing a timeout error	C_TIMEOUT	1 - 512	16	integer

Table 1: **MCH OPB DDR SDRAM Controller Design Parameters *(Continued)***

Grouping / Number	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type

Notes:

1. C_NUM_BANKS_MEM specifies the number of DDR SDRAM memory banks with identical device characteristics. All the DDR SDRAM device characteristics specified in parameters, G13 through G28, are applicable for all memory banks. The C_NUM_BANKS_MEM parameter specifies the size of the DDR_CSn signal(s).
2. C_EXTRA_TSU generic is don't care when generic C_REG_DIMM=1. When C_EXTRA_TSU=1 it enables extra setup time on the following signals: DDR_CSn, DDR_RASn, DDR_CASn, DDR_WEn, DDR_BankAddr, DDR_Addr. Setting C_EXTRA_TSU=1 is useful for certain memory board applications with high input capacitance on DDR control signals.
3. C_DDR_AWIDTH + C_DDR_COL_AWIDTH + C_DDR_BANK_AWIDTH + log2(C_DDR_DWIDTH/8) must be < C_MCH_OPB_AWIDTH-1.
4. This design can accommodate up to 4 banks of DDR memory. The address range generics are designated as C_MEM0_BASEADDR, C_MEM1_BASEADDR, C_MEM0_HIGHADDR, C_MEM1_HIGHADDR, etc.
5. The range specified by C_MEMx_BASEADDR and C_MEMx_HIGHADDR must comprise a complete, contiguous power of two range such that range = 2^m, and the m least significant bits of C_MEMx_BASEADDR must be zero.
6. This parameter adjusts the initialization time of the DDR for simulation only. Must be > 200 clocks
7. This design can accommodate up to 4 channels. The generics associated with the MCH interfaces are designated with a C_MCHx_ prefix where x indicates the channel number and must be value between 0 and 3.
8. C_MCHx_PROTOCOL = 0 (or XCL, Xilinx Cachelink) is the only supported protocol.
9. The depth of the MCH access buffer (C_MCHx_ACCESSBUF_DEPTH) must be large enough to hold a cacheline write. C_MCHx_ACCESSBUF_DEPTH >= C_XCLx_LINESIZE for optimal performance.
10. If the master connected to the MCH interface can consume data as soon as it is available (i.e., instruction cache masters) the ReadData buffer depth can be set to zero to save resources and eliminate extra latency. Otherwise, the ReadData buffer depth must be sized to accommodate any latency the master may have in reading data from this buffer.
11. If the master connecting to the channel x will only perform read transfers (i.e., instruction cache masters) set C_XCLx_WRITE_XFER=0 to save resources.

Allowable Parameter Combinations

The MCH OPB DDR SDRAM controller supports up to 4 banks of memory. Each bank of memory has its own independent base address and address range. Each address range specified by C_MEMx_BASEADDR and C_MEMx_HIGHADDR must comprise a complete, contiguous power of two range such that range = 2^m, and the m least significant bits of C_MEMx_BASEADDR must be zero. The range specified by these parameters should not exceed the MCH OPB DDR SDRAM memory space.

The OPB slave interface is only included in this design if C_INCLUDE_OPB_IPIF = 1. When C_INCLUDE_OPB_IPIF = 0, the C_INCLUDE_OPB_BURST_SUPPORT is unused.

Optimal MCH Parameter Settings

If an XCL channel is connected to a master that will only perform read transactions, then C_XCLx_WRITEXFER should be set to 0 indicating that no write transfers will be performed. This will reduce the channel logic to only contain logic for read transactions.

If an XCL channel is connected to a master that can consume data as soon as its available, then C_MCHx_RDDATABUF_DEPTH for that channel should be set to 0. This will eliminate the read data buffer and eliminate the latency that would normally exist in reading data from this buffer. If the master can not consume data as soon as its available, then C_MCHx_RDDATABUF_DEPTH for that channel should be set to accommodate any latency the master has in reading data from the ReadData Buffer.

Optimal performance will be achieved when the buffer depth of the Access Buffer is set greater than or equal to the line size of the channel (C_MCHx_ACCESSBUF_DEPTH >= C_XCLx_LINESIZE).

MCH OPB DDR SDRAM Controller I/O Signals

Table 2 provides a summary of all MCH OPB DDR SDRAM Controller input/output (I/O) signals, the interfaces under which they are grouped, and a brief description of the signals.

Table 2: **MCH OPB DDR SDRAM Controller Pin Descriptions**

Grouping		Signal Name	Interface	I/O	Initial State	Description
DDR SDRAM Signals	P1	DDR_Clk [0:C_NUM_CLK_PAIRS-1]	DDR	O	0	DDR Clock(1)
	P2	DDR_Clkn [0:C_NUM_CLK_PAIRS-1]	DDR	O	1	DDR inverted clock
	P3	DDR_CKE [0:C_NUM_BANKS_MEM-1]	DDR	O	0	DDR clock enable(s)
	P4	DDR_CSn [0:C_NUM_BANKS_MEM-1]	DDR	O	1	Active low DDR chip select(s)
	P5	DDR_RASn	DDR	O	1	Active low DDR row address strobe
	P6	DDR_CASn	DDR	O	1	Active low DDR column address strobe
	P7	DDR_WEn	DDR	O	1	Active low DDR write enable
	P8	DDR_DM[0:C_DDR_DWIDTH/8-1]	DDR	O	0	DDR data mask
	P9	DDR_BankAddr[0:C_DDR_BANK_AWIDTH-1]	DDR	O	0	DDR bank address
	P10	DDR_Addr[0:C_DDR_AWIDTH-1]	DDR	O	0	DDR address
	P11	DDR_DQ_o[0:C_DDR_DWIDTH-1]	DDR	O	0	Output data to DDR
	P12	DDR_DQ_i[0:C_DDR_DWIDTH-1]	DDR	I		Input data from DDR
	P13	DDR_DQ_t[0:C_DDR_DWIDTH-1]	DDR	O	0	3-state control for DDR data buffers
	P14	DDR_DQS_o[0:C_DDR_DWIDTH/8-1]	DDR	O	0	Output data strobe to DDR
	P15	DDR_DQS_i[0:C_DDR_DWIDTH/8-1]	DDR	I		Input data strobe from DDR
	P16	DDR_DQS_t[0:C_DDR_DWIDTH/8-1]	DDR	O	1	3-state control for DDR data strobe buffers
	P24	DDR_Init_done	DDR	O	0	Signals that the DDR initialization is complete
Clock Signals	P25	Device_Clk	CLK	I		DDR device clock. It can be MCH_OPB_Clk or an external clock.
	P26	Device_Clk_n	CLK	I		DDR device clock phase shifted by 180 degrees.
	P27	Device_Clk90_in	CLK	I		DDR device clock phase shifted by 90 degrees
	P28	Device_Clk90_in_n	CLK	I		DDR device clock phase shifted by 270 degrees
	P29	DDR_Clk90_in		I		DDR clock feedback shifted by 90 degrees
	P30	DDR_Clk90_in_n		I		DDR clock feedback shifted by 270 degrees

Table 2: **MCH OPB DDR SDRAM Controller Pin Descriptions *(Continued)***

Grouping		Signal Name	Interface	I/O	Initial State	Description
OPB Slave Signals(2)	P27	OPB_Select	OPB	I		OPB select
	P28	OPB_RNW	OPB	I		OPB read,not write
	P29	OPB_ABus[0:C_OPB_AWIDTH-1]	OPB	I		OPB address bus
	P30	OPB_DBus[0:C_OPB_DWIDTH-1]	OPB	I		OPB data bus
	P31	OPB_BE[0:C_OPB_DWIDTH/8-1]	OPB	I		OPB byte enables
	P32	OPB_seqAddr	OPB	I		OPB sequential address
	P33	Sl_xferAck	OPB	O	0	OPB DDR SDRAM Controller transfer acknowledge
	P34	Sl_errAck	OPB	O	0	OPB DDR SDRAM Controller error acknowledge
	P35	Sl_toutSup	OPB	O	0	OPB DDR SDRAM Controller timeout suppress
	P36	Sl_retry	OPB	O	0	OPB DDR SDRAM Controller retry
	P37	Sl_DBus[0:C_OPB_DWIDTH-1]	OPB	O	0	OPB DDR SDRAM Controller OPB slave data bus

Table 2: **MCH OPB DDR SDRAM Controller Pin Descriptions *(Continued)***

Grouping		Signal Name	Interface	I/O	Initial State	Description
MCH Signals		MCH_OPB_Clk	MCH	I		MCH/OPB clock
		MCH_OPB_Rst	MCH	I		MCH/OPB reset
		MCHx_Access_Control (x = 0 to 3)	MCH	I		Control signal to the Access buffer of MCH interface x (x = 0 to 3). This signal indicates the type of access to be performed (read or write) and the size of the access (byte, halfword, or word).
		MCHx_Access_Data(0:C_MCH_OPB_DWIDTH-1) (x = 0 to 3)	MCH	I		Write Data to the Access buffer of MCH interface x (x = 0 to 3).
		MCHx_Access_Write (x = 0 to 3)	MCH	I		Write signal to the Access buffer of MCH interface x (x = 0 to 3).
		MCHx_Access_Full (x = 0 to 3)	MCH	O	0	Indicator that the Access buffer of MCH interface x is full (x = 0 to 3).
		MCHx_ReadData_Control (x = 0 to 3)	MCH	O	1	Control signal for the ReadData buffer of MCH interface x (x = 0 to 3). This signal indicates if the data from the ReadData buffer is valid.
		MCHx_ReadData_Data(0:C_MCH_OPB_DWIDTH-1) (x = 0 to 3)	MCH	O	Zeros	Read data from the ReadData buffer of MCH interface x (x = 0 to 3).
		MCHx_ReadData_Read (x = 0 to 3)	MCH	I		Read signal to the ReadData buffer of MCH interface x (x = 0 to 3).
		MCHx_ReadData_Exists (x = 0 to 3)	MCH	O	0	Indicator that the ReadData buffer of MCH interface x is non-empty (x = 0 to 3).

Table 2: **MCH OPB DDR SDRAM Controller Pin Descriptions *(Continued)***

Grouping		Signal Name	Interface	I/O	Initial State	Description
System		DDR_Sleep	System	I		Rising edge on this signal enters the DDR SDRAM self refresh mode. A minimum period of 50uS after the assertion of DDR_Sleep is required before MCH_OPB_Rst can be asserted.
		DDR_WakeUp	System	I		This signal indicates whether the DDR SDRAM must go through the power-up initialization after reset, or if only the sequence to exit the self refresh mode needs to be executed. This signal is sampled when reset negates and therefore should be asserted XXX before MCH_OPB_Rst negates.

Notes:
1. DDR_Clk is the same frequency as MCH_OPB_Clk or Device_Clk depending on design parameter, C_DDR_ASYNC_SUPPORT.
2. Please refer to the IBM OPB Architecture Specification for more detailed information on these signals.

Parameter-Port Dependencies

The dependencies between the MCH OPB DDR SDRAM controller design parameters and I/O signals are shown in Table 3. It gives the information about how the ports and parameters get affected by changing certain parameters.

Table 3 shows when certain features are parameterized away, the related logic will be part of design and signals are unconnected and the related output signals are set to a constant value.

Table 3: **Parameter-Port Dependencies**

Grouping		Parameter	Affects	Depends	Description
Design Parameters	G3	C_NUM_BANKS_MEM	P3, P4		Specifies the number of DDR SDRAM memory banks
	G4	C_NUM_CLK_PAIRS	P1, P2		Number of generated DDR clock pairs
	G27	C_DDR_DWIDTH	P8, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P63	G6	
	G6	C_EXTRA_TSU		G2	C_EXTRA_TSU = 1 is valid only when C_REG_DIMM = 0
I/O Signals	P1	DDR_Clk [0:C_NUM_CLK_PAIRS-1]		G4	DDR clock(s)
	P2	DDR_Clkn [0:C_NUM_CLK_PAIRS-1]		G4	DDR clock(s) shifted by 180 degrees
	P3	DDR_CKE [0:C_NUM_BANKS_MEM-1]		G3	DDR clock enable(s)
	P4	DDR_CSn [0:C_NUM_BANKS_MEM-1]		G3	Active low DDR SDRAM chip select(s)
	P8	DDR_DM[0:C_DDR_DWIDTH/8-1]		G27	DQ mask
	P11	DDR_DQ_o[0:C_DDR_DWIDTH-1]		G27	DQ output
	P12	DDR_DQ_i[0:C_DDR_DWIDTH-1]		G27	DQ input
	P13	DDR_DQ_t[0:C_DDR_DWIDTH-1]		G27	3-state enable for DQ
	P14	DDR_DQS_o[0:C_DDR_DWIDTH/8-1]		G27	Data qualifier strobe output
	P15	DDR_DQS_i[0:C_DDR_DWIDTH/8-1]		G27	Data qualifier strobe input
	P16	DDR_DQS_t[0:C_DDR_DWIDTH/8-1]		G27	Data qualifier strobe 3-state

Connecting to Memory

Memory Data Types and Organization

MCH OPB DDR SDRAM memory can be accessed as byte (8 bits), halfword (2 bytes), word (4 bytes) or Double word (8 bytes) depending on the size of the bus to which the processor is attached. From the point of view of the MCH OPB, data is organized as big-endian. The bit and byte labeling for the big-endian data types is shown below in Figure 1.

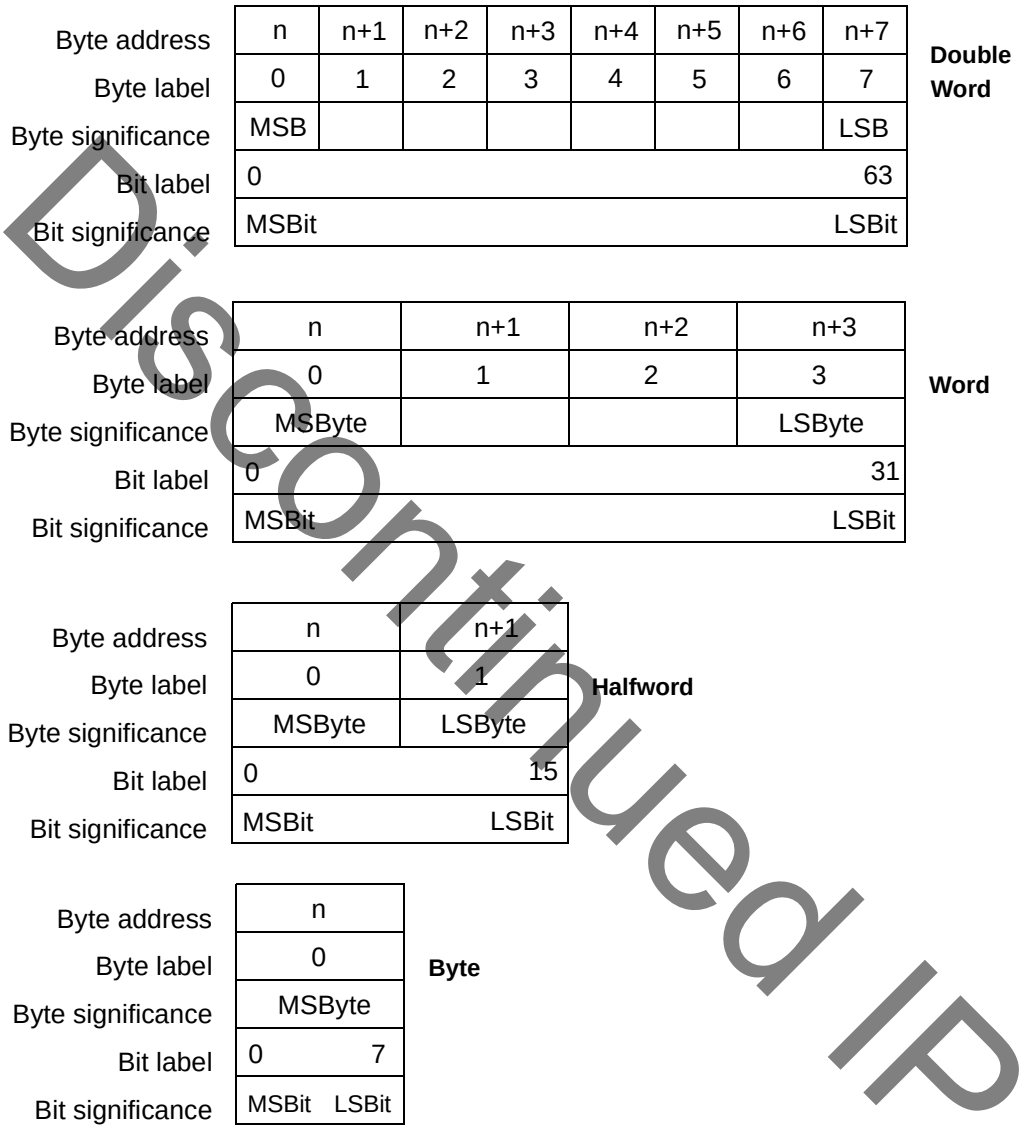


Figure 1: **Big-Endian Data Types**

Memory to MCH OPB DDR SDRAM Controller Connections

The data and address signals at the MCH OPB DDR SDRAM controller are labeled with big-endian bit labeling (for example, D(0:31), D(0) is the MSB), whereas most memory devices are either endian agnostic (they can be connected either way) or little-endian D(31:0) with D(31) as the MSB.

Caution must be exercised with the connections to the external memory devices to avoid incorrect data and address connections.

Table 4 shows the correct mapping of MCH OPB DDR SDRAM controller pins to memory device pins.

Table 4: **MCH OPB DDR SDRAM controller to memory interconnect**

Description	DDR SDRAM Controller Signal (MSB:LSB)	Memory Device Signal (MSB:LSB)
Data Bus	DDR_DQ(0:C_DDR_DWIDTH-1)	DQ(C_DDR_DWIDTH-1:0)
Bank Address	DDR_BankAddr(0:C_DDR_BANK_AWIDTH-1)	BA(C_DDR_BANK_AWIDTH-1:0)
Address	DDR_Addr(0:C_DDR_AWIDTH-1)	A(C_DDR_AWIDTH-1:0)
Data Strobe	DDR_DQS(0:C_DDR_DWIDTH/8-1)	UDQS, LDQS
Data Mask	DDR_DM(0:C_DDR_DWIDTH/8-1)	UDM, LDM

Example 1: 32-bit Connection

Figure 2 illustrates an example of connecting memory to the MCH OPB DDR SDRAM controller design. The example shown here has the following specified parameters:

- C_NUM_BANKS_MEM=1
- C_DDR_DWIDTH = 32
- C_DDR_BANK_AWIDTH = 2
- C_DDR_AWIDTH = 13

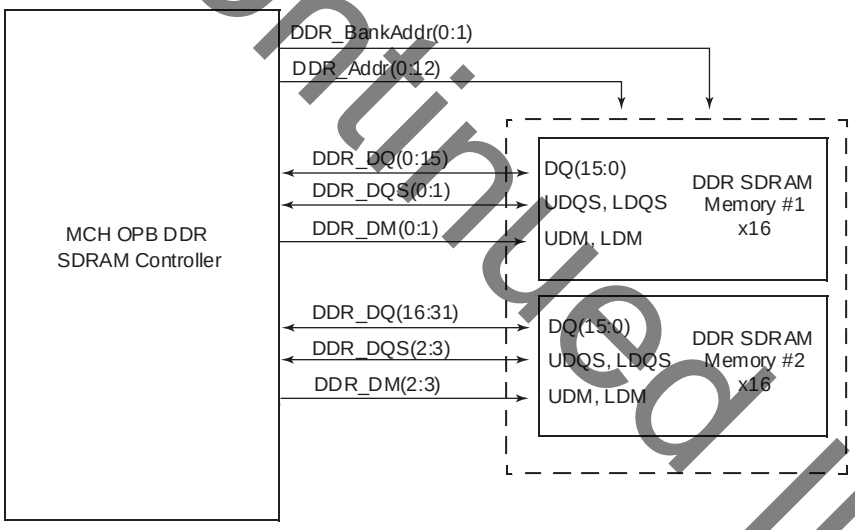


Figure 2: **32-bit Memory Connection Example**

DDR Address Mapping

An address offset is calculated based on the width of the DDR data bus. The DDR column address is then mapped from the MCH OPB address bus, followed by the bank address and row address.

The MCH OPB address bus bit locations for the DDR column, row, and bank addresses are calculated as shown in Table 5 and Table 6.

Table 5: **DDR Address offset calculations**

Variable	Equation
ADDR_OFFSET	log2(C_DDR_DWIDTH/8)
COLADDR_STARTBIT	C_MCH_OPB_AWIDTH - (C_DDR_COL_AWIDTH+ADDR_OFFSET)
COLADDR_ENDBIT	COLADDR_STARTBIT + C_DDR_COL_AWIDTH- 2 (A0 is not used)
BANKADDR_STARTBIT	COLADDR_STARTBIT - C_DDR_BANK_AWIDTH
BANKADDR_ENDBIT	BANKADDR_STARTBIT + C_DDR_BANK_AWIDTH-1
ROWADDR_STARTBIT	BANKADDR_STARTBIT - C_DDR_AWIDTH
ROWADDR_ENDBIT	ROWADDR_STARTBIT + C_DDR_AWIDTH-1

Table 6: **DDR - Address Bus Assignments**

DDR Address	Address Bus
Column Address	MCH_OPB_ABus(COLADDR_STARTBIT to COLADDR_ENDBIT) & '0'
Bank Address	MCH_OPB_ABus(BANKADDR_STARTBIT to BANKADDR_ENDBIT)
Row Address	MCH_OPB_ABus(ROWADDR_STARTBIT to ROWADDR_ENDBIT)

Table 7 and Table 8 show an example of the mapping between the MCH or OPB address and the DDR address when the data width of the DDR is 16 and the data width of the MCH/OPB bus is 32, the column address width is 9, the row address width is 13, and the bank address width is 2.

Table 7: **MCH OPB Example DDR Address offset calculations**

Variable	Value
ADDR_OFFSET	log2(16/8) = 1
COLADDR_STARTBIT	32 - (9+1) = 22
COLADDR_ENDBIT	22 + (9-2)= 29
BANKADDR_STARTBIT	22 - 2 = 20
BANKADDR_ENDBIT	20+ 2 -1 = 21
ROWADDR_STARTBIT	20 - 13 = 7
ROWADDR_ENDBIT	7 + 13 -1 = 19

Table 8: **DDR to MCH OPB Address Bus Assignments**

DDR Address	MCH or OPB Address Bus
Column Address	MCH_OPB_ABus(22: 29) & '0'
Bank Address	MCH_OPB_ABus(20:21)
Row Address	MCH_OPB_ABus(7:19)

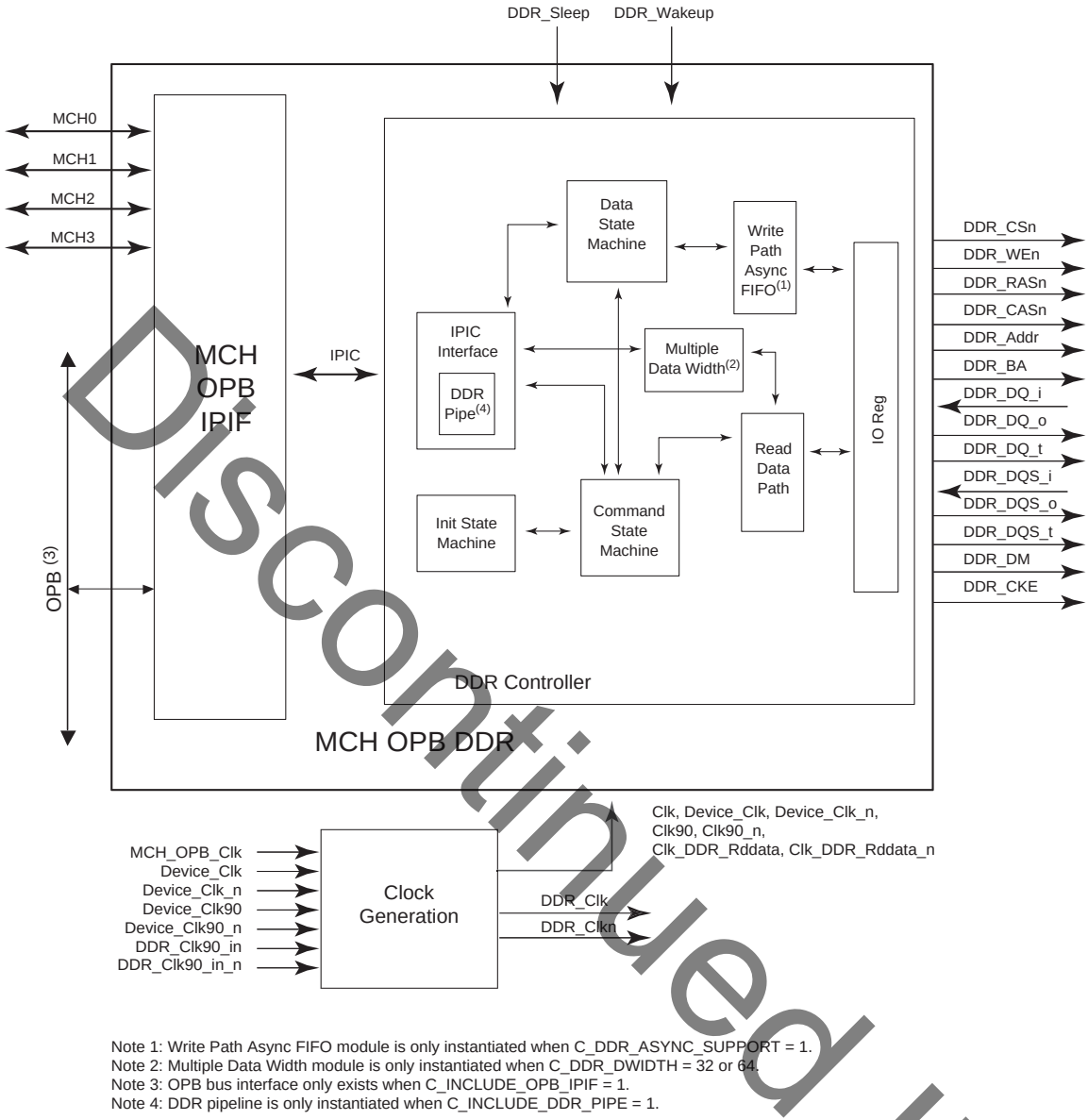
IMPORTANT: Virtex-II and Virtex-II Pro IO pairs share input and output clock signals. Since the DDR registers in the IO blocks use both of the input and output clock signals, the ports assigned to the IO pairs must use the same input and output clocks. Care should be taken when making port IO assignments that the DDR_DQ and DDR_DM signals use the system clock as the output clock and the DDR_DQS signals use a 90 degree phase shift of the system clock as the output clock. Therefore, a DDR_DQS signal should not be assigned with a DDR_DQ signal or a DDR_DM signal in an IO pair.

Note this MCH OPB DDR SDRAM controller design utilizes DDR registers in the FGPA IO blocks and may not be suitable for some FPGA families that do not support this feature.

Since the DDR_DQ and DDR_DQS busses are 3-stateable, the user should pullup these signals in the FPGA IO blocks or external to the FPGA in the board design. Note that the DDR controller design will drive the DQS signals to a '1' during the IDLE state so only one DDR controller can be used to control a DDR memory, i.e., two DDR controllers can not share the same DDR memory.

MCH OPB DDR SDRAM Controller Design

The block diagram for the MCH OPB DDR SDRAM controller is shown in Figure 3. The MCH OPB DDR consists of the MCH OPB IPIF and the DDR controller. The MCH OPB IPIF provides the bus protocol and Multi-CHannel (MCH) interface, while the DDR controller provides the DDR SDRAM interface, including the control logic state machines, initialization logic, and I/O registers.



Note 1: Write Path Async FIFO module is only instantiated when C_DDR_ASYNC_SUPPORT = 1.
Note 2: Multiple Data Width module is only instantiated when C_DDR_DWIDTH = 32 or 64.
Note 3: OPB bus interface only exists when C_INCLUDE_OPB_IPIF = 1.
Note 4: DDR pipeline is only instantiated when C_INCLUDE_DDR_PIPE = 1.

Figure 3: **MCH OPB DDR Block Diagram**

The separation of the Command State Machine and the Data State Machine allows for the application of commands to the DDR while data reception/transmission is in progress. Overlapping the DDR commands with the data transfer when accessing data in the same row of the same bank allows for more optimal DDR operation.

Supporting Open Row Management

To enable open row management, the design parameter, C_USE_OPEN_ROW_MNGT must be set to 1. By setting this parameter, the addressable row of memory currently being accessed will remain open for subsequent operations. Upon the completion of the current read or write transaction, a PRECHARGE command will not be executed to the memory device. In not closing the row at the end on the previous transaction, the subsequent operation can bypass the ACTIVE command (in conjunction with the READ/WRITE command). This is only true when the subsequent operation is to access the same addressable row of memory.

However, if the subsequent operation is to the same addressable row of memory, but in a different bank address, the ACTIVE command must be issued at the beginning of the read or write operation.

It is recommended the parameter, C_USE_OPEN_ROW_MNGT = 1 when accesses to memory will occur in a sequential manner. If the addressable accesses into DDR SDRAM can not be predicted (or will not occur in a sequential manner), then it is suggested the parameter, C_USE_OPEN_ROW_MNGT be set to 0.

While the open row management feature improves latency on back to back operations when accessing the same row of addressable memory, there is a penalty for crossing row addresses. When C_USE_OPEN_ROW_MNGT = 1 on a subsequent operation that requires a different addressable row of memory, a PRECHARGE must first be executed to the previously open row prior to completing the pending operation.

When C_USE_OPEN_ROW_MNGT = 0, the DDR SDRAM controller will execute a PRECHARGE at the end of read or write transaction to the current row being accessed in the SDRAM memory. This behavior is highlighted by transitioning to the PRECHARGE_CMD state in the Command State Machine (see "Command State Machine" on page 19).

Open Row Management with Multiple CS Banks of Memory

Note the following behavior when open row management is enabled, C_USE_OPEN_ROW_MNGT = 1 and multiple external chip selectable banks of memory are enabled, i.e., C_NUM_BANKS_MEM is greater than 1. If any back to back read or write operations access two different external chip selectable banks of memory, the currently access row of memory will be closed, i.e., a PRECHARGE command is issued, before accessing a different chip selectable bank of memory.

For example, if two memory banks (i.e., C_NUM_BANKS_MEM = 2) are specified as follows:

- C_MEM0_BASEADDR = 0x3000_0000
- C_MEM0_HIGHADDR = 0x3FFF_FFFF
- C_MEM1_BASEADDR = 0x4000_0000
- C_MEM1_HIGHADDR = 0x4FFF_FFFF

The external chip selects to DDR memory is DDR_CSn(0:1); where DDR_CSn(0) is used to access 0x3000_0000 to 0x3FFF_FFFF and DDR_CSn(1) is asserted to access 0x4000_0000 to 0x4FFF_FFFF.

If the first operation is accessing address 0x3000_1000 and the subsequent operation is accessing address 0x4000_1000, the row addresses match to allow open row management. However, since DDR_CSn(0) will negate after the first transaction and DDR_CSn(1) will assert for the second transaction, a PRECHARGE must be issued and close the open row for the operation at address 0x3000_1000. Then an ACTIVE command is issued to open the row for the operation at address 0x4000_1000.

Supporting Self Refresh

The DDR controller can be instructed to place the DDR SDRAM memory into self refresh mode. This mode is useful because the DDR SDRAM memory will maintain its data contents and issue its own refresh signals, allowing the controller and the rest of the system to be reset.

Two inputs to the DDR SDRAM controller are used to support the SDRAM self refresh mode, DDR_Sleep and DDR_WakeUp. These are discrete input signals and must be generated at the system level, they are not derived from the interface.

A rising edge of the DDR_Sleep signal will cause the DDR controller to execute the command sequence required to place the DDR SDRAM into self refresh. MCH_OPB_Rst is then asserted to place the entire system into reset. A minimum period of 50uS from the assertion of DDR_Sleep to the assertion of MCH_OPB_Rst is required to insure the DDR SDRAM is in the self refresh mode. Note that the DDR SDRAM controller does not provide the timing for the reset assertion, this should be done at the system level. Please refer to Figure 4 for information on the timing relationships of these signals.

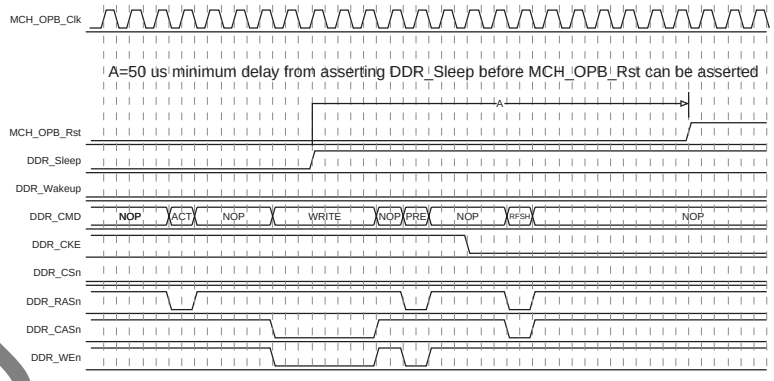


Figure 4: **Entering DDR Self Refresh**

The DDR_WakeUp signal is used to inform the DDR controller if the power-up intialization sequence needs to be performed, or if the sequence to instruct the DDR SDRAM to exit self refresh needs to be performed. If the DDR_WakeUp signal is negated when MCH_OPB_Rst negates, the SDRAM controller will perform the DDR SDRAM intialization sequence. If the DDR_WakeUp signal is asserted when MCH_OPB_Rst negates, the DDR controller will instruct the DDR to exit the self refresh mode. Note that the DDR_WakeUp signal must be at its desired level at least 5 clock periods before MCH_OPB_Rst negates. It is assumed that the clock is stable before MCH_OPB_Rst negates. Please refer to Figure 5 for information on the timing relationships of these signals.

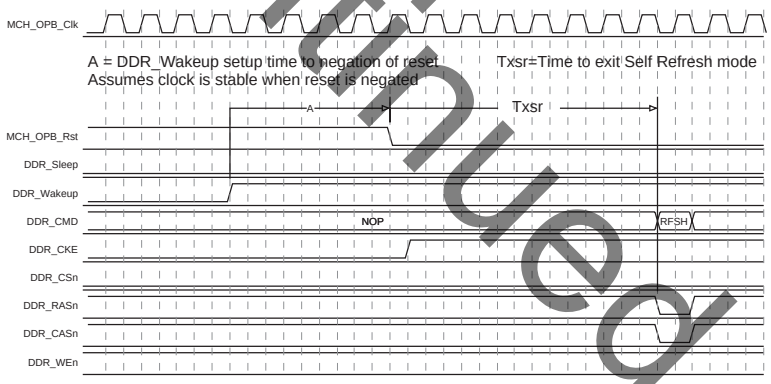


Figure 5: **Exiting DDR Self Refresh**

IPIC Pipeline

The parameter, C_INCLUDE_DDR_PIPE, configures the MCH OPB DDR core with an internal pipeline stage. The pipeline is optional and depending on other core parameter settings may allow the designer to reach a higher clock frequency in which the core can operate. The pipeline stage is inserted between the MCH OPB IPIF and the DDR control state machines and will add one clock cycle of latency on all memory transactions.

Init State Machine

DDR SDRAMs must be powered-up and initialized in a predefined manner. After power supplies and all the clocks are stable, the DDR SDRAM requires a 200uS delay prior to applying an executable command.

The Init State Machine provides the 200uS delay and the sequencing of the required DDR SDRAM start-up commands.It instructs the Command State Machine to send the proper commands in the proper sequence to the DDR SDRAM. This state machine starts execution after Reset and returns to the IDLE state when Reset is applied.

When the initialization sequence has been completed, the DDR_INIT_DONE signal asserts.

Note that after Reset has been applied, the 200uS delay is again implemented before any commands are issued to the DDR SDRAM. The 200uS delay must be accounted for in simulation as well as the delay of the command sequence.

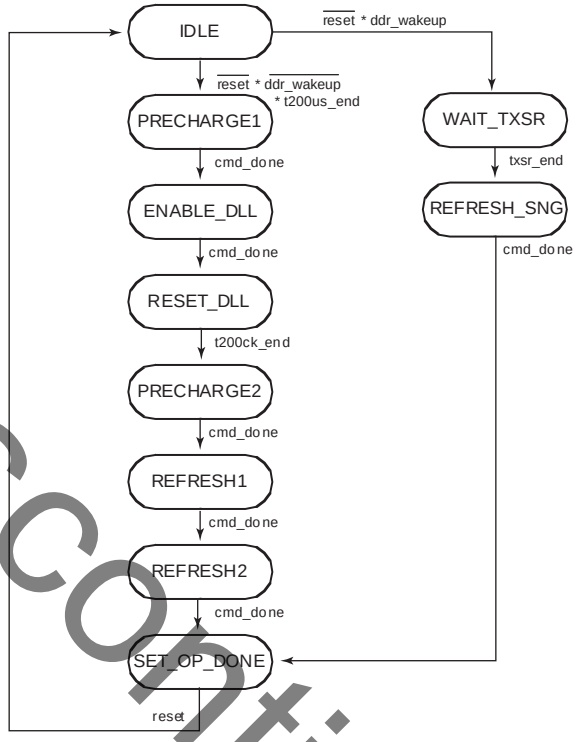


Figure 6: **DDR SDRAM Init State Machine**

Command State Machine

The Command State Machine provides the address bus and commands signals to the DDR SDRAM. It sends the DATA_EN signal to the Data State Machine to start the reception/transmission of data. If a burst transaction is in progress or a secondary transaction has been received, the Command State Machine will send the next command to the DDR SDRAM while data reception/transmission is still in progress to optimize the DDR SDRAM operation.

A simplified version of the Command State Machine is shown in Figure 7. For readability, only the major state transitions are shown. Figure 7 illustrates the Command State Machine implementation when open management is disabled, i.e., C_USE_OPEN_ROW _MNGT = 0.

When a rising edge on DDR_Sleep is detected, the Command State Machine will first close all open rows, with a PRECHARGE ALL command. The REFRESH command is then issued with the DDR_CKE signal negated to put the DDR SDRAM into the self refresh mode. The DDR SDRAM will remain in the self refresh mode for a minimum of TRAS. The Command State Machine remains in self refresh until RESET is asserted. RESET can only be asserted a minimum of 50 us after the assertion of DDR_Sleep.

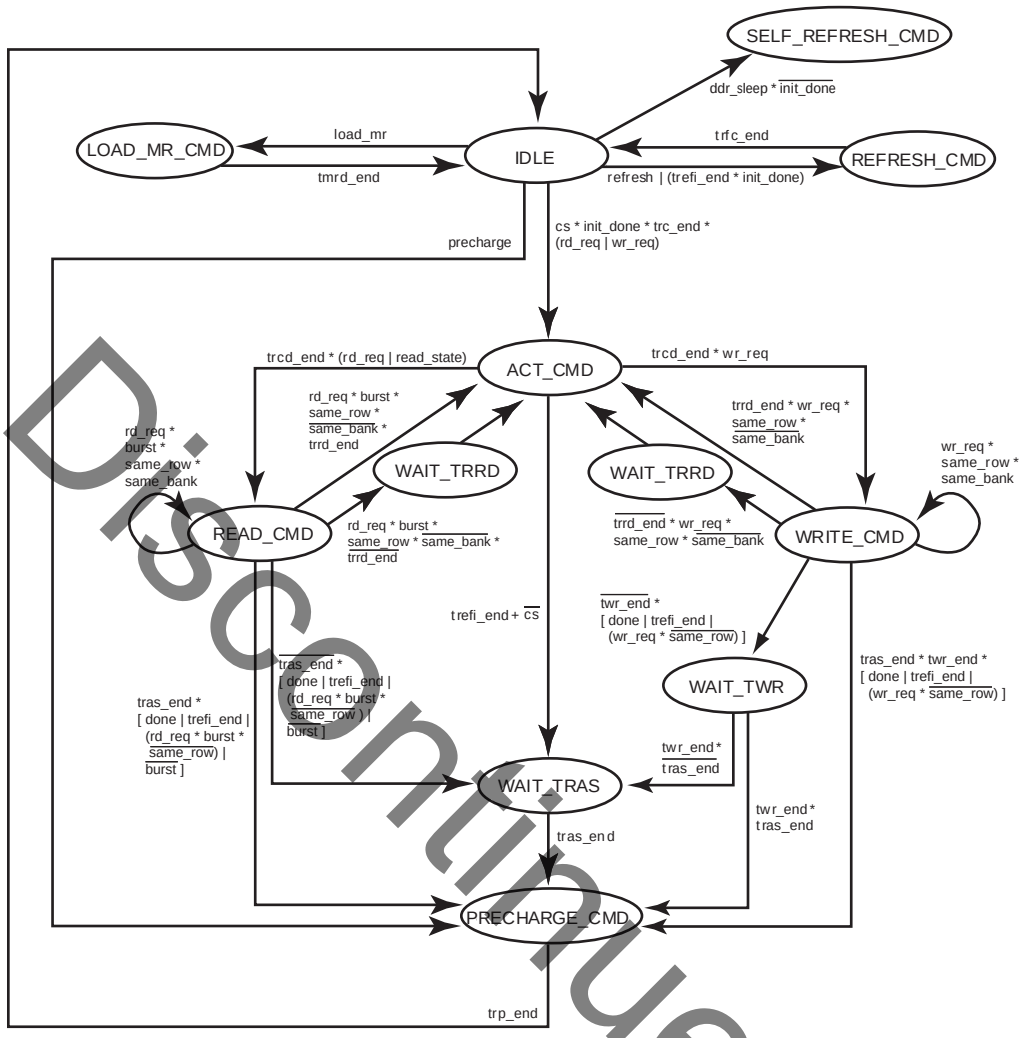


Figure 7: **DDR Command State Machine when C_USE_OPEN_ROW_MNGT = 0**

The Command State Machine shown in Figure 8 represents the logic when open row management is enabled, i.e., C_USE_OPEN_ROW_MNGT = 1. When open row management is enabled, the currently accessed row of the DDR SDRAM memory will remain open for subsequent operations unless one of the following conditions is true:

- A refresh operation is necessary, i.e., trefi_end is asserted
- The DDR SDRAM is entering Self Refresh mode, i.e., ddr_sleep is asserted
- The subsequent operation is requesting a read or write to a different row address, i.e., same_row is de-asserted
- The subsequent operation is crossing external memory chip select banks, i.e., DDR_CSn is changing value (only applicable when C_NUM_BANKS_MEM > 1)

Figure 8 illustrates the command sequence to execute for read or write operations when a row remains active after the previous operation.

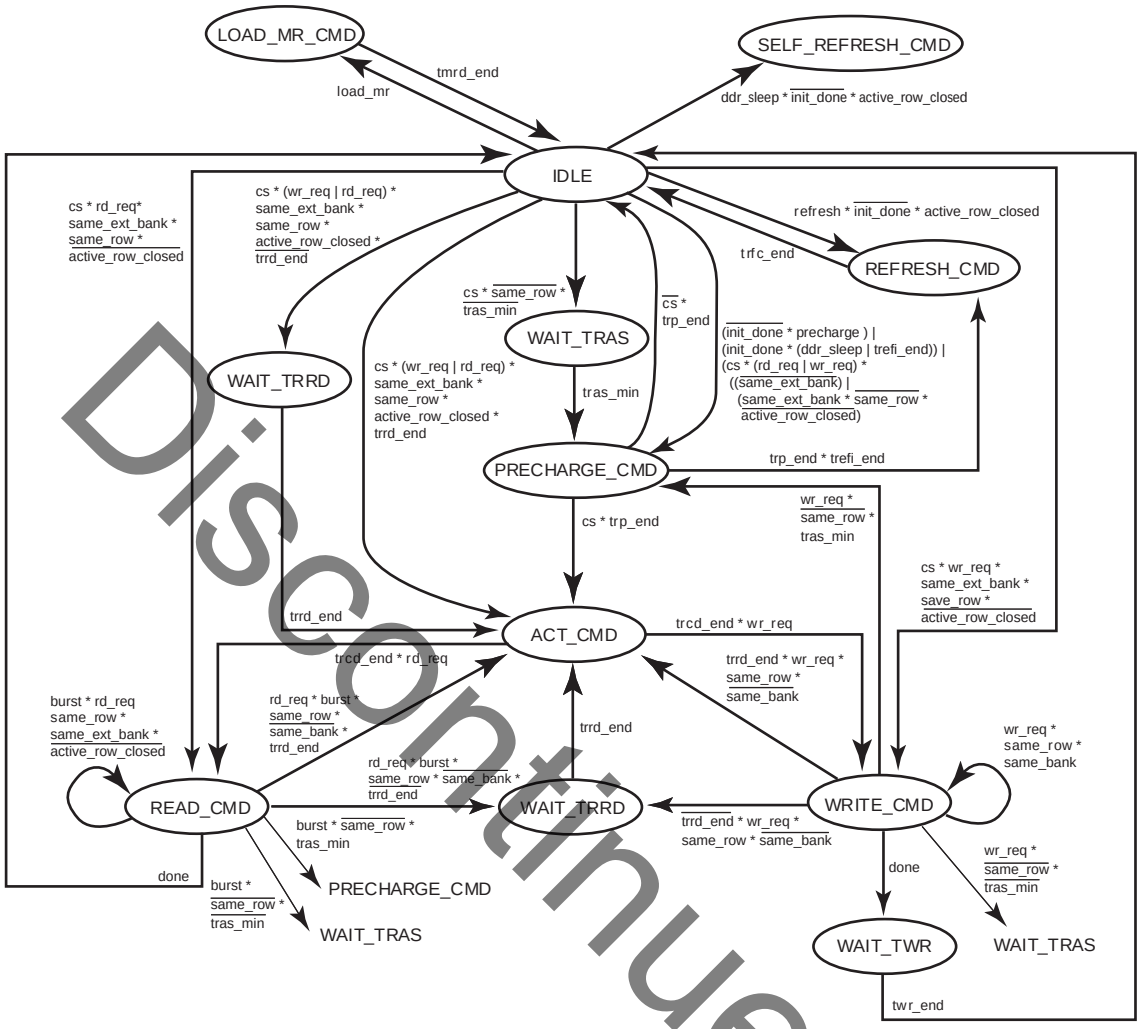


Figure 8: **DDR Command State Machine when C_USE_OPEN_ROW_MNGT = 1**

Data State Machine

The Data State Machine transfers the data to/from the DDR SDRAM and determines when the specified DDR SDRAM burst is complete. It monitors the PEND_OP signal from the Command State Machine to know if more data transmissions are required. It waits for CAS_LATENCY during read operations and signals when the DDR has completed the data transfer for both read and write operations. It provides the READ_DATA_EN signal to the input DDR SDRAM registers and read data FIFO.

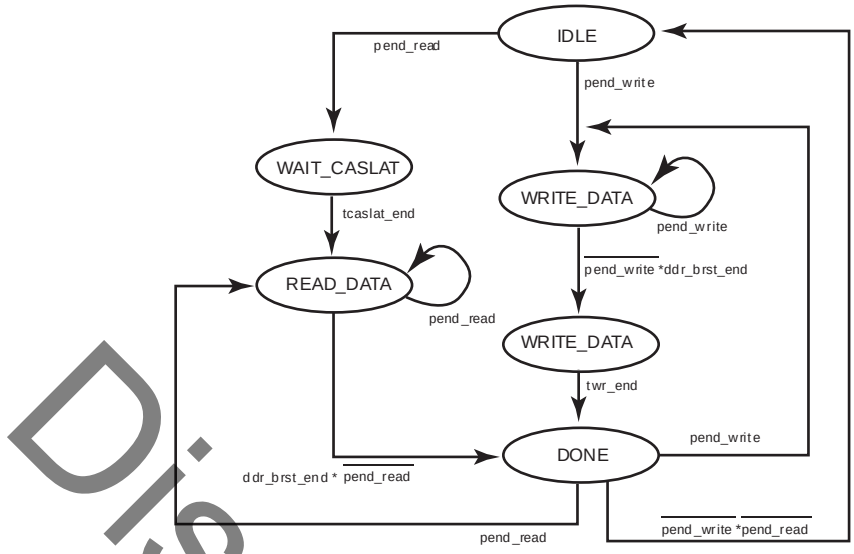


Figure 9: **DDR SDRAM Data State Machine**

Separate DDR Device Clock Operation

In many systems, it may be desired to operate the DDR at a separate clock frequency than the OPB or MCH clock. The parameter, C_DDR_ASYNC_SUPPORT = 1, allows the user to separate the system and DDR device clock domains. The Write Path Async FIFO block (shown in Figure 3) enables the DDR SDRAM to operation on a separate clock domain from the MCH_OPB bus clock. The logic includes a state machine and an asynchronous FIFO in order to synchronize the command, data, address, data mask and control signals. The output signals from the asynchronous FIFO are then inputs to IO REG module.

I/O Registers

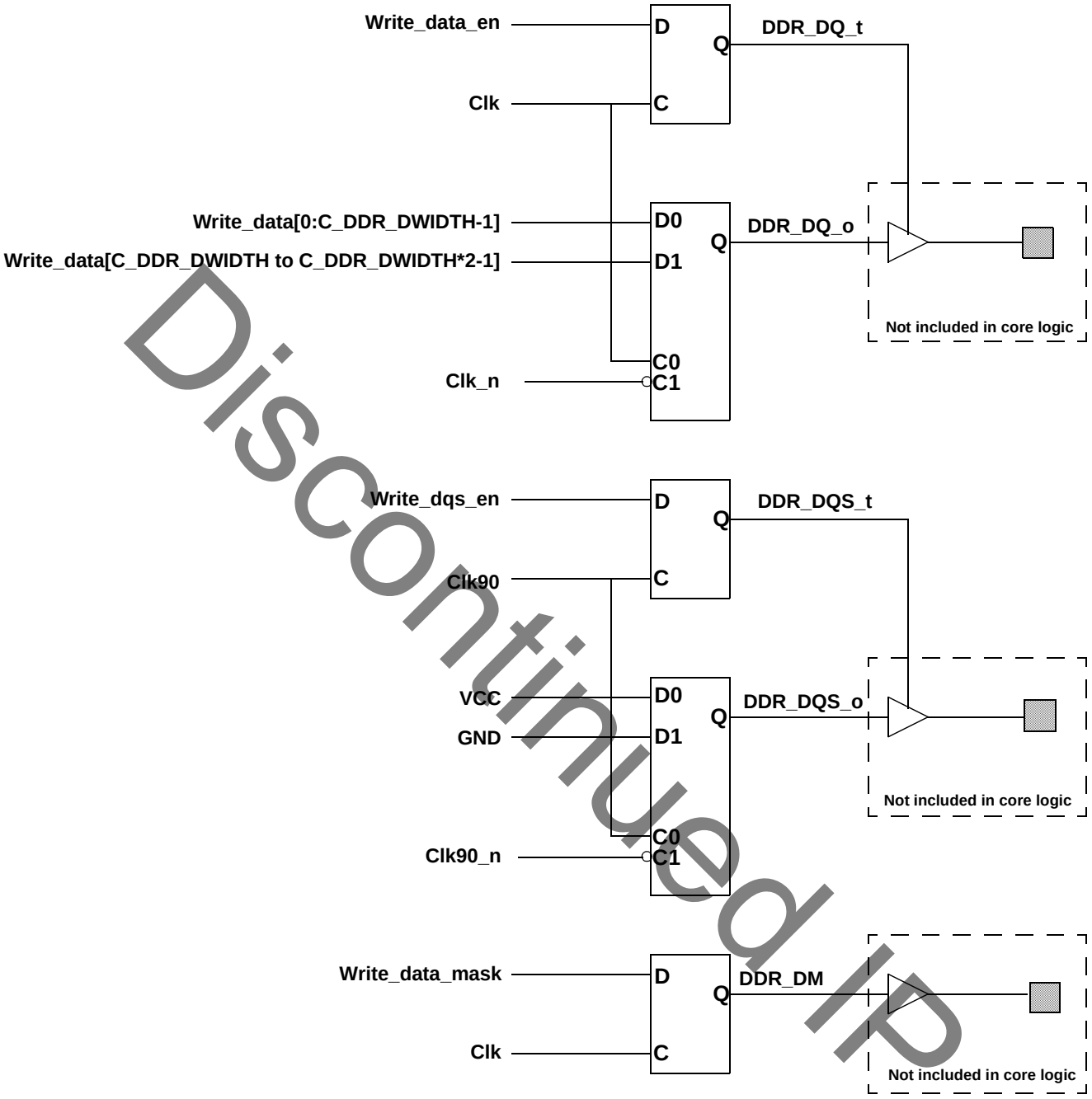
Control Signals

All control signals and the address bus to the DDR SDRAM are registered in the IOBs of the FPGA.

Write Data

The DDR I/O registers are used to output the write data to the DDR SDRAM as shown in Figure 10. Since the clock is being generated from the Clk90 output of the DCM, the Clk output is used to clock out the data so that the DDR clock is centered in the DDR data. This also allows a full clock period for the data to get to the IOBs.

DQS is generated from the Clk90 output so that it is centered in the data.



Note: The design parameter, C_DDR_ASYNC_SUPPORT, determines if Clk, Clk_n, Clk90, & Clk90_n are derived from MCH_OPB_Clk or Device_Clk.

Figure 10: **Write Data Path**

Read Data

The DDR I/O registers are used to input data from the DDR SDRAM as shown in Figure 11. The clock output to the DDR is used to clock the input data. This clock is input to a DCM and generates DDR_Clk90_in.

During a read cycle, the data strobe signal from the DDR SDRAM (DDR_DQS) is registered on the rising edge only of DDR_Clk90_in so that it is always high while the DDR SDRAM is transmitting data. This signal will be used by the Read Data Path logic as the write enable into a FIFO.

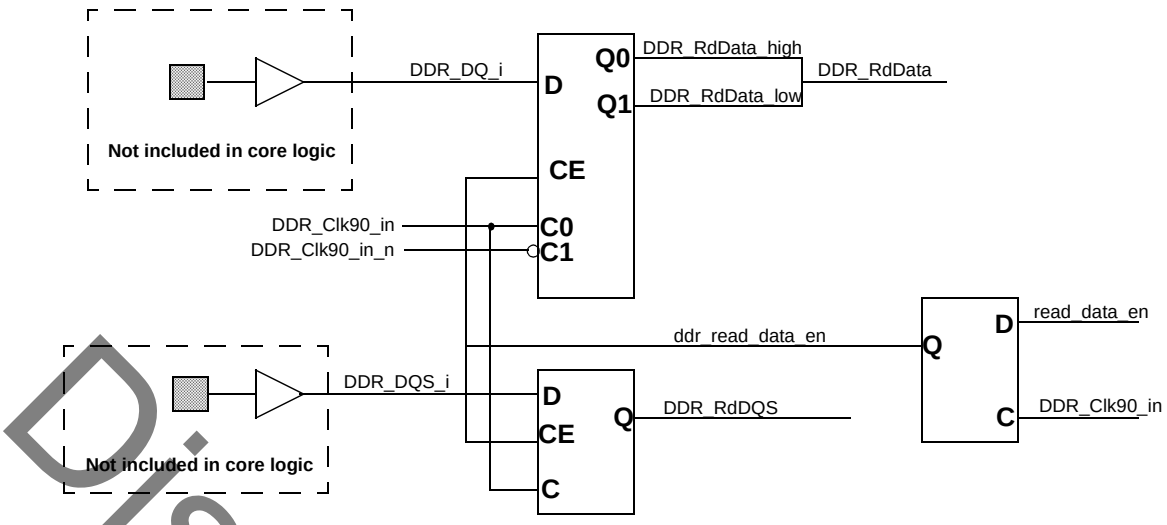


Figure 11: **DDR Input Data Registers**

Read Data Path Logic

The Read Data Path logic consists of an asynchronous FIFO in which the DDR SDRAM input data is written from the DDR_Clk90_in and read from the internal FPGA clock. The write enable to the FIFO is the DDR_RdDQS signal which will be high during DDR SDRAM data transmission.

Once the FIFO is not empty, the data is read from the FIFO and a read acknowledge is generated. This is shown in Figure 12.

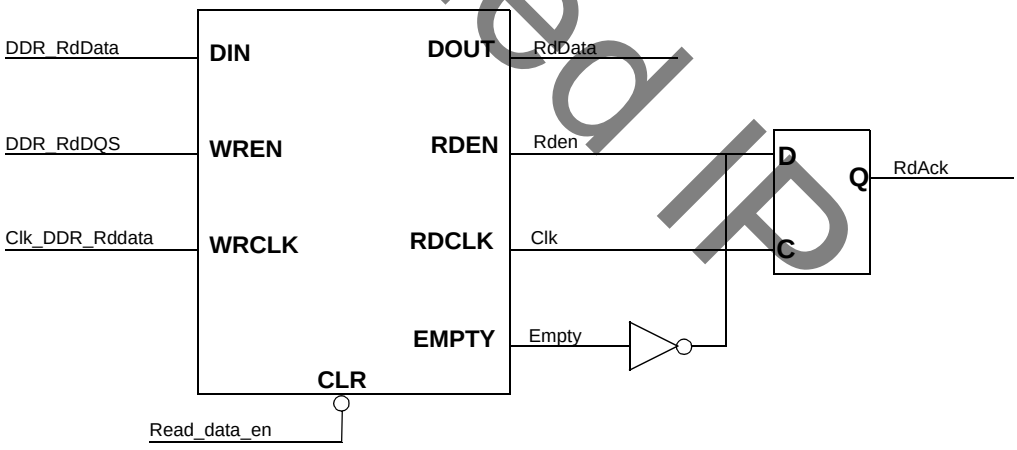


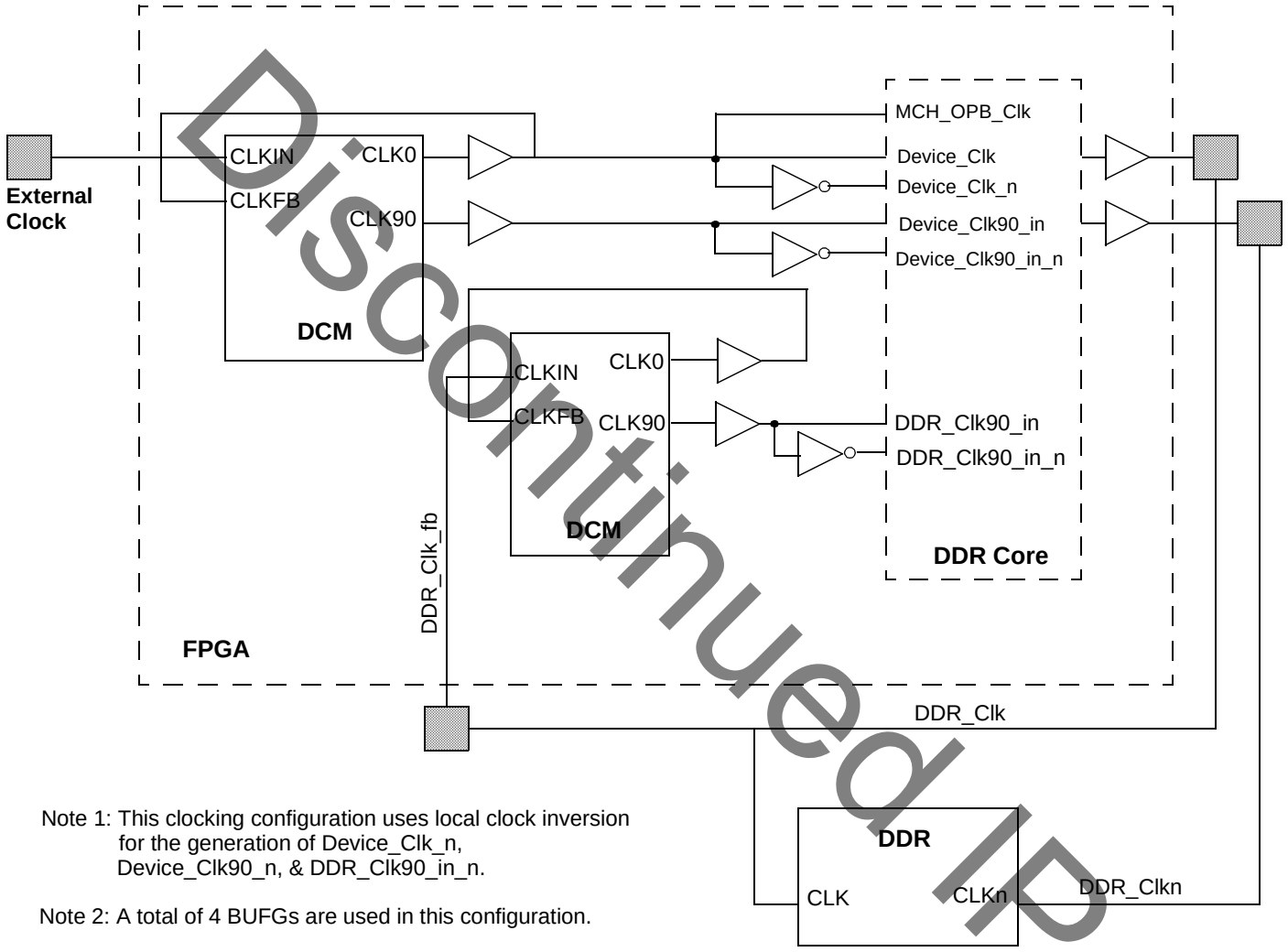
Figure 12: **Read Data Path**

DDR Clocking

Clock Generation

The clocking scheme required in the FPGA and used by the MCH OPB DDR SDRAM controller core is shown in Figure 13 through Figure 16. The input clock connections depend on the available BUFG resources in the FPGA and the design parameter, C_DDR_ASYNC_SUPPORT. When C_DDR_ASYNC_SUPPORT = 0, the MCH_OPB_Clk input port can be identical to the Device_Clk input. When C_DDR_ASYNC_SUPPORT = 1, the MCH_OPB_Clk is unique from the DDR Device External Clock source.

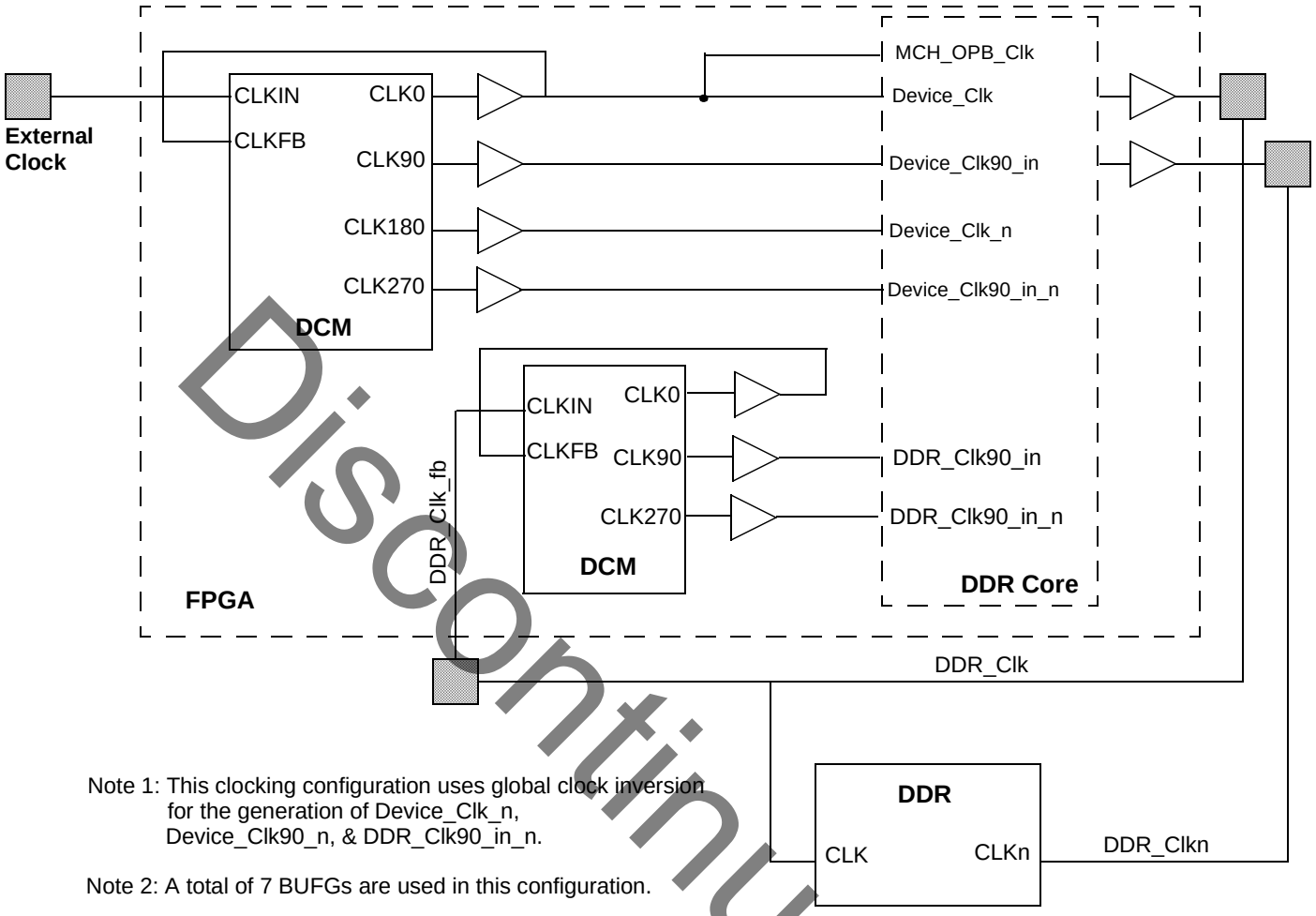
An example implementation can be found in the DDR Clock Module Reference design available in the EDK Toolkit.



Note 1: This clocking configuration uses local clock inversion for the generation of Device_Clk_n, Device_Clk90_n, & DDR_Clk90_in_n.

Note 2: A total of 4 BUFGs are used in this configuration.

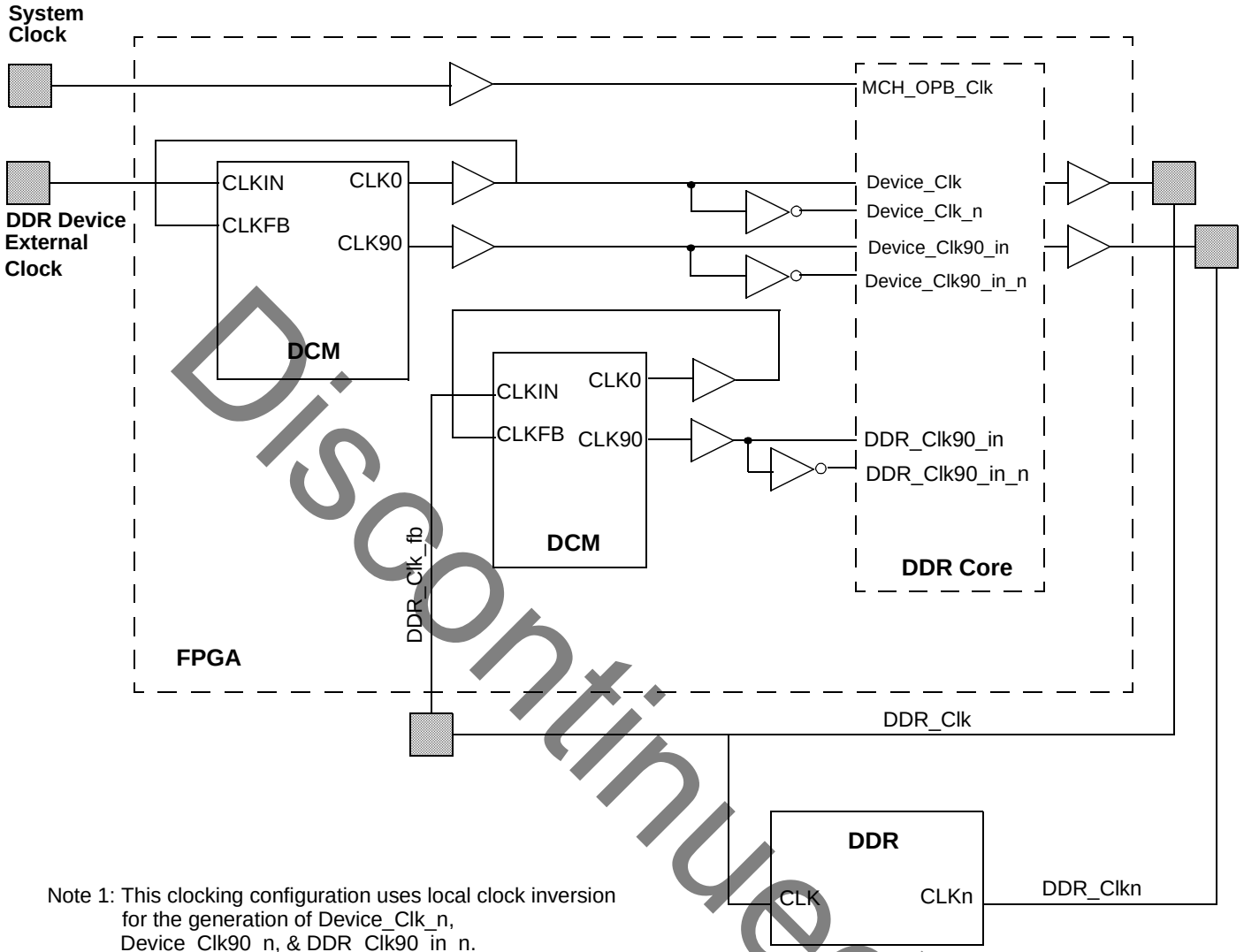
Figure 13: **DDR Clocking (Option 1) when C_DDR_ASYNC_SUPPORT = 0**



Note 1: This clocking configuration uses global clock inversion for the generation of Device_Clk_n, Device_Clk90_n, & DDR_Clk90_in_n.

Note 2: A total of 7 BUFGs are used in this configuration.

Figure 14: **DDR Clocking (Option 2) when C_DDR_ASYNC_SUPPORT = 0**

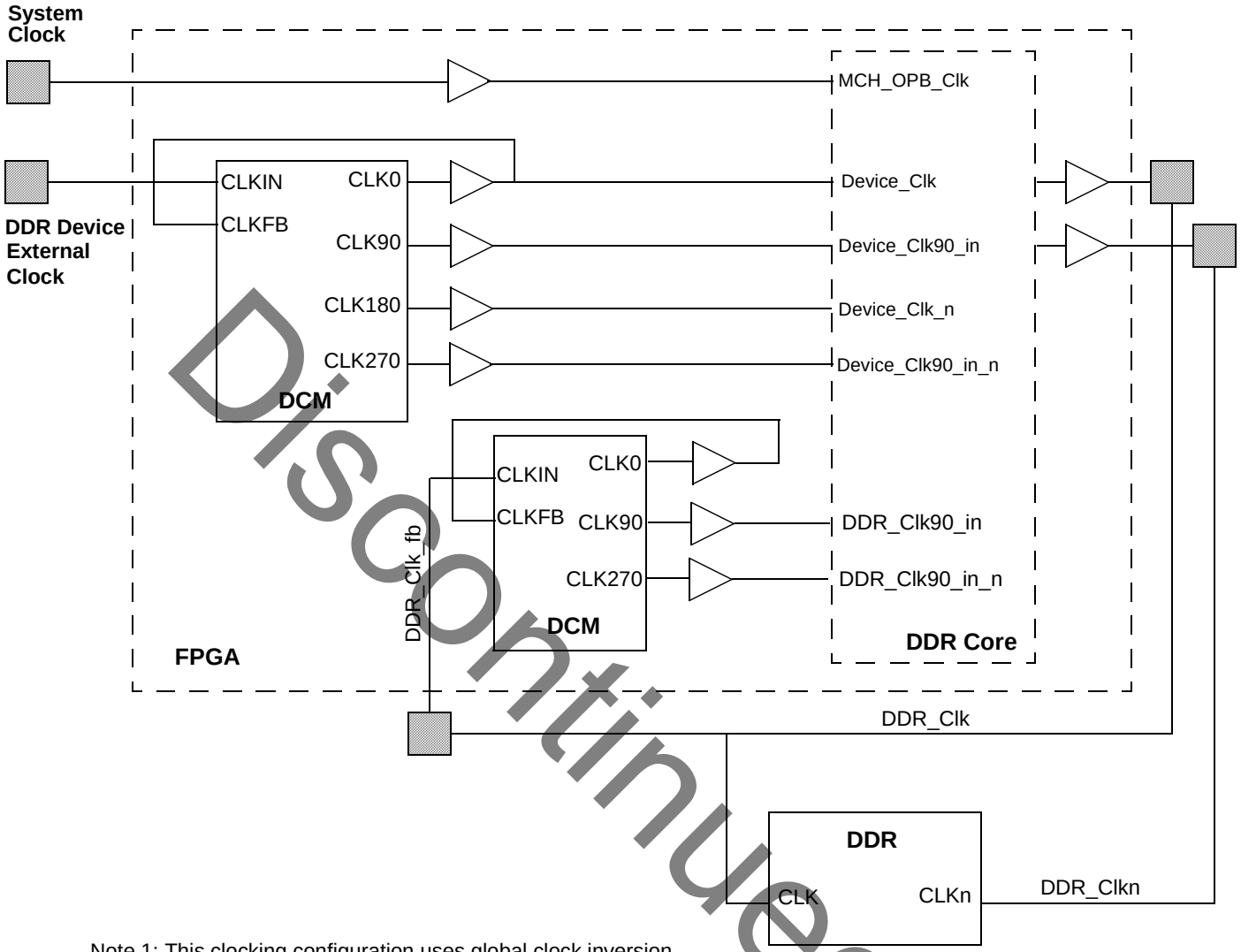


Note 1: This clocking configuration uses local clock inversion for the generation of Device_Clk_n, Device_Clk90_n, & DDR_Clk90_in_n.

Note 2: An additional BUFG is used for the MCH_OPB_Clk in this configuration.

Note 3: A total of 5 BUFGs are used in this configuration.

Figure 15: **DDR Clocking (Option 1) when C_DDR_ASYNC_SUPPORT = 1**



Note 1: This clocking configuration uses global clock inversion for the generation of Device_Clk_n, Device_Clk90_n, & DDR_Clk90_in_n.

Note 2: An additional BUFG is used for the MCH_OPB_Clk in this configuration.

Note 3: A total of 8 BUFGs are used in this configuration.

Figure 16: **DDR Clocking (Option 2) when C_DDR_ASYNC_SUPPORT = 1**

Clk and Clk90 Generation

A DCM is required to generate the clock used internal to the FPGA as shown in Figure 13 through Figure 16. A 90 degree phase output of the DCM is input to the MCH OPB DDR SDRAM controller core and is used to generate the DDR clock and DQS signals.

DDR Clock Generation

The clock output to the DDR SDRAMs is generated using the DDR I/O registers as shown in Figure 17. The Clk90_in and Clk90_in_n signals are used to generate the DDR_Clk (and DDR_Clkn) so that the clock is centered in the data output to the DDR SDRAM.

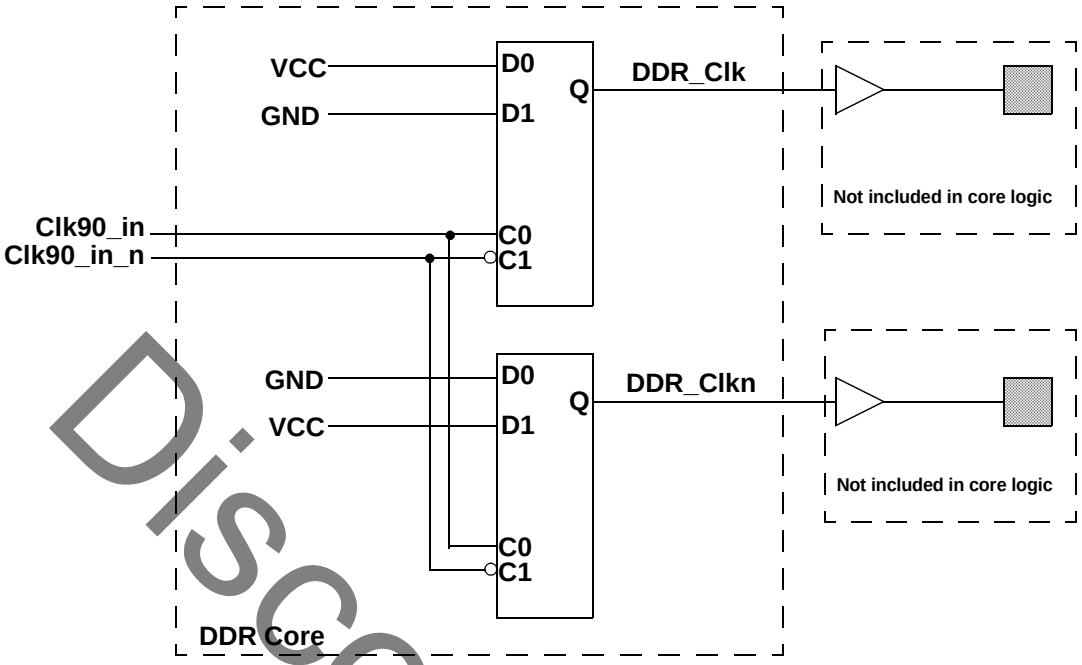


Figure 17: **DDR Clock Generation**

DDR SDRAM Clock Input Synchronization

Another DCM will be required by this design to align the clock output to the DDR registers with the data from the DDR SDRAM to accurately register this data. The DDR_Clk output will need to be connected to the DDR_Clk_fb shown in Figure 13 through Figure 16 as an external board connection. The Clk90 output of the DDR Clock DCM is input to the MCH OPB DDR SDRAM controller core and is used to clock in the DDR data.

Due to the variation in board layout, the DDR clock and the DDR data relationship can vary. Therefore, the designer should analyze the time delays of the system and set all of the attributes of the phase shift controls of the DCM as needed to insure stable clocking of the DDR data.

Timing Diagrams

The following diagrams illustrate the relationship between the Multi-CHannel connection(s) and the DDR memory.

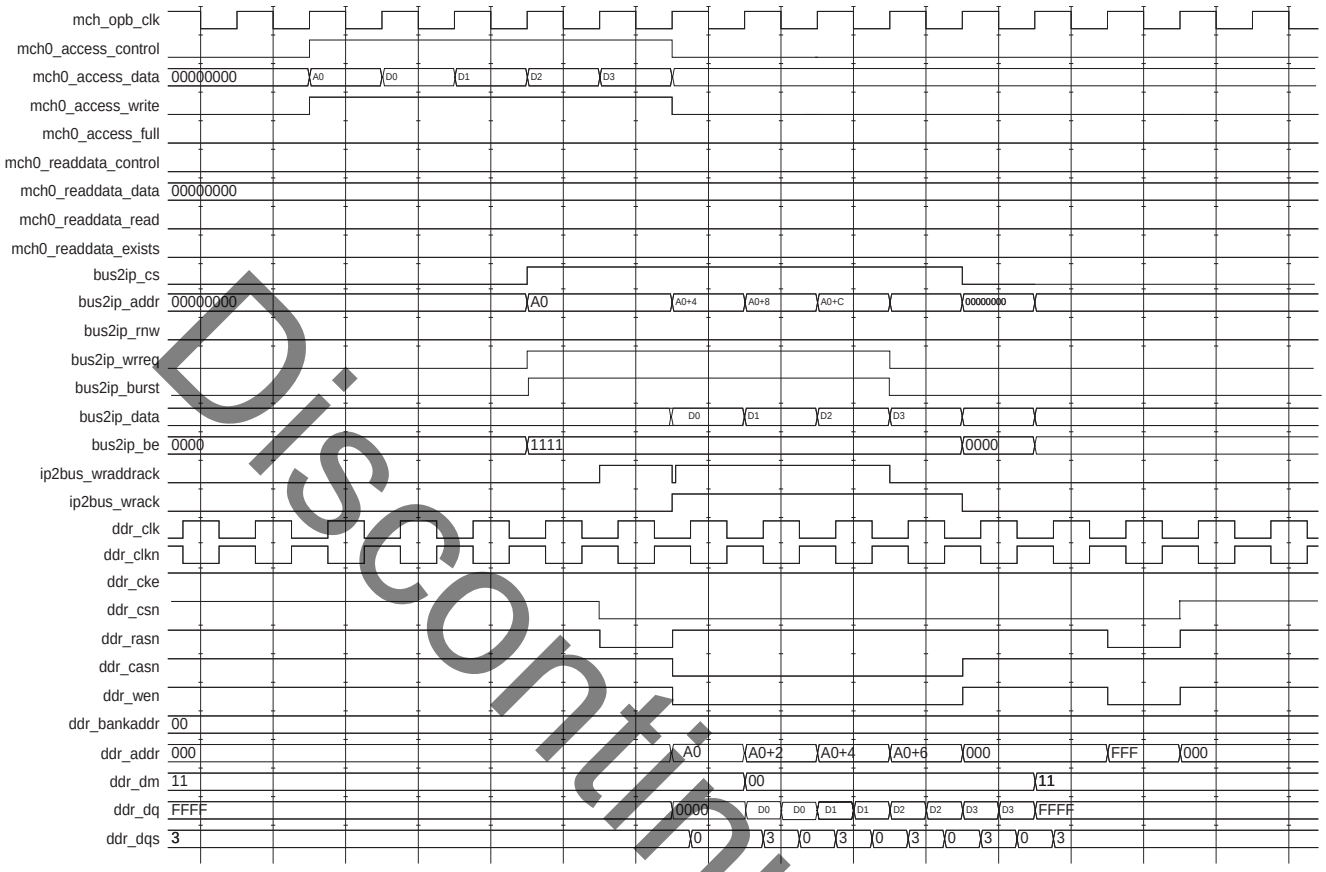


Figure 18: **Single XCL 4 Word Cacheline Write**

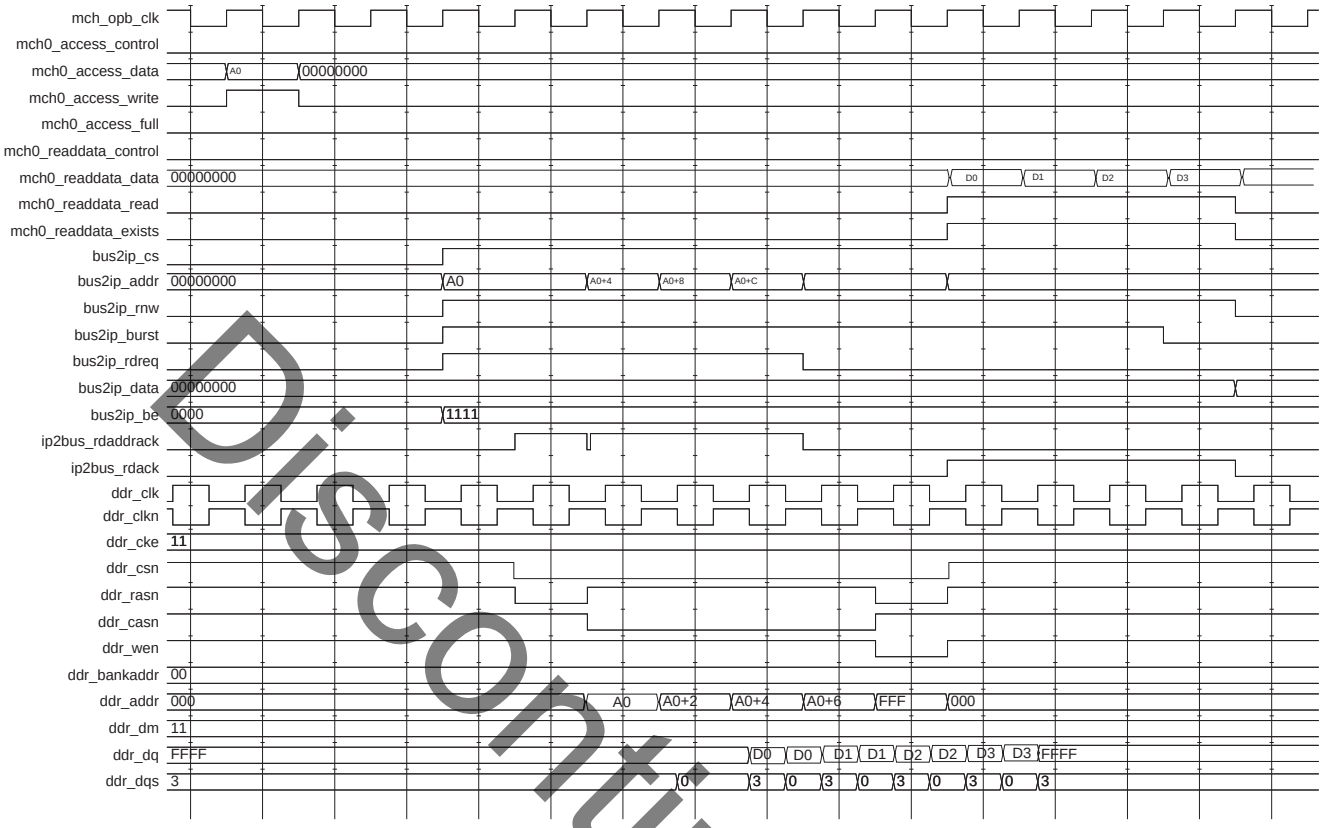


Figure 19: **Single XCL 4 Word Cacheline Read**

Design Constraints

Note: An example UCF for this core is available and must be modified for use in the system. Please refer to the *EDK Getting Started Guide* for the location of this file.

Timing Constraints

A timing constraint should be placed on the system clock, setting the frequency to meet the bus timing requirements. A timing constraint should also be placed on the DDR feedback clock to set the frequency of this clock. An example is shown in Figure 20.

```
NET "MCH_OPB_Clk" TNM_NET = "MCH_OPB_Clk";
TIMESPEC "TS_MCH_OPB_Clk" = PERIOD "MCH_OPB_Clk" 9 ns HIGH 50 %;

NET "Device_Clk" TNM_NET = "Device_Clk";
TIMESPEC "TS_Device_clk" = PERIOD "Device_Clk" 6 ns HIGH 50 %;

NET "Device_Clk_n" TNM_NET = "Device_Clk_n";
TIMESPEC "TS_Device_clk_n" = PERIOD "Device_Clk_n" "TS_device_clk"* 1 PHASE + 3ns;

NET "Device_Clk90_in" TNM_NET = "Device_Clk90_in";
TIMESPEC "TS_Device_Clk90_in" = PERIOD "Device_Clk90_in" "TS_device_clk"* 1 PHASE + 1.5ns;

NET "Device_Clk90_in_n" TNM_NET = "Device_Clk90_in_n";
TIMESPEC "TS_Device_Clk90_in_n" = PERIOD "Device_Clk90_in_n" "TS_device_clk"* 1 PHASE +
4.5ns;

NET "DDR_Clk90_in" TNM_NET = "DDR_Clk90_in";
TIMESPEC "TS_DDR_Clk90_in" = PERIOD "DDR_Clk90_in" 6 ns HIGH 50 %;

NET "DDR_Clk90_in_n" TNM_NET = "DDR_Clk90_in_n";
TIMESPEC "TS_DDR_Clk90_in_n" = PERIOD "DDR_Clk90_in_n" "TS_DDR_Clk90_in"* 1 PHASE + 3ns;
```

Figure 20: **DDR Timing Constraints**

Pin Constraints

The DDR I/O should be set to the SSTL2 I/O standard. If external pullups/pulldowns are not available on the DDR DQ and DQS signals, then these pins should be specified to use pullup or pulldown resistors. Pulldown resistors are preferred. An example is shown in Figure 21.

```
NET "DDR_DQS<*>" IOSTANDARD=SSTL2_I;
NET "DDR_DQS<*>" PULLDOWN;
NET "DDR_DQ<*>" IOSTANDARD=SSTL2_I;
NET "DDR_DQ<*>" PULLDOWN;
```

Figure 21: **DDR Pin Constraints**

Design Implementation

Target Technology

The intended target technology is a Spartan-3 or Virtex family FPGAs.

Device Utilization and Performance Benchmarks

The MCH OPB DDR SDRAM controller is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are estimates. As the MCH OPB DDR SDRAM controller is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the MCH OPB DDR SDRAM controller design will vary from the results reported here.

The MCH OPB DDR SDRAM controller benchmarks are shown in Table 9 for a Spartan-3 XC3S1500 -5 FPGA.

Table 9: **FPGA Performance and Resource Utilization (Spartan-3)**

Run #	Parameter Values									Device Resources			Performance	
	C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST	C_DDR_ASYNC_SUPPORT	C_USE_OPEN_ROW_MNGT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	C_INCLUDE_DDR_PIPE	Slices	Slice FFs	4-input LUTs	MCH / OPB Clock Fmax (MHz)	DDR Device Clock Fmax (Mhz)
1	1	0	0	0	0	0	1	16	0	424	309	482	115.5	N/A
2	1	0	0	0	0	0	4	16	0	425	313	521	110.7	N/A
3	2	0	0	0	0	0	1	16	0	629	416	773	112.1	N/A
4	4	0	0	0	0	0	1	16	0	910	605	1175	73.4	N/A
4									1	940	716	1332	91.6	N/A
5	2	1	0	0	0	0	1	16	0	866	678	939	81.9	N/A
6	2	1	1	0	0	0	1	16	0	906	696	1159	79.4	N/A
6									1	945	802	1324	87.9	N/A
7	4	1	1	0	0	0	1	16	0	1206	892	1557	66.4	N/A
7									1	1269	996	1752	74.9	N/A
8	2	0	0	1	0	0	1	16	0	704	569	1020	95.7	145.2
9	2	1	0	1	0	0	1	16	0	1022	823	1229	78.1	144.6
10	2	1	1	1	0	0	1	16	0	1068	840	1447	67.4	143.7
11	2	1	0	0	1	0	1	16	0	904	687	1019	66.7	N/A
11									1	918	802	1168	91.9	N/A
12	2	1	1	0	1	0	1	16	0	962	705	1232	72.8	N/A
12									1	955	820	1409	84.6	N/A
13	2	1	1	0	1	0	2	16	0	1022	726	1452	66.7	N/A
13									1	1037	844	1616	75.7	N/A
14	2	1	1	1	1	0	2	16	0	1156	882	1766	61.2	142.3
14									1	1223	1004	1866	70.3	147.0
15	2	1	0	1	0	1	2	16	0	1045	903	1296	68.7	146.4
16	2	1	0	1	1	1	2	16	0	1102	930	1527	64.6	145.3
16									1	1208	1030	1618	73.7	141.1
17	2	1	1	1	1	1	2	16	0	1101	932	1766	63.3	129.4
17									1	1250	1046	1884	80.3	147.5
18	2	1	1	0	0	0	1	32	0	1035	776	1368	71.8	N/A
18									1	1039	875	1492	82.8	N/A
19	2	1	1	1	1	0	1	32	0	1326	1007	1857	66.2	145.7
19									1	1293	1115	1911	86.6	143.3

The MCH OPB DDR SDRAM controller benchmarks are shown in Table 10 for a Virtex-II Pro XC2VP20 -6 FPGA.

Table 10: **FPGA Performance and Resource Utilization (Virtex-II Pro)**

	Parameter Values									Device Resources			Performance	
Run #	C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST	C_DDR_ASYNC_SUPPORT	C_USE_OPEN_ROW_MNGT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	C_INCLUDE_DDR_PIPE	Slices	Slice FFs	4-input LUTs	MCH / OPB Clock Fmax (MHz)	DDR Device Clock Fmax (Mhz)
1	1	0	0	0	0	0	1	16	0	362	306	476	132.2	N/A
2	1	0	0	0	0	0	4	16	0	400	308	509	130.9	N/A
3	2	0	0	0	0	0	1	16	0	556	419	759	127.4	N/A
4	4	0	0	0	0	0	1	16	0	831	621	1141	123.1	N/A
4									1	1049	716	1343	126.3	N/A
5	2	1	0	0	0	0	1	16	0	980	681	916	126.7	N/A
6	2	1	1	0	0	0	1	16	0	1000	707	1134	117.3	N/A
6									1	988	797	1300	124.9	N/A
7	4	1	1	0	0	0	1	16	0	1299	898	1537	87.9	N/A
7									1	1348	994	1724	99.9	N/A
8	2	0	0	1	0	0	1	16	0	850	568	1005	125.3	139.9
9	2	1	0	1	0	0	1	16	0	1070	828	1163	125.0	164.6
10	2	1	1	1	0	0	1	16	0	1138	844	1374	116.8	146.1
11	2	1	0	0	1	0	1	16	0	990	699	998	119.6	N/A
11									1	1051	793	1162	125.3	N/A
12	2	1	1	0	1	0	1	16	0	1040	719	1211	116.0	N/A
12									1	1101	815	1373	121.3	N/A
13	2	1	1	0	1	0	2	16	0	1055	734	1414	96.7	N/A
13									1	1032	828	1516	114.6	N/A
14	2	1	1	1	1	0	2	16	0	1197	896	1698	85.9	151.1
14									1	1294	995	1774	114.6	148.5
15	2	1	0	1	0	1	2	16	0	1092	898	1268	109.3	160.8
16	2	1	0	1	1	1	2	16	0	1212	915	1474	90.9	157.2
16									1	1311	1026	1556	124.1	150.0
17	2	1	1	1	1	1	2	16	0	1223	941	1700	85.0	170.0
17									1	1309	1041	1770	116.0	163.1
18	2	1	1	0	0	0	1	32	0	1075	774	1312	104.7	N/A
18									1	1128	874	1449	125.1	N/A
19	2	1	1	1	1	0	1	32	0	1333	1004	1773	100.7	152.6
19									1	1389	1099	1845	125.0	147.2

The MCH OPB DDR SDRAM controller benchmarks are shown in Table 11 for a Virtex-4 XC4VLX60 -11 FPGA.

Table 11: **FPGA Performance and Resource Utilization (Virtex-4)**

Run #	Parameter Values									Device Resources			Performance	
	C_NUM_CHANNELS	C_INCLUDE_OPB_IPIF	C_INCLUDE_OPB_BURST	C_DDR_ASYNC_SUPPORT	C_USE_OPEN_ROW_MNGT	C_REG_DIMM	C_NUM_BANKS_MEM	C_DDR_DWIDTH	C_INCLUDE_DDR_PIPE	Slices	Slice FFs	4-input LUTs	MCH / OPB Clock Fmax (MHz)	DDR Device Clock Fmax (Mhz)
1	1	0	0	0	0	0	1	16	0	366	306	494	162.4	N/A
2	1	0	0	0	0	0	4	16	0	372	309	516	136.2	N/A
3	2	0	0	0	0	0	1	16	0	567	430	782	136.7	N/A
4	4	0	0	0	0	0	1	16	0	890	621	1189	126.6	N/A
4									1	1013	719	1399	126.8	N/A
5	2	1	0	0	0	0	1	16	0	824	682	994	133.6	N/A
6	2	1	1	0	0	0	1	16	0	909	707	1193	126.7	N/A
6									1	1026	801	1382	126.9	N/A
7	4	1	1	0	0	0	1	16	0	1184	902	1621	125.2	N/A
7									1	1349	998	1876	126.8	N/A
8	2	0	0	1	0	0	1	16	0	777	575	1059	127.4	217.8
9	2	1	0	1	0	0	1	16	0	992	830	1230	126.0	215.0
10	2	1	1	1	0	0	1	16	0	1096	851	1510	125.6	175.4
11	2	1	0	0	1	0	1	16	0	887	696	1049	125.6	N/A
11									1	1025	798	1296	127.5	N/A
12	2	1	1	0	1	0	1	16	0	948	716	1301	125.6	N/A
12									1	1074	820	1461	126.2	N/A
13	2	1	1	0	1	0	2	16	0	1039	735	1508	117.3	N/A
13									1	1160	839	1604	126.7	N/A
14	2	1	1	1	1	0	2	16	0	1229	895	1772	107.3	164.9
14									1	1393	1013	1878	126.0	144.1
15	2	1	0	1	0	1	2	16	0	1110	909	1364	125.3	210.5
16	2	1	0	1	1	1	2	16	0	1159	920	1570	114.9	212.4
16									1	1351	1051	1685	126.1	156.1
17	2	1	1	1	1	1	2	16	0	1260	944	1776	110.2	198.45
17									1	1416	1073	1878	127.6	192.5
18	2	1	1	0	0	0	1	32	0	1033	786	1420	126.9	N/A
18									1	1154	882	1531	126.9	N/A
19	2	1	1	1	1	0	1	32	0	1337	1013	1852	114.4	161.2
19									1	1459	1117	1932	126.8	154.2

Reference Documents

The following documents contain reference information important to understanding the MCH OPB DDR SDRAM Controller design:

1. MicroBlaze Processor Reference Guide, UG081.
2. MCH OPB IPIF Specification, DS494.
3. OPB DDR SDRAM Specification, DS424.

Revision History

Date	Version	Revision
06/15/05	1.0	Initial release.
7/1/05	1.1	Incorporated CR211535 to update async clock freq support.
7/28/05	1.2	Added XCL timing diagrams.
11/2/05	1.3	Fixed CR 210313, 210315, and 210316. Revised version # of core to v1.00b.
11/15/05	1.4	Updated DWIDTH parameters allowable values.