Multi-Gigabit Transceiver (MGT) Protector (v1.00a)

DS605 April 24, 2009 **Product Specification**

Introduction

The MGT Protector core puts uninstantiated Multi-Gigabit Transceivers (MGTs) on the device into a safe activity mode. This is required because of the Negative-Bias Temperature Instability (NBTI) of the Virtex®-4 device MGTs.

For more information relating to the Virtex-4 device RocketIO™ MGT Static Operating Behavior, see:

- EN014, Errata for Virtex-4 FX FPGA CES2 and CES3 Devices
- EN042, Errata for Virtex-4 FPGA CES4 Devices

This core is intended to be used when one or both MGTs in a tile will be used in the future, but neither MGT is instantiated in the current design. For other workarounds, see Xilinx XAPP732, *Inactive Transceiver Behavior Work-Arounds for Virtex-4 FX RocketIO MGTs*, and Xilinx Answer Records 21127, 23410.

Features

- Configurable number of tiles.
- Configurable Port LOC constraints.

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	See EDK Supported Device Families.	
Version of Core	mgt_protector	v1.00a
Resources Used		
	Min	Max
Slices	0	0
LUT	0	0
FFs	0	0
Block RAMs	0	0
GT11	2	32
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

Functional Description

The block diagram for the MGT protector is shown in Figure 1.

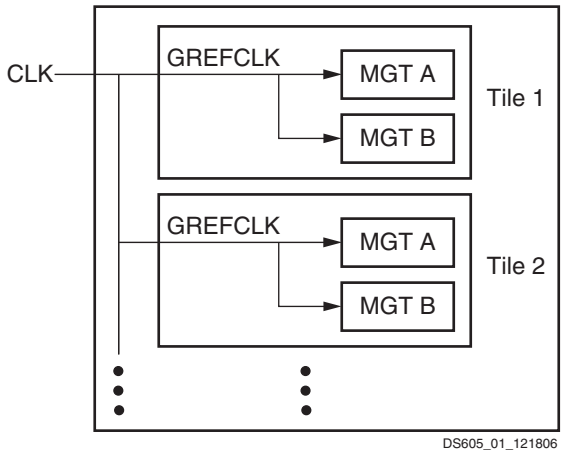

Figure 1: **MGT Protector Block Diagram**

The core instantiates macros for both MGTs in each tile that has been marked to be protected. The drop in macros are available at:

http://www.xilinx.com/xlnx/xweb/xil_publications_file.jsp?iLanguageID=1&ipoid=24332297&category=-1210767&filename=Null_Tile.zip&file=539

Note: This link prompts the user to log in to a xilinx.com account and accept a license agreement. After doing so, click on the **Download Design File** link.

The core delivers the bus clock to the GREFCLK pins on the MGTs and puts each individual MGT into a safe activity mode.

MGT Protector I/O Signals

Table 1: **MGT Protector Signal Descriptions**

Signal Name	Interface	I/O	Description
CLK	None	I	Input Clock

MGT Protector Parameters

Table 2: MGT Protector Parameters

Parameter Name	Parameter Description	Default Value	VHDL Type
C_NUM_TILES	Number of MGT tiles in the device.	16	integer
C_LOC_*i*_AB (*i* is an integer value from 1 to C_NUM_TILES)	LOC constraint for the MGT pair on the tile	NOT_SET	string
C_USE_*j* (*j* is an integer value from 1 to C_NUM_TILES)	Instantiate a macro for tile using C_LOC_*j*_AB if the parameter value is 1	1	std_logic

Allowable Parameter Combinations

The number of C_LOC constraint parameters and the number of C_USE parameters should be equal to the value of C_NUM_TILES parameter.

Parameter - Port Dependencies

Not applicable.

MGT Protector Register Descriptions

Not applicable.

MGT Protector Interrupt Descriptions

Not applicable.

Design Implementation

Design Tools

The MGT Protector design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the MGT Protector.

Target Technology

The intended target technology is an FPGA of the Virtex-4 family containing one or more MGT tiles.

Device Utilization and Performance Benchmarks

This core does not contain any logic. It utilizes two MGTs for each tile chosen to be protected. There are no performance benchmarks available.

Specific Exceptions

Not applicable.

Reference Documents

Not applicable.

Revision History

Date	Version	Revision
12/18/2005	1.0	Initial release.
4/24/09	1.1	Replaced references to supported device families and tool names with hyperlink to PDF file.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

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