7 Series FPGAs Memory Interface Solutions (v1.7)

DS176 October 16, 2012 **Advance Product Specification**

Introduction

The Xilinx® 7 series FPGAs memory interface solutions cores provide high-performance connections to DDR3 and DDR2 SDRAMs, QDRII+ SRAM, and RLDRAM II/RLDRAM III.

DDR3 and DDR2 SDRAMs

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in DDR3 and DDR2 SDRAMs. These solutions are available with an optional AXI4 slave interface.

DDR3 SDRAM Features

- Component support for interface widths up to 72 bits
- Single and dual rank UDIMM, RDIMM, and SODIMM support
- DDR3 (1.5V) and DDR3L (1.35V)
- 1, 2, and 4 Gb density device support
- 8-bank support
- x8 and x16 device support
- 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 72 bits)
- 8-word burst support
- Support for 5 to 14 cycles of column-address strobe (CAS) latency (CL)
- On-die termination (ODT) support
- Support for 5 to 10 cycles of CAS write latency
- ZQ calibration – initial and periodic (configurable)
- Write leveling support for DDR3 (fly-by routing topology required for DDR3 component designs)
- JEDEC-compliant DDR3 initialization support
- Source code delivery in Verilog and VHDL (top-level files only)
- 4:1 and 2:1 memory to FPGA logic interface clock ratio
- ECC support
- I/O Power Reduction option reduces average I/O power by automatically disabling DQ/DQS IBUFs and internal terminations during writes and periods of inactivity
- Internal V_{REF} support
- Multicontroller support for up to eight controllers
- Two controller request processing modes:
  - Normal: reorder requests to optimize system throughput and latency
  - Strict: memory requests are processed in the order received

LogiCORE™ IP Facts Table							
Core Specifics							
Supported Device Family(1)	Zynq™-7000(2), Artix™-7, Virtex®-7(3), and Kintex™-7(3)						
Supported Memory	DDR3 Component and DIMM, DDR2 Component and DIMM, QDRII+, and RLDRAM II Components						
Resources	**Product(4)**	**LUTs**	**Flip-Flops**	**BUFG**	**PLLE2**	**MMCM**	**Block RAM**
	7 Series FPGAs DDR3 SDRAM	10,554	6,682	2	1	1	0
	7 Series FPGAs DDR2 SDRAM	7,633	4,588	2	1	1	0
	7 Series FPGAs QDRII+ SRAM	2,536	2,117	2	1	1	0
	7 Series FPGAs RLDRAM II	5,134	3,308	2	1	1	0
	7 Series FPGAs RLDRAM III	8,731	5,259	2	1	1	0
Provided with Core							
Documentation	Product Specification User Guide						
Design Files	Verilog, VHDL (top-level files only)						
Example Design	Verilog, VHDL (top-level files only)						
Test Bench	Not Provided						
Constraints File	ISE: UCF Vivado: XDC						
Supported S/W Driver	N/A						
Tested Design Flows(5)							
Design Entry	ISE Design Suite v14.3 Vivado Design Suite v2012.3(6)						
Simulation (Behavioral only)	ISim(7) (Verilog designs only), Mentor Graphics ModelSim Vivado Simulator(7)						
Synthesis	XST, Synopsys Synplify Pro Vivado™ Synthesis						
Support							
Provided by Xilinx @ www.xilinx.com/support							

Notes:

1. For a complete listing of supported devices, see the release notes for MIG.
2. Supported in ISE® Design Suite implementations only.
3. See the *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics* or the *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* for performance information.
4. Resource utilization can change depending on the options chosen, memory device used, or both. Resource information is provided for 72-bit DDR3 SDRAM, 72-bit DDR2 SDRAM, 36-bit QDRII+ SRAM, 72-bit RLDRAM II, and 72-bit RLDRAM III interfaces.
5. For the supported versions of the tools, see the *Xilinx Design Tools: Release Notes Guide*.
6. Supports only 7 series devices.
7. ISim and Vivado Simulators are supported for DDR3 SDRAM, DDR2 SDRAM, QDRII+ SRAM, and RLDRAM II.

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DDR2 SDRAM Features

- Component support for interface widths up to 64 bits
- Single rank UDIMM, RDIMM, and SODIMM
- 1 and 2 Gb density device support (additional densities supported in the MIG tool using the Create Custom Part feature)
- 4- and 8-bank support
- x8 and x16 device support
- 8:1 DQ:DQS ratio support
- Configurable data bus widths (multiples of 8, up to 72 bits)
- 8-word burst support
- Support for 3 to 6 cycles of column address strobe (CAS) latency
- On-die termination (ODT) support
- JEDEC-compliant DDR2 initialization support
- Source code delivery in Verilog and VHDL (top-level files only)
- 4:1 and 2:1 memory to FPGA logic interface clock ratio
- ECC support
- I/O Power Reduction option reduces average I/O power by automatically disabling DQ/DQS IBUFs and internal terminations during writes and periods of inactivity
- Internal V_{REF} support
- Two controller request processing modes:
  - Normal: Reorder requests to optimize system throughput and latency
  - Strict: Memory requests are processed in the order received
- Multiple controllers per FPGA supported running the MIG tool multiple times

Applications

Typical applications for the Xilinx 7 series FPGAs memory interface solutions include DDR3 SDRAM and DDR2 SDRAM interfaces.

Figure 1 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to a DDR2 or DDR3 SDRAM device. The physical layer (PHY) side of the design is connected to the DDR2 or DDR3 SDRAM device through FPGA I/O blocks (IOBs), and the user interface side is connected to the user design through FPGA logic. See *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) for more details regarding the design.

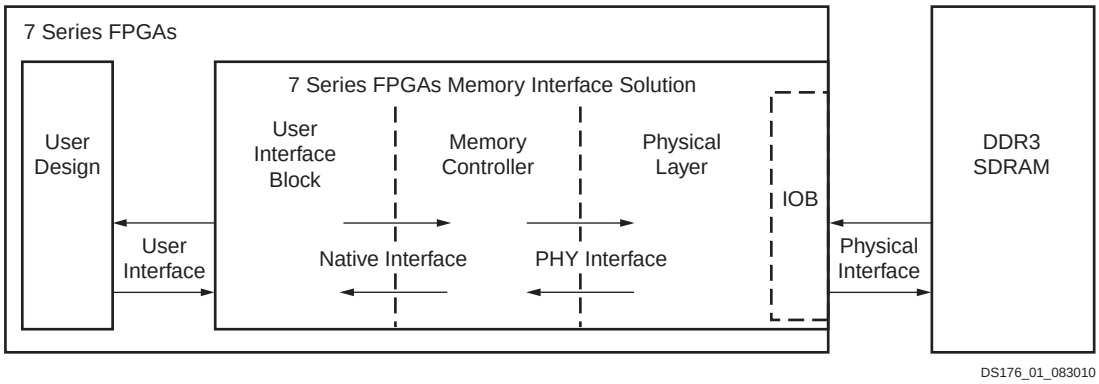

Figure 1: **DDR2/DDR3 SDRAM Memory Interface Solution**

Functional Description

As shown in Figure 1, the top-level functional blocks of the Xilinx 7 series FPGAs memory interface solution include:

- The User Interface block:
  - Presents the user interface to a user design
  - Provides a simple and user-friendly alternative to the native interface
  - Buffers read and write data
  - Reorders read return data to match the request order
  - Presents a flat address space and translates it to the addressing required by the SDRAM
- The Memory Controller block:
  - Receives requests from the user design
  - Reorders requests to minimize dead states for maximum SDRAM performance
  - Manages SDRAM row/bank configuration
  - Performs high-level SDRAM management such as refresh and activate/precharge
- The PHY block:
  - Interfaces with the Memory Controller block over a simple interface and translates the signals into the actual signals sent to the SDRAM, and vice versa
  - Translates and synchronizes control and data over various clock domains
  - Initializes the SDRAM
  - Performs write leveling for DDR3 (fly-by routing topology required for component designs)
  - Performs calibration to center align capture clocks with read data

Figure 1 also shows a user design connecting to the memory interface. An example user design is provided with the core. See *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) for more details regarding the design.

AXI4 Slave Interface Features

These features are optional and selectable using the MIG GUI:

- AMBA® AXI4 slave-compliant memory-mapped interface
- AXI4-Lite interface support for ECC control and status registers
- 1:1 clock rate to the controller

- AXI4 interface data widths can be 64, 128, 256, or 512 bits to correspond with memory data widths of 8, 16, 32, 64, or 72 bits
- Parameterized address width support
- Support for incremental (INCR) burst up to 256 data beats
- WRAP burst support
- Multicontroller support for up to eight DDR3 SDRAM controllers

QDRII+ SRAM

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in QDRII+ SRAMs.

Features

- QDRII+ SRAM device support
- x18 and x36 memory width support
- Configurable data bus widths (x18, x36)
- 2-word and 4-word burst support
- Source code delivery in Verilog only
- 2:1 memory to FPGA logic interface clock ratio
- 2.0-cycle and 2.5-cycle read latency support
- Fixed latency mode support
- Internal V_{REF} support
- Multicontroller support for up to eight controllers

Applications

QDRII+ SRAMs offer high-speed data transfers on separate read and write buses on the rising and falling edges of the clock. These memory devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers

Figure 2 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to a QDRII+ SRAM device.

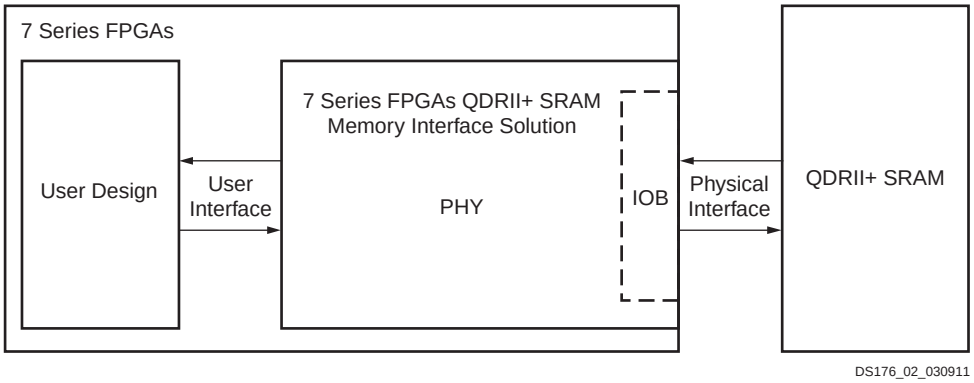

Figure 2: **QDRII+ SRAM Memory Interface Core**

Functional Description

As shown in Figure 2, the top-level functional block is composed of a PHY that interfaces to the user and to the QDRII+ SRAM device. The PHY block:

- Translates simple user read and write commands to conform to QDRII+ SRAM protocol
- Enables the user to provide up to one read and one write transaction per clock cycle for maximum throughput
- Performs calibration to center align clocks with data
- Returns data to the user with a corresponding valid signal
- Translates and synchronizes over various clock domains
- Implements an optimized half-frequency design that eliminates the need for a memory controller

For more details regarding the design, see *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) provided with the core.

RLDRAM II/RLDRAM III

This section discusses the features, applications, and functional description of Xilinx 7 series FPGAs memory interface solutions in RLDRAM II/RLDRAM III devices.

RLDRAM II Features

- RLDRAM II common I/O (CIO) memory device support
- x18 and x36 memory width support
- Configurable data bus widths (x18, x36, x72)
- 4-word and 8-word burst support
- Configuration 1, 2, 3 support
- Address Multiplexing Mode support
- ODT support
- Source code delivery in Verilog only
- 2:1 memory to FPGA logic interface clock ratio
- Internal V_{REF} support

- Multicontroller support for up to eight controllers

RLDRAM III Features

- x18 and x36 memory width support
- Configurable data bus widths (x18, x36, x72)
- 2-word, 4-word, and 8-word burst support
- Address Multiplexing Mode support
- ODT support
- Source code delivery in Verilog only
- 4:1 memory to FPGA logic interface clock ratio
- Internal V_{REF} support

Applications

RLDRAM II and RLDRAM III devices are used in high-performance systems as temporary data storage, such as:

- Look-up tables in networking systems
- Packet buffers in network switches
- Cache memory in high-speed computing
- Data buffers in high-performance testers

Figure 3 shows a high-level block diagram of the 7 series FPGAs memory interface solution connecting a user design to an RLDRAM device. The physical layer is connected to the RLDRAM device through FPGA IOBs, and the user interface is connected to the user design through FPGA logic.

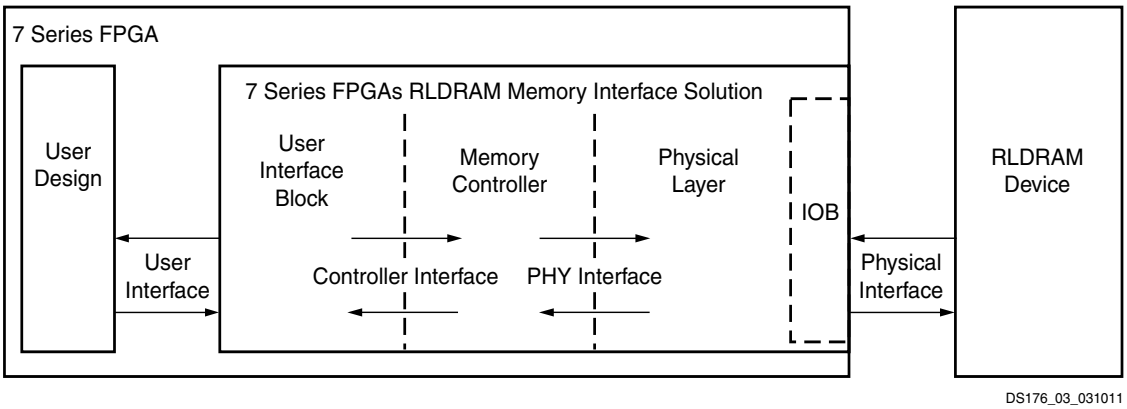

Figure 3: **RLDRAM Memory Interface Core**

Functional Description

As shown in Figure 3, the top-level functional blocks of the RLDRAM memory interface solution include:

- The User Interface block:
  - Presents the user interface to a user design
  - Buffers commands and write data
- The Memory Controller block:
  - Receives requests from the user design
  - Processes commands in order and adheres to memory specifications

  - Performs high-level SDRAM management, such as refresh, and controls bank access
- The Physical Layer (PHY) block:
  - Interfaces with the Memory Controller block over a simple interface and translates the signals into the actual signals sent to the RLDRAM, and vice versa.
  - Performs memory initialization sequence.
  - Performs calibration to center align clocks with data
  - Returns data to the user with a corresponding valid signal

For more details regarding the design, see *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) provided with the core.

General Specifications

See the *7 Series FPGAs Memory Interface Solutions User Guide* for more details regarding specific banking, pin location, and internal clock resource requirements for all cores.

Verification

Xilinx 7 series FPGAs memory interface solutions cores have been verified in simulation. Verification tests include:

- Initialization sequence
- Read calibration
- Memory read operation
- Memory write operation
- Row/bank management
- Write leveling

Additional Resources

This section provides additional information related to this data sheet:

- JEDEC Standard JESD79-3E: DDR3 SDRAM, JEDEC Solid State Technology Association
  JEDEC Standard JESD79-2F: DDR2 SDRAM Specification, JEDEC Solid State Technology Association
  www.jedec.org

This Xilinx document can be located on the MIG Solution Center Documentation page:

- UG586, *7 Series FPGAs Memory Interface Solutions User Guide*

The data sheets for the Xilinx 7 series FPGAs can be located at
www.xilinx.com/support/documentation/7_series.htm:

- DS183, *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics*
- DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*

Licensing and Ordering Information

The Memory Interface Generator (MIG) is included at no additional charge with the Xilinx ISE® Design Suite software and is provided under the terms of the Xilinx Core License Agreement. The memory cores are generated

using the Xilinx CORE Generator™ software, which is a standard component of the Xilinx ISE software. For more information, visit the MIG product page.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/01/11	1.0	Initial Xilinx release.
06/22/11	1.1	ISE 13.2 software release. Added RLDRAM II support throughout document. Added single rank UDIMM support bullet to DDR3 SDRAM Features, page 1. Added internal Vref support.
10/19/11	1.2	ISE 13.3 software release for MIG v1.3. • Added Resources to the IP Facts table. • For DDR3 SDRAM, added support for up to eight controllers, added 2:1 as an interface clock ratio, added AXI4-Lite interface support, and added 72 as a memory data width option. • For QDRII+ SRAM, added support for 2-word bursts and support for up to eight controllers. • For RLDRAM II, added support for Address Multiplexing Mode and support for up to eight controllers.
01/18/12	1.3	ISE 13.4 tool release for MIG v1.4. • For DDR3 SDRAM: Added support for 4 Gb density, DDR3L (1.35 V), and dual rank UDIMM, RDIMM, and SODIMM. Removed support for AXI4-Lite interface and 72-bit data width. • Added DDR2 SDRAM support.
04/24/12	1.4	ISE 14.1 tool release for MIG v1.5. • Added VHDL source code for top-level files for all memory devices • For DDR3 and DDR2 SDRAM, added: I/O Power Reduction option, AXI4-Lite interface support for ECC control and status registers, and 72-bit data width.
07/25/12	1.5	ISE 14.2 and Vivado 2012.2 Design Suite releases for MIG v1.6.
10/16/12	1.6	ISE 14.3 and Vivado 2012.3 Design Suite releases for MIG v1.7. Added RLDRAM III content.

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