



Features

- Supported FPGA families: Virtex®-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan®-3, and Spartan-3A
- MPEG-4 Part 2 Simple Profile Level 5 (Standard Definition)
- User-defined maximum frame size
- Directional squared motion estimation with early stop
- Half-pixel motion estimation
- 4:2:0: YUV processing
- Single external frame buffer; predicted frame processing
- Variable length coding in hardware
- Host interface for rate control algorithm
- Support for full MPEG-4 header

Applications

Applications for the MPEG-4 Simple Profile Encoder core are:

- **Automotive** – Global Positioning Systems (GPS), collision avoidance systems, and video compression technology.
- **Medical Imaging** – Medical imaging, processing, and archival for both still and video images in non-clinical application setting.
- **Industrial and Security** – Video sequencing from multiple locations to a central processing location.
- **Broadcasting** – Transmitting information in a highly compressed format to deliver high-quality video both inside and outside studios, as in HDTV.
- **Military** – Video surveillance from military aircraft over wireless communication channels.
- **Video Conferencing** – Transmitting high-quality video to multiple sites in real time.
- **Streaming Video** – Internet communications technology.
- **Video Messaging** – Cellular telephones, including video and small-screen applications.

General Description

The Xilinx® MPEG-4 Part 2 Simple Profile Encoder (MPEG-4 Encoder) core is a fully functional VHDL design implemented on a Xilinx FPGA. The MPEG-4 Encoder core accepts uncompressed video and generates compressed bitstreams based on the “Information Technology–Generic Coding of Audio Visual Objects–Part 2 Visual” section of the ISO/IEC 14496-2 standard. For a list of unsupported features, see the MPEG-4 Simple Profile Encoder Data Sheet (DS511).

Resources

Table 1: Virtex-4, Virtex-II Pro, Virtex-II, Spartan-3, Spartan-3A FPGA Resource Usage

Resources Used	Slices	LUTs	FFs	Block RAMs	Mults/DSP48s
QCIF	8,303	12,630	6,093	16	17
CIF	9,019	12,778	6,335	23	17
4CIF	9,353	13,260	6,598	36	17
QCIF with Memory Controller	9,138	13,036	6,575	20	17
CIF with Memory Controller	9,251	13,085	6,650	27	17
4CIF with Memory Controller	9,639	13,592	6,944	40	17

Table 2: Virtex-5 FPGA Resource Usage

Resources Used	LUTs	FFs	Block RAMs	DSP48s
QCIF without Memory Controller	9,859	5,643	11	18
CIF without Memory Controller	9,848	5,780	13	18
4CIF without Memory Controller	10,050	6,067	20	18
QCIF with Memory Controller	10,148	6,021	14	18
CIF with Mem Controller	10,165	6,163	17	18
4CIF with Mem Controller	10,336	6,448	23	18

Support and Ordering Information

The MPEG-4 Simple Profile Encoder product, sold as netlist, is provided under the [LogiCORE Core Site License Agreement](#). A free evaluation version is available from Xilinx DSP marketing or from your local Xilinx [sales representative](#).

For part number information, go to the MPEG-4 Simple Profile product page on the Xilinx [IP Center](#). To purchase the core, contact your local Xilinx sales representative.

Revision History

Date	Version	Revision
10/20/05	1.0	Initial Xilinx release.
09/19/06	1.1	Updated for Virtex-5 FPGAs.
04/14/08	1.2	Updated for core version 1.2.

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