LogiCORE IP OBSAI v4.2

DS612 July 23, 2010 **Product Specification**

Introduction

The LogiCORE™ IP OBSAI core implements an OBSAI RP3 interface supporting RP3-01 at 768 Mbps, 1.5 Gbps, and 3 Gbps line rates using GTP or GTX transceivers in Virtex®-5, Spartan®-6 and Virtex-6 FPGAs. 6 Gbps line rate is supported in Virtex-6 devices.

The OBSAI core can be configured as a master or slave for use in base station or Remote RF Units (RRUs).

Features

- Designed to *OBSAI RP3 v4.2* specification[Ref 1]
- Supports CDMA or WCDMA/WiMAX 802.16/LTE framing formats
- GTP or GTX Transceivers support 768 Mbps, 1.5 Gbps, and 3 Gbps line rates in Virtex-5 devices
- GTPA1 Transceivers support 768 Mbps, 1.5 Gbps, and 3 Gbps line rates in Spartan-6 devices
- GTXE1 Transceivers support 768 Mbps, 1.5 Gbps, 3 Gbps and 6 Gbps line rates in Virtex-6 devices
- Physical and Data Link Layer functions provided
- Supports RP1 Ethernet Messages[Ref 2], [Ref 3]
- Ethernet interface connects directly to LogiCORE IP MACs
- Supports RP1 Frame Clock Burst Messages
- Provides dedicated serial interfaces for RP1 frame clock bursts
- Creates and processes Round Trip Time (RTT) messages
- Creates (Master mode core) or processes (Slave mode core) HW Reset Messages
- Provides Generic RP3 Messaging interfaces to support Application Layer messaging
- Supports RP3-01 auto-negotiation
- Microprocessor-neutral configuration interface

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Virtex-5 LXT/SXT/FXT[2] Virtex-6 LXT/SXT/HXT/CXT Spartan-6 LXT			
Resources Used[3]	**Slices**	**LUTs**	**FFs**	**Block RAMs**
	870-1600	1680-3250	1360-2520	0 - 5
Special Features	Delivered through CORE Generator™ software Hardware Verified			
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	NGC netlist			
Constraints File	User Constraints File (.ucf)			
Verification	VHDL Test Bench			
Example Design	VHDL			
Design Tool Requirements				
Xilinx® Implementation Tools	ISE® v12.2			
Simulation Tools[4]	Mentor Graphics ModelSim v6.5c and above			
Synthesis	XST			
Support				
Provided by Xilinx, Inc.@ www.xilinx.com/support				

1. For the complete list of supported devices, see the release notes for this core.
2. Virtex-5 LX20T FPGA is not supported due to clocking resource limitations.
3. Figures quoted are approximate for Virtex-5 FPGA default configuration. See Table 1, Table 2 and Table 3 for detailed information.
4. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Overview

OBSAI RP3 is a high-speed serial interface designed to connect radio and baseband units within a wireless system. OBSAI RP3-01 is an extension to RP3, which provides the ability to site Remote RF Units (RRUs) at a different location from the Baseband Unit (BBU). RP3-01 enables RP1 messages defined in the *OBSAI RP1 Specification v2.1*[Ref 2] to be passed using only the RP3 physical interface. In RP3-01, the same serial RP3 interface carries both data and control information. The OBSAI RP3-01 interface is specified in the *OBSAI RP3 v4.2* specification[Ref 1].

Applications

Figure 1 shows a typical OBSAI system with a RRU.

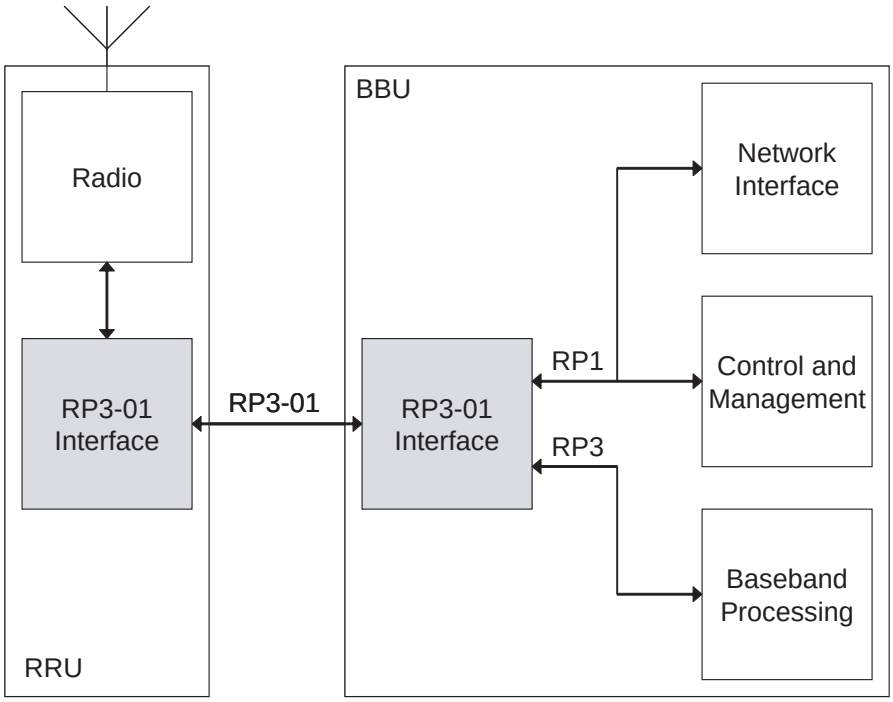

Figure 1: **OBSAI RP3-01 Link Between BBU and RRU**

Functional Description

Figure 2 illustrates a block diagram of the OBSAI RP3-01 core implementation.

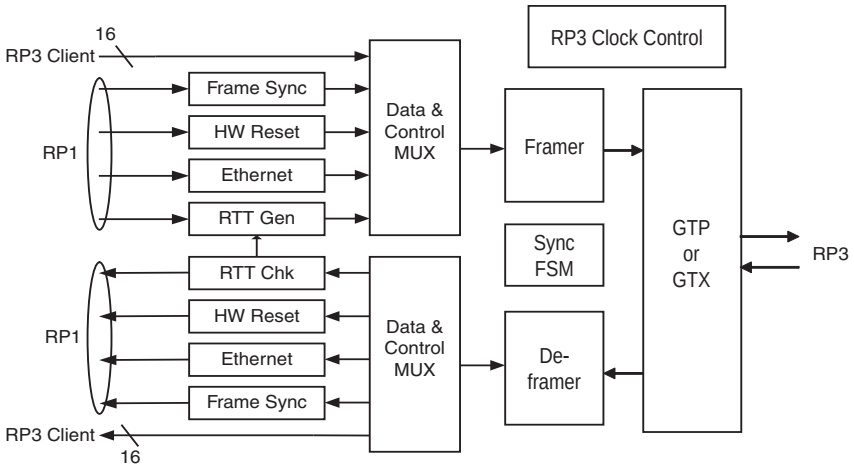

Figure 2: **OBSAI Core Implementation**

The major functional blocks of the core include the following:

- **Transmit Data and Control Multiplexer**. Inserts Control Messages in the RP3 data stream during control slots or empty data slots if permitted.
- **Transmit RP3-01 Control Interfaces**. Ethernet, O&M, and Timing Synchronizations Messages can be inserted in the RP3 data stream.
- **Transmit RP3 Generic Message Interface**. Allows the transmission of Application Layer generated RP3 messages such as Generic Control or Generic Packet types.
- **RP3 Transmit Framer**. Creates a single stream to the device-specific transceiver.
- **RP3 Receive De-framer**. Extracts messages from the data from the device-specific transceiver.
- **Receive Data and Control Demultiplexer**. Extracts Control messages from the stream and passes them to the RP3-01 control interfaces.
- **ReceiveRP3-01 Control Interfaces**. Extracts the Ethernet, O&M, and Frame Clock Burst data from the Control Messages.
- **Receive RP3 Generic Message Interface**. Extracts selected RP3 message types such as Generic Control or Generic Packet types and passes them to a separate interface for Application Layer use.
- **Clock Control**. Manages the switching of the GTP or GTX transceiver speed and generates the correct clocks to the other parts of the core and to the higher-layer logic created by the user.

Device Utilization

Virtex-5 FPGAs

Table 1 provides approximate device utilization figures for core configured to support WCDMA framing format on a Virtex-5 SXT or LXT device. The values include the RocketIO™ transceiver and clock control logic.

Table 1: **Device Utilization - Virtex 5 FPGA**

Parameter Values				Device Resources					
Mode	**Master/ Slave**	**Include Ethernet**	**Include Generic Messaging**	**LUTs**	**Registers**	**Block RAM (18K)**	**PLL**	**BUFG**	**BUFR**
RP3	Master	N/A	N/A	1680	1360	1	1	4	1
	Slave	N/A	N/A	1665	1360	0	1	4	1
RP3-01	Master	N	N	2700	1930	1	1	4	1
	Master	Y	N	3250	2520	5	1	4	1
	Master	N	Y	2970	2270	3	1	4	1
	Slave	N	N	2660	2140	0	1	4	1
	Slave	Y	N	3200	2730	4	1	4	1
	Slave	N	Y	2930	2480	2	1	4	1

Note: All configurations use a single GTP_DUAL tile (FXT/LXT) or GTX_DUAL tile (FXT)

Virtex-6 FPGAs

Table 2 provides approximate device utilization figures for core configured to support WCDMA framing format on a Virtex-6 LXT device. The values include the GTXE1 transceiver and clock control logic.

Table 2: **Device Utilization - Virtex 6 FPGA**

Parameter Values				Device Resources					
Mode	**Master/ Slave**	**Include Ethernet**	**Include Generic Messaging**	**LUTs**	**Registers**	**Block RAM (18K)**	**MMCM**	**BUFG**	**BUFR**
RP3	Master	N/A	N/A	1790	1340	1	1	4	1
	Slave	N/A	N/A	1780	1350	0	1	4	1
RP3-01	Master	N	N	2830	1910	1	1	4	1
	Master	Y	N	3460	2490	5	1	4	1
	Master	N	Y	3140	2240	3	1	4	1
	Slave	N	N	2980	2130	0	1	4	1
	Slave	Y	N	3580	2710	4	1	4	1
	Slave	N	Y	3290	2460	2	1	4	1

Note: All configurations use a single GTXE1 transceiver.

Spartan-6 FPGAs

Table 3 provides approximate device utilization figures for core configured to support WCDMA framing format on a Spartan-6 LXT device. The values include the GTPA1 transceiver and clock control logic.

Table 3: **Device Utilization - Spartan-6 FPGA**

Parameter Values				Device Resources							
Mode	Master/ Slave	Include Ethernet	Include Generic Messaging	LUTs	Registers	Block RAM (18K)	PLL	DCM	BUFG	BUFIO2	BUFIO2FB
RP3	Master	N/A	N/A	1400	1330	1	1	1	5	2	2
	Slave	N/A	N/A	1380	1340	0	1	1	5	2	2
RP3-01	Master	N	N	2280	1900	1	1	1	5	2	2
	Master	Y	N	2750	2490	5	1	1	5	2	2
	Master	N	Y	2500	2240	3	1	1	5	2	2
	Slave	N	N	2550	2150	0	1	1	5	2	2
	Slave	Y	N	2860	2740	4	1	1	5	2	2
	Slave	N	Y	2620	2480	2	1	1	5	2	2

Note: All configurations use a single GTPA1 transceiver.

References

1. *OBSAI RP3 Specification v4.2* (www.obsai.com)
2. *OBSAI RP1 Specification v2.1*. (www.obsai.com)
3. *IEEE Standard 803.3-2005* (www.standards.ieee.org/getieee802/)

Support

Please visit www.xilinx.com/support for technical support. Xilinx provides technical support for this product when used as described in product documentation. Xilinx cannot guarantee timing, functionality,or support of product if implemented in devices that are not listed in the documentation or if customized.

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License. The core is generated using the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite.

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Related Information

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Revision History

Date	Version	Revision
8/8/07	1.0	Initial Xilinx release.
3/24/08	1.2	Update core to version 1.2; Xilinx tools v10.1.
4/16/08	2.1	Update core to version 2.1; Add FXT support.
4/24/09	3.1	Update core to version 3.1; Add RP3 v4.1 and Virtex-6 FPGA support.
6/24/09	3.2	Update core to version 3.2; Xilinx tools v11.2.
9/16/09	3.3	Update core to version 3.3; Xilinx tools v11.3.
4/19/10	4.1	Update core to version 4.1; Xilinx tools v12.1. Add 6G line rate and Spartan-6 FPGA support.
7/23/10	4.2	Update core to version 4.2; Xilinx tools v12.2.

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