OPB Block RAM (BRAM) Interface Controller

DS468 December 1, 2005 Product Specification

Introduction

The OPB BRAM Interface Controller is a module that attaches to the OPB (On-chip Peripheral Bus) .

This controller supports the OPB v2.0 byte enable architecture. Any access size up to the width of the OPB data bus is permitted. The OPB BRAM Interface Controller is the interface between the OPB and the bram_block peripheral. A BRAM memory subsystem consists of the controller along with the actual BRAM components that are included in the bram_block peripheral. If the text-based Microprocessor Hardware Specification (MHS) file is used for design entry, then the bram controller and bram_block must both be explicitly instantiated.

Features

- OPB V2.0 bus interface with byte-enable support
- Used in conjunction with bram_block peripheral to provide total BRAM memory solution
- Supports a wide range of memory sizes
- Handles Virtex, Virtex-E, Spartan-II, Virtex-II and Virtex-II Pro BRAM
- Handles byte, half-word, word and double word single transfers
- Burst support enabled by a design parameterread bursts must be word transfers

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Spartan-3E, Virtex, Virtex-II, Virtex-4, Virtex-E	
Version of Core	opb_bram_if_cntlr	v1.00a
Resources Used		
	Min	Max
Slices	25	34
LUTs	16	30
FFs	33	55
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

Functional Description

The OPB BRAM Interface Controller is the interface between the OPB and the bram_block peripheral. The OPBslave interface input/output signals are shown in Figure 1 and described in Table 1. See the OPB Signals in the On-Chip Peripheral Bus Architecture Specification (v2.0) for detailed functional description of the signals.

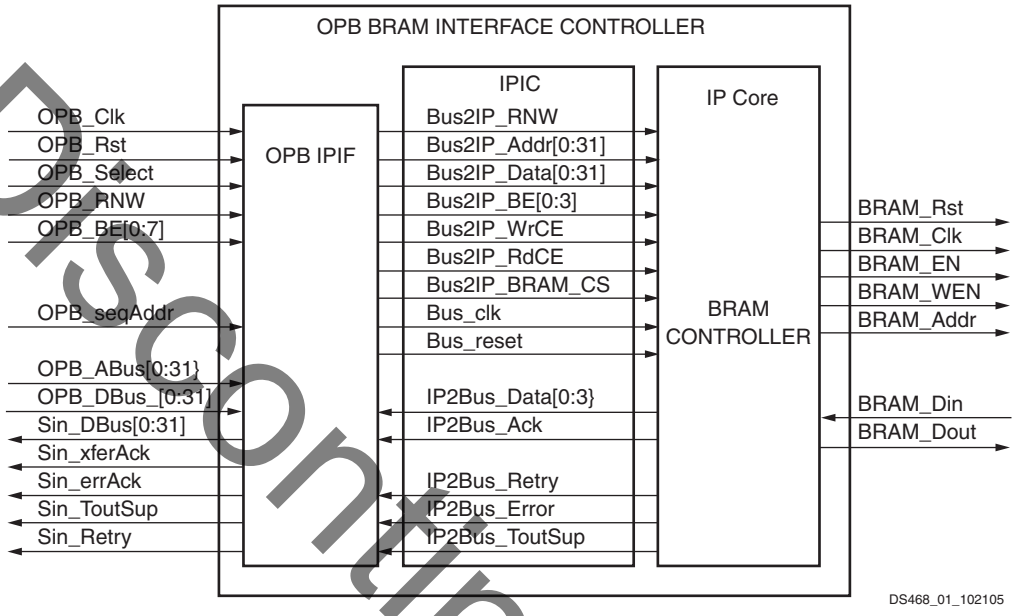

Figure 1: **OPB Slave Interface**

The OPB IPIF used in the OPB BRAM Interface Controller design allows for the inclusion/exclusion of pipeline registers to/from the OPB. The OPB BRAM Interface Controller design uses only the pipeline register stage for signals going from the core to the OPB. This allows for minimal latency in obtaining data from the BRAM memory. However, this means that there could be longer timing paths on the OPB bus signals, specifically OPB_Select. If the user determines that these timing paths become critical, the pipeline model of the OPB IPIF can be modified to include the pipeline register stage on signals coming from the OPB to the core. This is done by modifying the constant PIPELINE_MODEL from 4 to 5. This is detailed in the comments in the source code. Note however, that this will increase the transaction latency by 1 clock.

OPB BRAM Interface Controller I/O Signals

The I/O signals for the OPB BRAM Interface Controller are listed and described in Table 1.

Table 1: **OPBBRAM Interface Controller I/O Signals**

Signal Name	Interface	I/O	Description
OPB_Clk	OPB	I	OPB Clock
OPB_Rst	OPB	I	OPB Reset
OPB_ABus(0:C_OPB_AWIDTH-1)	OPB	I	OPB Address Bus
OPB_BE(0:C_OPB_DWIDTH/8-1)	OPB	I	OPB Byte Enables
OPB_DBus(0:C_OPB_DWIDTH-1)	OPB	I	OPB Data Bus
OPB_RNW	OPB	I	OPB Read, Not Write
OPB_select	OPB	I	OPB Select
OPB_seqAddr	OPB	I	OPB Sequential Address
Sln_DBus(0:C_OPB_DWIDTH-1)	OPB	O	Memory Controller Data Bus
Sln_errAck	OPB	O	Memory Controller Error Acknowledge
Sln_retry	OPB	O	Memory Controller Retry
Sln_toutSup	OPB	O	Memory Controller Timeout Suppress
Sln_xferAck	OPB	O	Memory Controller Transfer Acknowledge
BRAM_Rst	IP Core	O	BRAM Reset
BRAM_Clk	IP Core	O	BRAM Clock
BRAM_EN	IP Core	O	BRAM Enable
BRAM_WEN	IP Core	O	BRAM Write Enable
BRAM_Addr(0:C_OPB_AWIDTH-1)	IP Core	O	BRAM Address
BRAM_Din(0:C_OPB_DWIDTH-1)	IP Core	I	BRAM Data Input
BRAM_Dout(0:C_OPB_DWIDTH-1)	IP Core	O	BRAM Data Output

OPB BRAM Interface Controller Parameters

To allow you to obtain an OPB BRAM Interface Controller that is uniquely tailored for your system, certain features can be parameterized in the OPB BRAM Interface Controller design. This allows you to configure a design that only utilizes the resources required by your system, and operates with the best possible performance. The features that can be parameterized in Xilinx OPB BRAM Interface Controller designs are shown in Table 2.

Table 2: OPB **BRAM Interface Controller Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
OPBBRAM Base Address	C_BASEADDR	Valid Address Range(2)	None(1)	std_logic_vector
OPBBRAM HIGH Address	C_HIGHADDR	Valid Address Range(2)	None(1)	std_logic_vector
Include support for OPB burst(3)	C_INCLUDE_BURST_SUPPORT	0 = don't include logic to support OPB burst 1 = include logic to support OPB burst transfers	0	string
OPB Data Bus Width	C_OPB_DWIDTH	32	32	integer
OPB Address Bus Width	C_OPB_AWIDTH	32	32	integer
OPB Clock Period	C_OPB_CLK_PERIOD_PS	>0	40000	integer

Notes:
1. No default value is specified for C_BASEADDR and C_HIGHADDR to insure that the actual value is set; if the value is not set, a compiler error is generated. These generics must be a power of 2. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.
2. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power-of-two range, such that range = 2^n, and the n least significant bits of C_BASEADDR must be zero.Read bursts must be word transfers.

Programming Model

Supported Memory Sizes

The BRAM memory sizes listed in Table 3 are supported for Virtex, Virtex-E, and Spartan-II devices:

Table 3: **Supported BRAM Memory sizes for Virtex, Virtex-E, and Spartan-II**

Host Bus Size (bits)	Supported Memory Sizes (Bytes)
32	2KB, 4KB, 8KB, 16KB
64	4KB, 8KB, 16KB, 32KB

The BRAM memory sizes listed in Table 4 are supported for Virtex-II and Virtex-II Pro devices:

Table 4: **Supported BRAM Memory Sizes for Virtex-II and Virtex-II Pro**

Host Bus Size (bits)	Supported Memory Sizes (Bytes)
32	8KB, 16KB, 32KB, 64KB
64	16KB, 32KB, 64KB, 128KB

Example Base Address, High Address Specifications

The base address (C_BASEADDR) and high address (C_HIGHADDR) must specify a valid range for the BRAM that is attached to the BRAM Controller. The range (C_HIGHADDR – C_BASEADDR)

specified by the high address and base address must be equal to 2^n bytes, where n is a positive integer and 2^n is a valid memory size as shown above. In addition, the n least significant bits of C_BASEADDR must be equal to 0. Example address range specifications are listed in Table 5.

Table 5: **Example Address Range Specifications**

Memory Size (Bytes)	C_BASEADDR	C_HIGHADDR
2K	0x10000000	0x100007FF
4K	0x50000000	0x50000FFF
8K	0x24000000	0x24001FFF
16K	0xE0000000	0xE0003FFF
32K	0x3FF00000	0x3FF07FFF
64K	0x82000000	0x8200FFFF
128K	0xB0000000	0xB001FFFF

Parameter-Port Dependencies

The width of many of the BRAM Interface Controller signals depends on the number of memories in the system and the width of the various data and address busses. The dependencies between the BRAM design parameters and the I/O signals are listed in Table 6.

Table 6: **Parameter-Port Dependencies**

Name	Affects	Depends	Relationship Description
C_OPB_DWIDTH	OPB_BE OPB_DBus Sln_DBus	0 to C_OPB_DWIDTH/8 -1 0 to C_OPB_DWIDTH -1 0 to C_OPB_DWIDTH -1	Number of Byte Enables Decoded Width of the OPB Data Bus Width of the Slave read Data Bus
C_OPB_AWDITH	OPB_ABUS	0 to C_OPB_AWIDTH -1	Width of the OPB Address Bus
I/O Signals			
OPB_ABus		C_OPB_AWIDTH	Width varies with the width of the OPB Address Bus
OPB_BE		C_OPBDWIDTH	Width varies with the width of the OPB Data Bus

OPB Timing

This section describes the basic read and write timing for the OPB. For detailed descriptions refer to the IBM OPB Specification(v2.0). An OPB cycle is initiated with a master request. The highest priority request is granted the bus, and in the next cycle the master asserts the bus select signal and begins the transfer. The transfer is completed with the return of transfer acknowledge, retry, or error acknowledge.

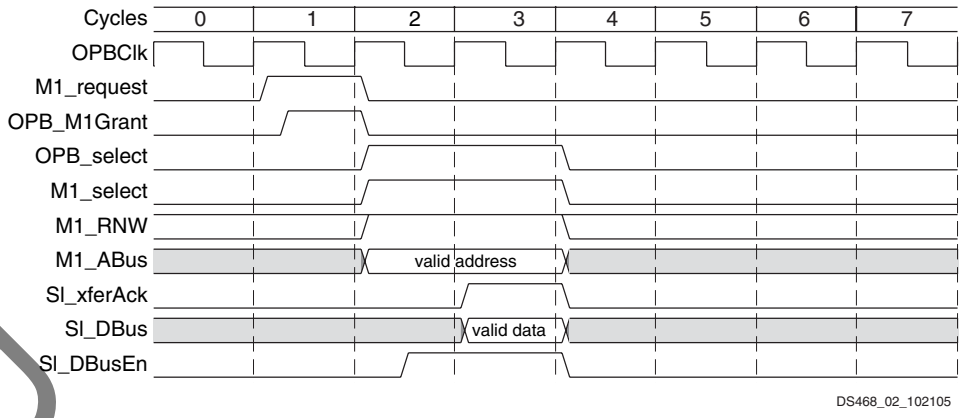

Figure 2: **Basic OPB Data Transfer**

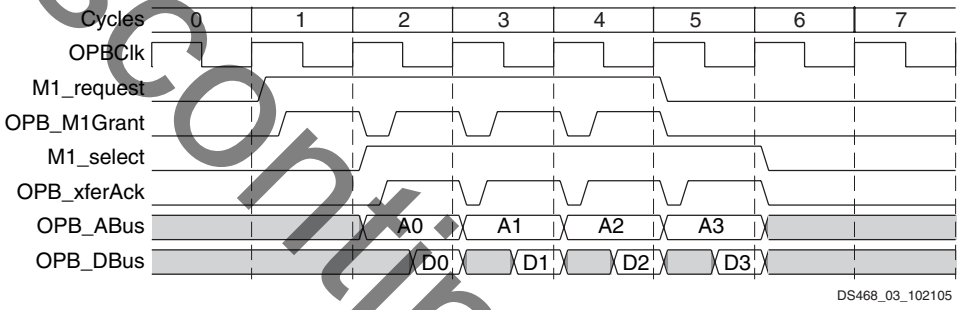

Figure 3: **OPB Data Transfer with Continuous Master Request**

Single byte, halfword, and word transactions are supported in the BRAM Interface Controller. A single word write followed by a single word read is shown in Figure 4.

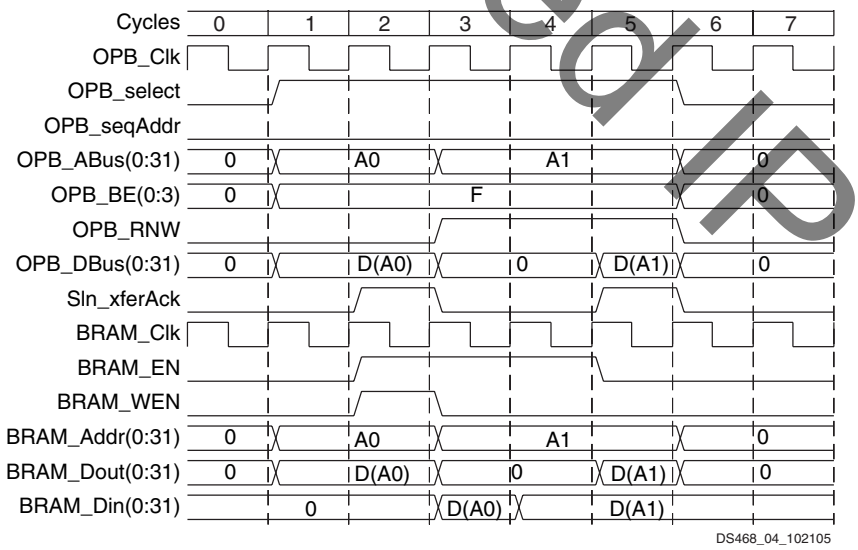

Figure 4: **Single Word Write/Read**

Burst write byte, halfword, and word transactions and burst read word transactions are also supported if the parameter C_INCLUDE_BURST_SUPPORT=1. The BRAM Interface Controller contains an internal read address counter that supplies the address to the BRAM a clock ahead of the address on the OPB so that read data can be supplied every clock during a read burst. This internal address counter counts 32-bit addresses, so only read bursts of words are supported. This is not a limitation however as the BRAM connected to the BRAM Interface Controller is always as wide as the OPB bus width. An 8-word burst write followed by an 8-word burst read is shown in Figure 5.

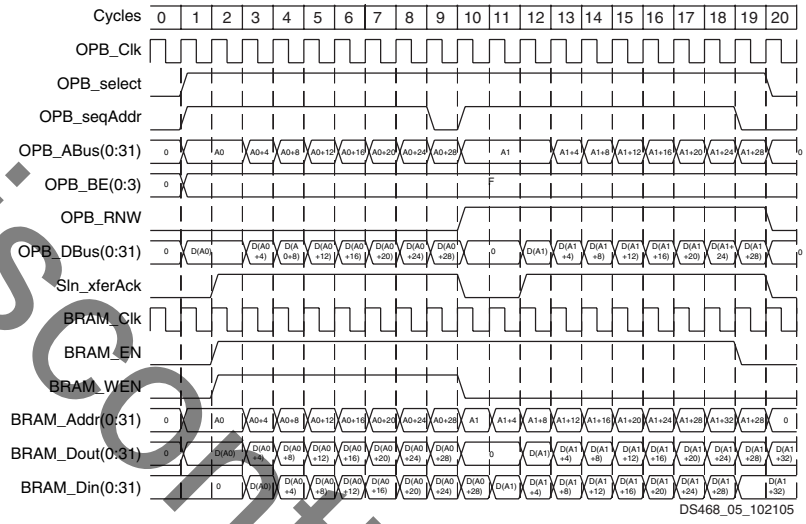

Figure 5: **8-Word Burst Write/Read**

The timing diagrams shown in Figure 4 and Figure 5 are specific to this version of the OPB BRAM Interface Controller and may vary slightly in other versions.

Data Types and Organization

The BRAMs are organized as big-endian data. The bit and byte labeling for the OPB big-endian data types is shown in Figure 6.

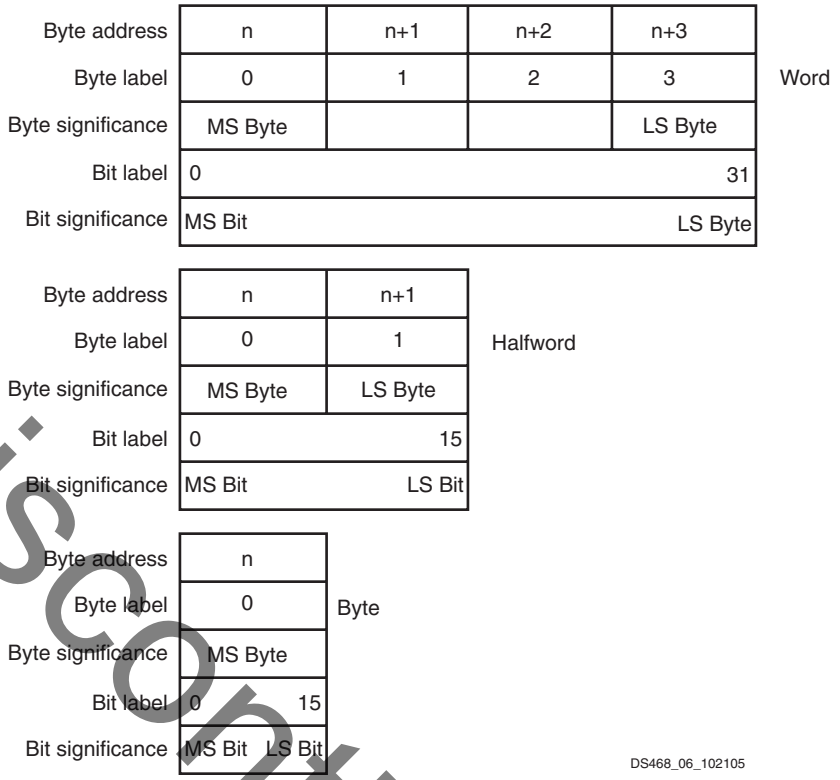

Figure 6: **OPB Big-Endian Data Types**

Design Implementation

Device Utilization and Performance Benchmarks

Because the OPB BRAM Interface Controller is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are estimates only. As the BRAM Interface Controller is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the BRAM Interface Controller design will vary from the results reported here.

The OPB BRAM Interface Controller benchmarks are shown in Table 7 for a Virtex-II Pro -7 FPGA.

Table 7: OPBBRAM Interface **FPGA Performance and Resource Utilization Benchmarks (Virtex-II Pro -7)**

Parameter Values	**Device Resources**			f_{MAX} (MHz)
C_INCLUDE_BURST_SUPPORT	Slices	Slice Flip-Flops	4-input LUTs	f_{MAX}
0	25	35	16	135
1	34	55	30	137

Notes:

1. These benchmark designs contain the OPB BRAM IF Controller with BRAM memory blocks present in the design, but without any additional logic.. Benchmark numbers approach the performance ceiling rather than representing performance under typical user conditions.

Target Technology

The intended target technology is a Virtex-II FPGA.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/10/02	1.0	Initial release.
11/11/02	1.2	Updated supported memory sizes table
05/29/03	1.3	Added burst support and resource utilization table. Updated timing diagrams.
07/15/03	1.4	Update to new template
07/29/03	1.4.1	Change DS number because of duplication
8/12/04	1.5	Updated for EDK Gmm; updated trademark and supported device family listing.
10/25/05	1.6	Converted to new DS template; updated figures to Xilinx graphic standards; updated trademark usage.
12/1/05	1.7	Added Spartan-3E to supported device listing.