Microprocessor Debug Module (MDM)

DS450 (v1.1) March 26, 2003

Product Overview

Introduction

This document provides the design specification for the Microblaze Debug Module (MDM). The MDM core enables JTAG-based debugging of one or more MicroBlaze processors.

Features

- Support for JTAG-based software debug tools
- Support for debugging a configurable number of MicroBlaze processors
- Support for synchronized control of multiple MicroBlaze processors - stop and single step
- Support for a JTAG-based UART with an OPB interface
- Based on BSCAN logic in Xilinx FPGAs
- Supports connection to Chipscope ICON core through unused BSCAN signals

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	TBD	
Version of Core	opb_mdm	v1.00.c
Resources Used		
	Min	Max
Slices	TBD	TBD
LUTs	TBD	TBD
FFs	TBD	TBD
Block RAMs	TBD	TBD
Provided with Core		
Documentation	Product Specification	
Design File Formats	TBD	
Constraints File	TBD	
Verification	TBD	
Instantiation Template	TBD	
Reference Designs	TBD	
Design Tool Requirements		
Xilinx Implementation Tools	TBD	
Verification	TBD	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

MDM Design Parameters

The features that can be parameterized in the Microprocessor Debug Module are shown in the following table:

Table 1: **OPB_MDM Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Number of MicroBlaze ports	C_MB_DBG_PORTS	0-8	1	integer
UART Interface	C_USE_UART	0,1	1	integer
UART data width	C_UART_WIDTH	8,16,32	32	integer

Number of MicroBlaze ports

Specifies the number of MicroBlaze debug ports that have been interfaced with the MDM. The default is 1 connection. For multiple connections, the debug signals for each processor have to be explicitly connected to the MDM.

UART Interface

Enables the UART interface on the OPB bus. This UART works over the JTAG port of Xilinx FPGAs and communicates with the Xilinx Microprocessor Debug tool.

UART data width

Specifies the width of the FIFOs on the UART. When the width is 8, this UART behaves in a manner similar to the OPB_UARTLITE or the OPB_JTAGUART cores.

OPB_MDM I/O Signals

The I/O signals for the OPB_MDM are listed in Table 2.

Table 2: **OPB_MDM I/O Signals**

Signal Name	Interface	I/O	Description
OPB_Clk	OPB	I	OPB clock for UART interface
OPB_Rst	OPB	I	OPB Reset for UART interface
Interrupt	Interrupt	O	Interrupt output from UART interface
Debug_SYS_Rst	Reset	O	Reset output to MicroBlaze and OPB bus
Debug_Rst	Reset	O	Reset output to MicroBlaze
Ext_BRK	Break	O	External Break signal to MicroBlaze
Ext_NM_BRK	Break	O	Non Maskable External Break signal
OPB_ABus[0:31]	OPB	I	OPB Address Bus
OPB_BE[4]	OPB	I	OPB Byte Enable
OPB_RNW	OPB	I	OPB Read Not Write
OPB_select	OPB	I	OPB Select
OPB_seqAddr	OPB	I	OPB Sequential Address
OPB_DBus[0:31]	OPB	I	OPB Data Bus
MDM_DBus	OPB	O	MDM Data Bus
MDM_errAck	OPB	O	MDM Error Ack
MDM_retry	OPB	O	MDM Retry
MDM_toutSup	OPB	O	MDM Timeout Suppress

Table 2: **OPB_MDM I/O Signals *(Continued)***

Signal Name	Interface	I/O	Description
MDM_xferAck	OPB	O	MDM Transfer Acknowledge
Dbg_Clk_0	Debug	O	MDM-MicroBlaze debug clock
Dbg_TDI_0	Debug	O	MDM-MicroBlaze debug TDI
Dbg_TDO_0	Debug	INT	MicroBlaze-MDM debug TDO
Dbg_Reg_En_0	Debug	O	MDM-MicroBlaze debug register enable
Dbg_Capture_0	Debug	0	MDM-MicroBlaze debug Capture
Dbg_Update_0	Debug	O	MDM-MicroBlaze debug Update
bscan_tdi	ICON	O	Connection to Chipscope ICON core
bscan_reset	ICON	O	Connection to Chipscope ICON core
bscan_shift	ICON	O	Connection to Chipscope ICON core
bscan_update	ICON	O	Connection to Chipscope ICON core
bscan_capture	ICON	O	Connection to Chipscope ICON core
bscan_sel1	ICON	O	Connection to Chipscope ICON core
bscan_drck1	ICON	O	Connection to Chipscope ICON core
bscan_tdo1	ICON	in	Connection to Chipscope ICON core

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
2/12/03	1.0	Initial Xilinx release.
3/26/03	1.1	Brought unused BSCAN signals out for Chipscope ICON usage.
12/19/03	1.2	Added LogiCORE Facts table. Reformatted to current Xilinx template.