

Introduction

The OPB System ACE Interface Controller is the interface between the OPB and the Microprocessor Interface (MPU) of the System ACE™ Compact Flash solution peripheral.

This module attaches to the OPB (On-chip Peripheral Bus).

Features

- OPB v2.0 bus interface with byte-enable support
- Used in conjunction with System ACE Compact Flash Solution to provide a System ACE memory solution
- System ACE Microprocessor Interface (MPU)
 - Read/Write from or to a Compact Flash device
 - Supports both 8-bit and 16-bit data bus access modes

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIe, Spartan-3, Spartan-3E, Virtex Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	opb_sysace	v1.00c
Resources Used		
	Min	Max
Slices		
LUTs		
FFs		
Block RAMs	--	--
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	6.3i or later	
Verification	ModelSim SE 5.8b or later	
Simulation	ModelSim SE 5.8b or later	
Synthesis	XST 6.3i	
Support		
Support provided by Xilinx, Inc.		

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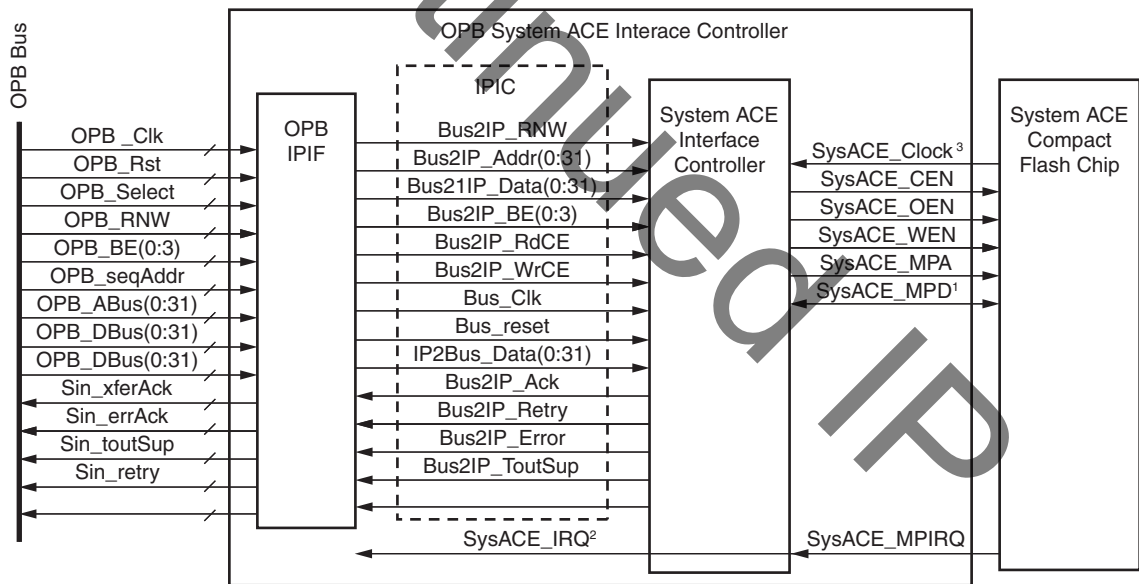
Functional Description

The Xilinx System ACE Compact Flash chip contains many registers that control the function of the chip, report the status of operations, and provide the interface to the data buffers for reading and writing sectors of the actual Compact Flash memory. The OPB System ACE Interface Controller provides the MPU interface of the Xilinx System ACE Compact Flash chip. The registers and data buffers of the Xilinx System ACE Compact Flash chip then become accessible via the OPB. See DS080, *System ACE Compact Flash Solution* for detailed information on the operation of the MPU interface, the MPU interface register definitions, and the MPU interface register address map.

The Xilinx System ACE supports an 8-bit and a 16-bit data bus access mode to these registers and data buffers. When set in 8-bit mode, the registers of the System ACE Compact Flash chip should be accessed via byte accesses only. When set in 16-bit mode, the registers of the System ACE Compact Flash chips should be accessed via half-word accesses only. The OPB System ACE Interface Controller core provides the parameter, C_MEM_WIDTH, to indicate the data bus access mode desired. Setting of this parameter will size the data bus to the Xilinx System ACE MPU correctly. The software drivers use this parameter to configure the Xilinx System ACE Bus Mode register (setting the Xilinx System ACE MPU data bus access width to the desired mode) and to access the registers with the proper type of transaction.

Figure 1 shows the overall block diagram of the OPB System ACE Interface Controller and its connections to/from the OPB and its connections to/from the Xilinx System ACE Compact Flash chip.

The OPB System ACE interface Controller is composed of the OPB IPIF and the System ACE Interface Controller. The OPB IPIF is configured in a simple OPB slave mode.



Notes:

1. SysACE_MPD is formed in the IOB from SysACE_MPD_I, SysACE_MPD_0, and SysACE_MPD_T.
2. SysACE_IRQ should be connected to an interrupt controller or to the interrupt input of the processor.
3. SysACE_Clk should be connected to a global clock buffer by the user.

DS475_01

Figure 1: OPB System ACE Interface Controller Block Diagram

System ACE Interface Controller

The System ACE interface controller contains a controller state machine and logic to synchronize signals across the OPB_Clk and SysACE_Clk domains as shown in [Figure 2](#).

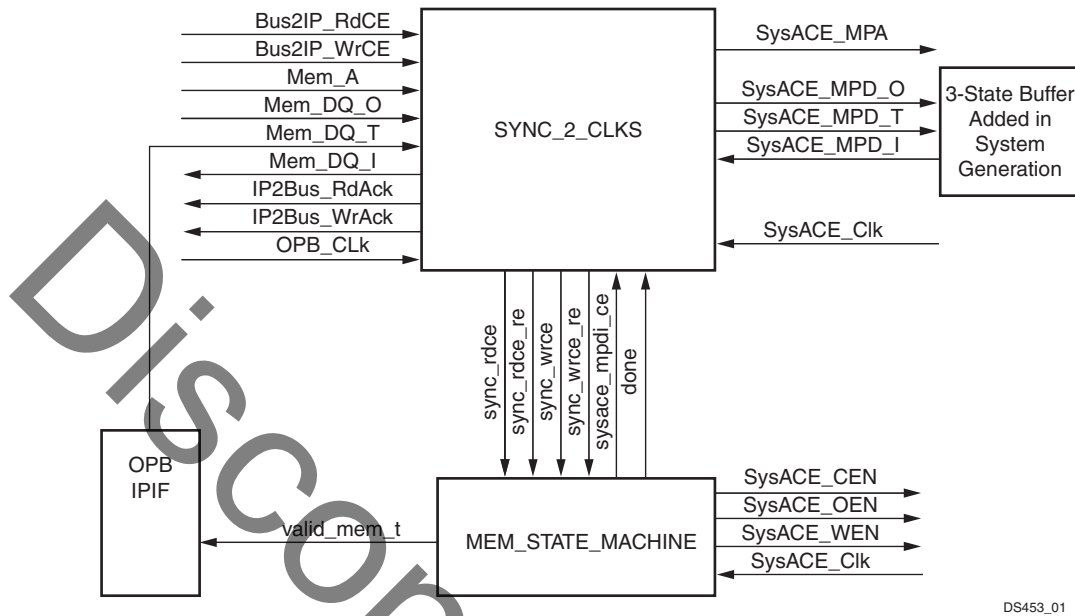


Figure 2: System ACE Interface Controller Diagram

The OPB System ACE Interface Controller core does not contain any internal registers or addressable memory space, therefore the mapping of OPB address bus is one-to-one with the System ACE address bus (SYSACE_MPA) as shown in [Table 1](#).

Table 1: OPB Address Bus to System ACE Address Bus Mapping (done in IP core)

OPB Address Bus	System ACE Address Bus
OPB_ABus(25 to 31)	SysACE_MPA(6 downto 0)

The Xilinx System ACE Compact Flash chip is a true little-endian device and the OPB is a big-endian bus. Therefore the OPB System ACE Interface Controller will do a bit-swap in each byte when connecting the OPB data bus to the System ACE data bus as shown in [Table 2](#).

Table 2: OPB Data Bus to System ACE Data Bus Mapping (done in IP core)

OPB Data Bus	System ACE Data Bus
OPB_DBus(8 to 15)	SysACE_MPD(15 downto 8)
OPB_DBus(0 to 7)	SysACE_MPD(7 downto 0)

Note however, that the OPB System ACE Interface Controller does not perform the byte swapping necessary to interface to a little-endian device when configured to use 16-bit mode. Therefore, the software drivers provided for this core will perform the necessary byte-swapping to correctly interface to the Xilinx System ACE Compact Flash chip as shown in [Table 3](#).

Table 3: OPB Big Endian to System ACE Little Endian Conversion (done in software driver)

Byte	OPB Data Bus	System ACE Data Bus
MSB	OPB_DBus(0 to 7)	SysACE_MPD(15 downto 8)
LSB	OPB_DBus(8 to 15)	SysACE_MPD(7 downto 0)

Clocking - Sync_2_Clks Module

The controller state machine runs off the SysACE_Clk. The IPIC signals indicating the start of a transaction are synchronized to the System ACE clock and used to start the state machine. All address, data, and control signals are output to the System ACE Compact Flash chip are synchronized to the SysACE_Clk and registered in the FPGA IO registers using SysACE_Clk to insure a clean interface between this chip and the FPGA. Data from the System ACE Compact Flash chip is also registered in FPGA IO registers using SysACE_Clk. It is then synchronized to the OPB_Clk for transmission on the bus. The frequency of the SysACE_Clk must be less than the frequency of the OPB_Clk.

Note that the address and data (if a write transaction) from the OPB will stay stable during the entire bus transaction and therefore would not have to be synchronized and output using the SysACE_Clk. This was done to provide a robust design, however, if the overall FPGA design is limited on resources, these synchronization registers could possibly be removed. The user is cautioned to analyze timing before removing these registers.

Also note that this core does not instantiate a global clock buffer for SysACE_Clk. This is left for the user to instantiate based on the resource requirements of their system.

System ACE Control state machine - Mem_state_machine Module

The state machine in the System ACE Interface controller performs the specified transaction to the MPU interface of System ACE Compact Flash chip and is shown in Figure 3. This state machine is clocked by SysACE_Clk and therefore outputs all System ACE control signals synchronous to this clock. The input control signals from the IPIF have been synchronized to the SysACE_Clk in the sync_2_clocks module.

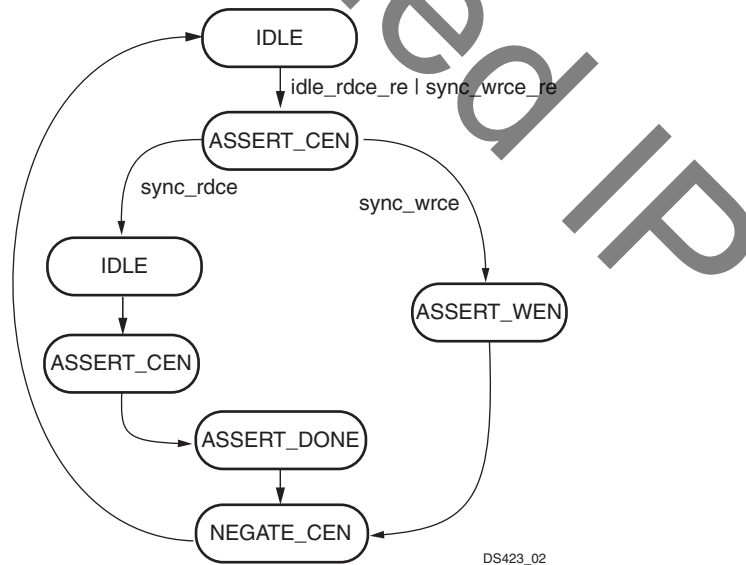


Figure 3: System ACE Interface Control State Machine

OPB System ACE Interface Controller I/O Signals

The I/O signals for the OPB System ACE Interface Controller are listed in [Table 4](#).

Table 4: OPB System ACE Interface Controller I/O Signals

Port	Signal Name	Interface	I/O	Description
OPB Slave Signals				
P1	OPB_Clk ⁽¹⁾	OPB	I	OPB Clock
P2	OPB_Rst	OPB	I	OPB Reset
P3	OPB_ABus(0:C_OPB_AWIDTH-1)	OPB	I	OPB Address Bus
P4	OPB_BE(0:C_OPB_DWIDTH/8-1)	OPB	I	OPB Byte Enables
P5	OPB_DBus(0:C_OPB_DWIDTH-1)	OPB	I	OPB Data Bus
P6	OPB_RNW	OPB	I	OPB Read, Not Write
P7	OPB_select	OPB	I	OPB Select
P8	OPB_seqAddr	OPB	I	OPB Sequential Address
P9	Sln_DBus(0:C_OPB_DWIDTH-1)	OPB	O	Memory Controller Data Bus
P10	Sln_errAck	OPB	O	Memory Controller Error Acknowledge
P11	Sln_retry	OPB	O	Memory Controller Retry
P12	Sln_toutSup	OPB	O	Memory Controller Timeout Suppress
P13	Sln_xferAck	OPB	O	Memory Controller Transfer Acknowledge
System ACE Signals				
P14	SysACE_Clk ^(1,2)	System Ace Core	I	System ACE Clock
P15	SysACE_MPIRQ	System Ace Core	I	System ACE Active high Interrupt Input
P16	SysACE_CEN	System Ace Core	O	System ACE Chip Enable
P17	SysACE_OEN	System Ace Core	O	System ACE Enable
P18	SysACE_WEN	System Ace Core	O	System ACE Write Enable
P19	SysACE_MPA(6:0)	System Ace Core	O	System ACE Address

Table 4: OPB System ACE Interface Controller I/O Signals (Contd)

Port	Signal Name	Interface	I/O	Description
P20	SysACE_MPD(C_MEM_WIDTH-1:0)	System Ace Core	I/O	System ACE Data Input/Output
P21	SysACE_IRQ ⁽³⁾	System Ace Core	O	System ACE Active High Interrupt Output

Notes:

1. OPB_Clk Frequency must be greater than or equal to SysACE_CLK Frequency
2. This design does not instantiate a global buffer on the SysACE_Clk. The user is advised to use a global buffer on this clock net.
3. This interrupt output is just a pass-through of the System ACE interrupt (SysACE_MPIRQ) and should be connected to an interrupt controller or directly to the processor's interrupt input.

OPB System ACE Interface Controller Parameters

To allow the designer to obtain an OPB System ACE Interface Controller that is uniquely tailored for designer's system, certain features can be parameterized in the OPB System ACE Interface Controller design. This allows the designer to configure a design that only utilizes the resources required by designer's system, and operates with the best possible performance. The features that can be parameterized in Xilinx OPB System ACE Interface Controller designs are shown in Table 5.

Table 5: OPB System ACE Interface Controller Parameters

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Address space					
G1	OPB System ACE Base Address	C_BASEADDR	Valid Address Range ⁽²⁾	None ⁽¹⁾	std_logic_vector
G2	OPB System ACE High Address	C_HIGHADDR	Valid Address Range ⁽²⁾	None ⁽¹⁾	std_logic_vector
System ACE MPU I/F					
G3	System ACE MPU Data Bus Access Mode ⁽³⁾	C_MEM_WIDTH	8,16	16	integer
	OPB Bus Interface				
G4	OPB Data Bus Width	C_OPB_DWIDTH	32	32	integer
G5	OPB Address Bus Width	C_OPB_AWIDTH	32	32	integer

Notes:

1. No default value is specified for C_BASEADDR and C_HIGHADDR to insure that the actual value is set; if the value is not set, a compiler error is generated. These generics must be a power of two.
2. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power of two range, such that range = 2ⁿ, and the n least significant bits of C_BASEADDR must be zero. The minimum range specified by these parameters must be at least 0x7F. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR + 1.
3. Please refer to Xilinx DS080, System ACE Compact Flash Solution, for more information.

Allowable Parameter Combinations

The address range of the OPB System ACE Interface Controller must be a power of 2. If the desired address range is represented by 2^n , then the n least significant bits of the base address must be 0. The minimum range specified by C_BASEADDR and C_HIGHADDR must be at least 0x7F to cover the addressable registers and data buffer available in the Xilinx System Ace Compact Flash chip.

Parameter-Port Dependencies

The width of many of the OPB System ACE Interface Controller signals depends on the width of the various data and address buses in the system. The dependencies between the OPB System ACE Interface Controller design parameters and I/O signals are shown in [Table 6](#).

Table 6: Parameter-Port Dependencies

Name	Affects	Depends	Relationship Description
C_OPB_DWIDTH	OPB_BE OPB_DBus SIn_DBus		Number of Byte Enables Decoded Width of the OPB Data Bus Width of the Slave read Data Bus
C_OPB_AWIDTH	OPB_ABUS		Width of the OPB Address Bus
C_MEM_WIDTH	SysACE_MPD_I SysACE_MPD_O SysACE_MPD_T		Width of the System ACE Data Bus
I/O Signals			
OPB_ABus		C_OPB_AWIDTH	Width varies with the width of the OPB Address Bus
OPB_BE		C_OPB_DWIDTH	Width varies with the width of the OPB Data Bus
SysACE_MPD_I SysACE_MPD_O SysACE_MPD_T		C_MEM_WIDTH	Width varies with the width of the System ACE Data Bus

OPB System ACE Timing Diagrams

This section contains timing diagrams showing the register read and write accesses to the Xilinx System ACE controller. Note that the System ACE clock is not driven from this core, it is an input to this core. Also note the byte swapping that occurs during the register accesses.

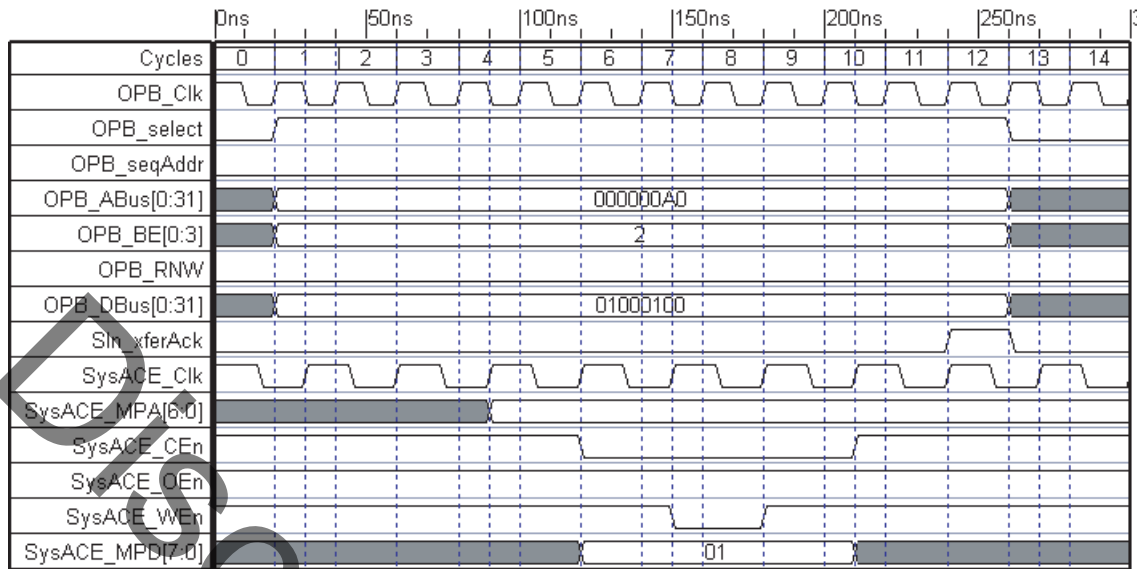


Figure 4: OPB System ACE 8-bit Register Write

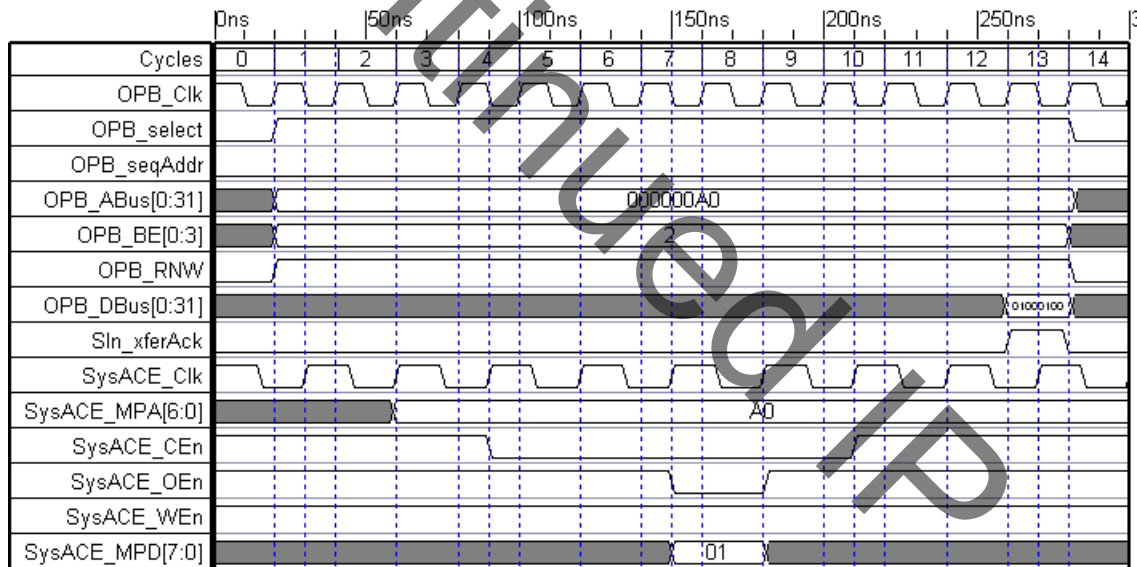


Figure 5: OPB System ACE 8-bit Register Read

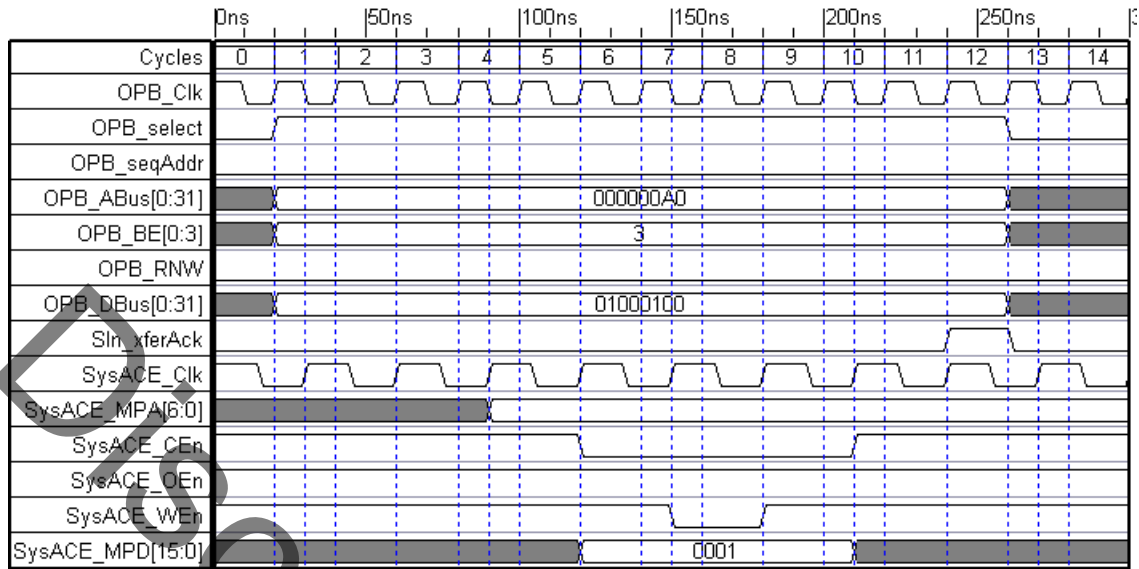


Figure 6: OPB System ACE 16-bit Register Write

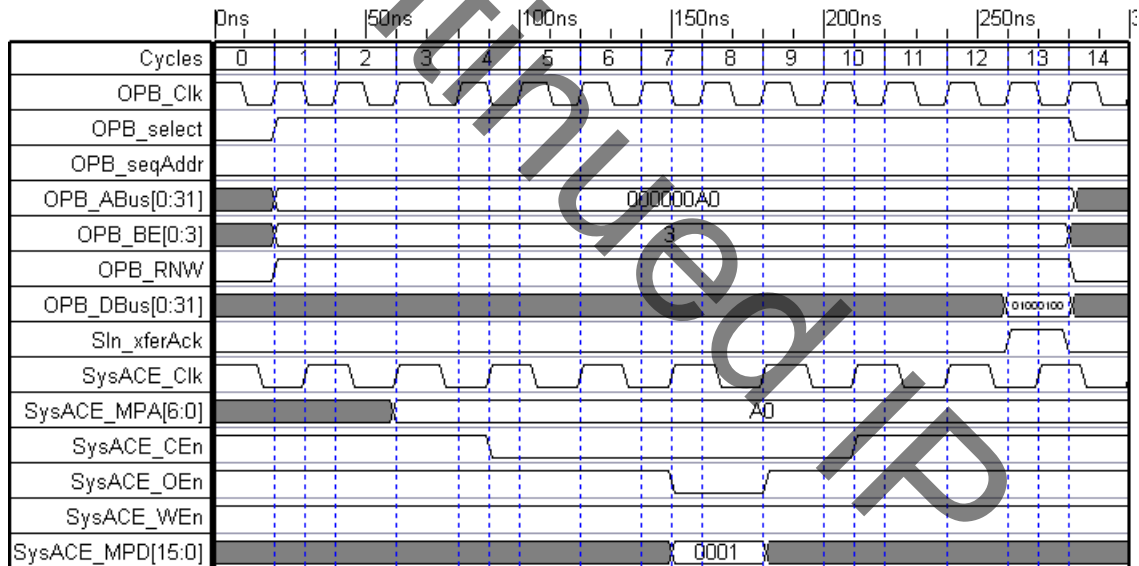


Figure 7: OPB System ACE 16-bit Register Read

Design Constraints

Timing Constraints

A timing constraint should be placed on the clock, setting the frequency to meet the bus timing requirements. For example:

```
NET "OPB_Clk" TNM_NET = "OPB_Clk";
```

```
TIMESPEC "TS_OPB_clk" = PERIOD "OPB_Clk" 9 ns HIGH 50 %;
```

Design Implementation

Target Technology

The intended target technology is a Virtex-II PRO FPGA.

Device Utilization and Performance Benchmarks

Because the System Ace Controller is a module that will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are just estimates. As the OPB System Ace Interface Controller is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing will vary from the results reported here.

The OPB System Ace Interface Controller benchmarks are shown in [Table 7](#) for a Virtex-II Pro -6 FPGA.

Table 7: System Ace Interface Controller FPGA Performance and Resource Utilization Benchmarks (Virtex-II Pro xc2vp20-7-ff896)

Parameter Values			Device Resources			f _{MAX}
C_MEM_WIDTH	C_OPB_DWIDTH	C_OPB_AWIDTH	Slices	Slice Flip-Flops	4- input LUTs	(MHz)
8	32	32	103	155	81	190
16	32	32	112	186	80	205

Notes:

1. These benchmark designs contain only the System Ace interface controller with registered inputs/outputs without any additional logic. Benchmark numbers approach the performance ceiling rather than representing performance under typical user conditions.

Reference Documents

The following documents contain reference information important to understanding the OPB SysACE Controller design:

- *IBM 64-Bit On-Chip Peripheral Bus, Architecture Specifications, v2.0*
- *IBM OPB Bus Functional Model Toolkit, User's Manual, v3.1*
- *On-Chip Peripheral Bus IP VHDL Test Harness, IPSPEC045*
- *System Ace: Configuration Solution for Xilinx FPGAs*
- *DS080 System ACE Compact Flash Solution*

Revision History

Date	Version	Revision
09/10/02	1.0	Initial release.
10/21/02	1.1	Added Device Utilization Table and Values
11/08/02	1.2	Added Interrupt I/O Signals
11/11/02	1.3	Added Device Utilization numbers with new I/O
01/07/03	1.4	Update for EDK SP3
07/22/03	1.5	Remove SGP Section per CR 171674; update to new template
09/24/03	1.5.1	Update trademarks
09/24/03	2.0	Release version b
02/09/04	2.1	Added timing diagrams
8/12/04	2.2	Updated for Gmm; updated trademarks and supported device family listing.
9/8/04	2.2.1	Incorporate CR193674: in tables 2 and 7, C_MEM_WIDTH was C_MEM_DWIDTH.
11/02/04	2.3	Updated for opb_ipif_v3_01_a
5/11/05	2.3.1	Updated to incorporate CR206050; updated trademark usage/placement; added Spartan-3E to supported device listing in hidden conditional text.
9/28/05	2.4	Converted to new DS template; updated figures to Xilinx graphic standards; performed overall review; made minor edits.
12/2/05	2.5	Added Spartan-3E to supported device families listing.