IP Facts

***Note*:** Up until Vivado 2019.2, the Radio over Ethernet (RoE) Framer IP included an O-RAN mode. In Vivado 2020.1, O-RAN mode became a separate O-RAN Radio Interface IP, which is documented here. For information about the RoE Framer core, refer to the *Radio over Ethernet Framer LogiCORE IP Product Brief* (PB056).

The Xilinx® O-RAN Radio Interface (O-RAN Radio IF) core is part of a system solution developed on the Versal™ ACAP, Zynq® UltraScale+™ MPSoC, and Zynq UltraScale+ RFSoC, relying on both hardware and software to provide a comprehensive and efficient computing platform required to implement an O-RAN radio unit. The core supports the use of the following protocols: eCPRI, IEEE 1914.3 (NGFI), IEEE 1588, Synchronous Ethernet, and Node and Network OAM. The core enables radio data transmission through a packet-based transport network connecting Remote Radio Units (RRUs) to the centralized Baseband Unit (BBU).

Additional Documentation

A product guide is available for this core. Access to this material can be requested by clicking on this registration link: https://www.xilinx.com/member/oran-radio-if.html.

Features

- Provides O-RU (O-RAN radio unit) function only.
- Supports eCPRI and 1914.3 over standard IEEE 802.1 Ethernet packets, optionally including VLAN tags, as well as UDP over IPv4 or IPv6, over Ethernet.
- Fully programmable filtering rules allow the hardware to identify and manage user plane packets.
- Each Ethernet and IP/UDP header field is fully programmable.
- Alignment to an external 10 ms Start of Radio Frame pulse, enabling 1588 synchronization.
- The core implements *O-RAN Control, User and Synchronization Plane Specification v4.0* (O-RAN Specification v4.0). The core supports up to four 10 Gb/s or four 25 Gb/s Ethernet ports. Mixed rate mode is not supported.
  - Currently supports eight component carriers (CCs), with independent uplink and downlink timers.
  - Supports a resolution of down to one resource block (RB) per section message.
  - U-Plane support for up to 16 spatial streams, one additional separate stream for SSB traffic (PSS, SSS, PBCH), PRACH and four shared unsolicited data streams (for use in SRS).

- One PRACH uplink data port.
- The core implements the radio fronthaul interface, managing both the control and user planes, implementing the appropriate timing advances and compensating for the delay variations of packets coming from different BBUs. User radio blocks with related beam IDs are extracted from received packets at the appropriate symbol period and forwarded through AXI4-Stream outputs to external double buffers interfacing the beamforming function.

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Kintex® UltraScale™, Virtex® UltraScale™, Zynq®-7000 SoC, Kintex® UltraScale+™, Virtex® UltraScale+™, Zynq® UltraScale+™ MPSoC, Zynq® UltraScale+™ RFSoC, Versal™ ACAP.
Supported User Interfaces	AXI4-Stream
Resources	Performance and Resource Use web page (registration required)
Provided with Core	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	Verilog
Supported S/W Driver	Linux user space driver (Libmetal)
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 73648
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

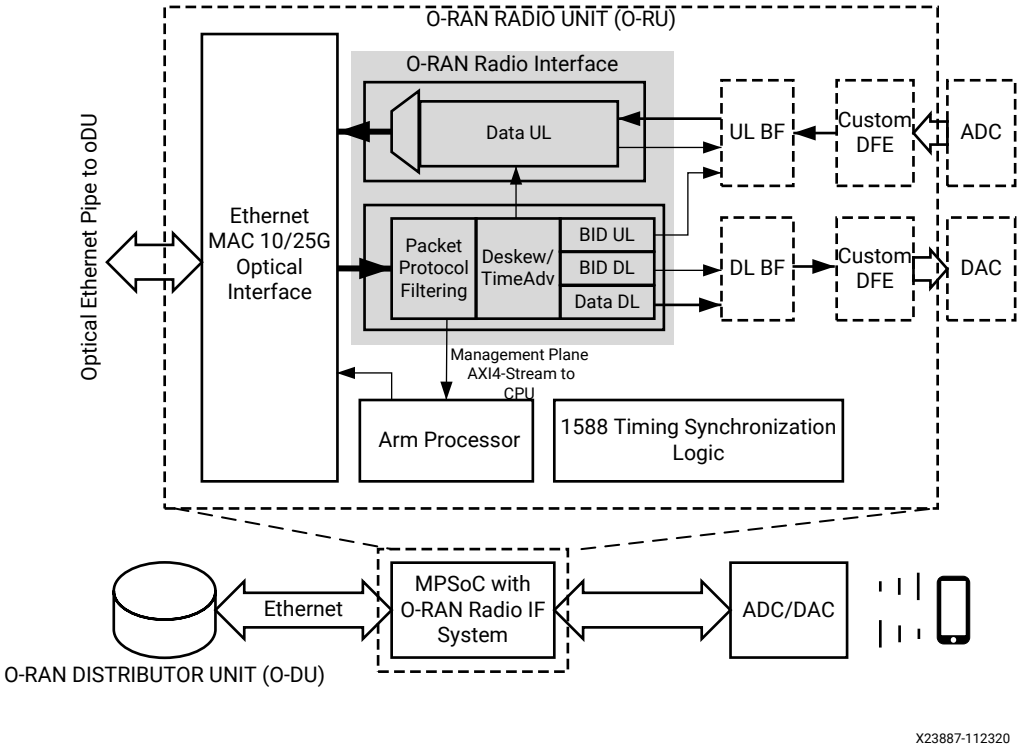
1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The O-RAN Radio Interface allows the development of a complete solution to support all the features required by an advanced fronthaul interface. In the LTE and 5G radio mobile architectures, fronthaul is the transport network interconnecting the Remote Radio Units (RRUs) to the Baseband Units (BBUs) and relies on different topologies, such as point-to-point, point-to-multipoint, and ring. To match modern network requirements in efficiency and flexibility, the fronthaul network is packet-based, relying either directly on the Ethernet network protocol or on a UDP/IP stack.

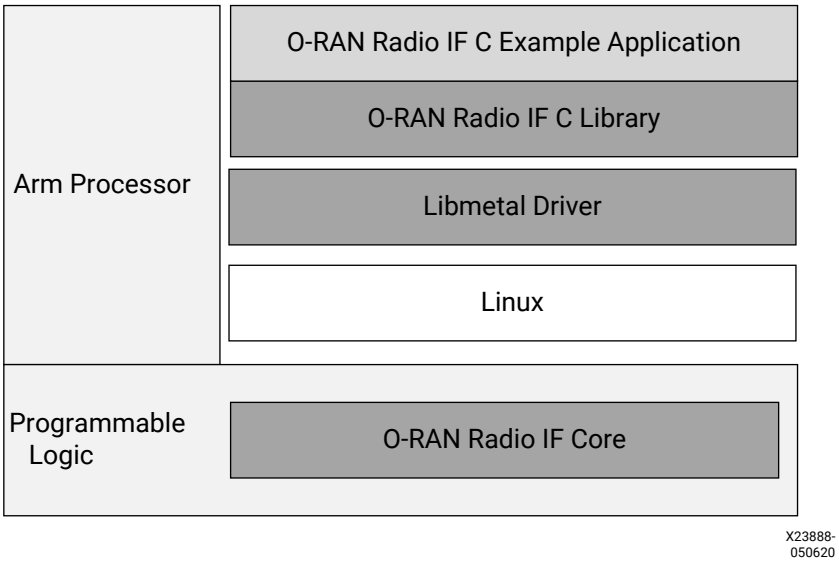
The O-RAN Radio IF system, shown in the following figure, built from the O-RAN Radio Interface and other Xilinx® IP, is a computing platform designed to support the management of the user, control, and synchronization planes, working as an intelligent and adaptable network interface submodule within an implementation of a 5G RRU.

Figure 1: **Top Level Overview**



The O-RAN Radio IF supplies IP, drivers, and software APIs to implement supported protocols. The O-RAN Radio IF IP is implemented in the programmable logic (PL), and the drivers and software APIs run on Linux on the Arm® processor. In the following figure, the O-RAN Radio IF C library, the libmetal driver, and the O-RAN Radio IF IP core comprise the solution and are required for full protocol support; the O-RAN Radio IF C example application provides code to demonstrate the solution.

Figure 2: **O-RAN Radio IF IP Solution**



The C-Plane and U-Plane are handled in hardware. The subsystem configuration and other user services can be handled by a software API library running on the embedded processor in conjunction with dedicated hardware features, such as packet timestamping at the PCS/PMA level. Because no more circuit-based interconnections are available, it is also necessary to synchronize each node through the packet network; the synchronization plane therefore relies on a PTP protocol such as *IEEE 1588 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems* (IEEE 1588), and on Synchronous Ethernet.

The O-RAN Radio IF system provides a platform to run the Linux PTP Precision Time Protocol (ptp4l) for IEEE 1588 hardware timestamping for Linux and control the hardware-based timer. The O-RAN Radio IF core can realign its internal timers to the Start of Radio Frame information transported by the synchronization plane. Control plane management relies on protocols such as SNMP and ICMP, running on an IP stack and implemented in software on the embedded processor.

The O-RAN Radio IF system deals with two different packet flows:

- A time-sensitive and high-priority flow of user plane data traffic handled by dedicated and adaptable O-RAN Radio IF hardware
- A lower-priority traffic flow, constituted by different streams and protocols, all of which can be managed by the Zynq® UltraScale+™ MPSoC processor

The O-RAN Radio IF can filter each incoming downlink packet in real time, recognize messages carrying antenna-carrier data, and forward them to the managing hardware, while redirecting all remaining traffic to the embedded processor through a DMA interface. In the uplink direction, the subsystem must arbitrate access to the supported Ethernet ports between the higher priority stream generated by the O-RAN Radio IF core and that coming from the embedded processor.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement.The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Evaluation licenses and hardware timeout licenses are available for this core. Contact your local Xilinx sales representative for information about pricing and availability.

Note: To verify that you need a license, check the License column of the IP Catalog. Included means that a license is included with the Vivado® Design Suite; Purchase means that you have to purchase a license to use the core.

For more information about this core, visit the O-RAN lounge webpage.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/23/2020 Version 1.1	
General Updates	Updated in line with Product Guide.
06/03/2020 Version 1.0	
Initial release.	N/A

Please Read: Important Legal Notices

Copyright