

Table 1: DDR SDRAM Controller Design Parameters (Continued)

| Grouping / Number | Feature / Description | Parameter Name | Allowable Values | Default Value | VHDL Type |
|---|--|---|-------------------------|--------------------------------------|------------------|
| G12 | Delay after ACTIVE command for a row before an ACTIVE command for another row (ps) | C_DDR_TRRD | | 15000 | integer |
| G13 | Delay after a PRECHARGE command (ps) | C_DDR_TRP | | 20000 | integer |
| G14 | Average periodic refresh command interval (ps) | C_DDR_TREFI | | 7800000 | integer |
| G15 | Refresh command interval (ps) | C_DDR_TREFC | | 70300 | |
| G16 | CAS latency | C_DDR_CAS_LAT | 2,3 | 2 | integer |
| G17 | Total data width of DDR devices (bits) | C_DDR_DWIDTH | 32 | | integer |
| G18 | DDR address width | C_DDR_AWIDTH | See note ⁽³⁾ | 13 | integer |
| G19 | DDR column address width | C_DDR_COL_AWIDTH | See note ⁽³⁾ | 9 | integer |
| G20 | DDR bank address width | C_DDR_BANK_AWIDTH | See note ⁽³⁾ | 2 | integer |
| Address Space | G21 | Base Address | C_BASEADDR | Valid address ⁽⁴⁾ | std_logic_vector |
| | G22 | High Address | C_HIGHADDR | Valid address ⁽⁴⁾ | std_logic_vector |
| PLB Bus Interface | G23 | PLB Data bus width | C_PLB_DWIDTH | 64 | integer |
| | G24 | PLB Address bus width | C_PLB_AWIDTH | 32 | integer |
| | G25 | Number of PLB bus masters | C_PLB_NUM_MASTERS | 1 - 16 | integer |
| | G26 | PLB clock period (ps) | C_PLB_CLK_PERIOD_PS | | integer |
| Simulation Only | G27 | DDR Initialization time for simulation ⁽⁶⁾ | C_SIM_INIT_TIME_PS | Minimum 200 clock periods 2000000 | integer |
| Auto-calculated parameters ⁽⁵⁾ | G28 | Number of bits required to encode the number of PLB Masters | C_PLB_MID_WIDTH | 1 - log ₂ (C_NUM_MASTERS) | integer |

Notes:

1. The DDR DQS signals should either internal or external pull resistors. Set this parameter to indicate if these resistors are pull up resistors or pull down resistors.
2. Data width of DDR devices must be half of the PLB data width.
3. $C_DDR_AWIDTH + C_DDR_COL_AWIDTH + C_DDR_BANK_AWIDTH + \log_2(C_DDR_DWIDTH/8)$ must be $< C_PLB_AWIDTH-1$.
4. The range specified by C_BASEADDR and C_HIGHADDR must comprise a complete, contiguous power of two range such that range = 2^n , and the n least significant bits of C_BASEADDR must be zero.
5. These parameters are automatically calculated by the system generation tool and are not input by the user.
6. This parameter adjusts the initialization time of the DDR for simulation only. Must be > 200 clocks

