PLB Master BFM

DS131 (v2.0) April 30, 2004 **Product Overview**

Introduction

The CoreConnect Toolkit PLB Master Bus Functional Model is a simulation hardware component that has a PLB bus interface and may act as a bus master.

The component contains logic to automatically initiate bus transactions on the PLB bus.

The model maintains an internal memory which can be initialized through the bus functional language and may be dynamically checked during simulation, or when all bus transactions have completed.

Features

- Xilinx PLB bus interface
- Initiates bus transactions
- In Command Mode, the behavior is defined in a Bus Functional Language (BFL) file
- In Auto Mode, the model generates random bus transactions
- The model may be dynamically checked during simulation or when all bus transactions have completed

More Information

For detailed information on the IBM PLB Bus Functional Model Toolkit, you may register for the **CoreConnect Lounge** on the Xilinx web site to get access to the IBM CoreConnect documentation.

Core Facts

Core Specifics		
Supported Device Family	All	
Version of Core	plb_master _bfm	v1.00.a
Resources Used		
	Min	Max
I/O	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	This document	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	EDK 6.2 or later ISE 6.2 or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	N/A	
Support		
Support provided by Xilinx, Inc.		

Implementation

The PLB is a full-featured bus architecture with many features that increase bus performance. To obtain an efficient use of FPGA resource, Xilinx uses a subset of the PLB for Xilinx-developed PLB devices.

The CoreConnect PLB master model has an interface to a full-featured PLB bus. Xilinx has created an interface to the Core-Connect Toolkit components for them to be used within the Xilinx implementation of the PLB bus.

The CoreConnect PLB CoreConnect Toolkit contains standard Bus Functional Models and a Bus Functional Compiler for a rich Bus Functional Language specification. Xilinx utilizes these to provide the functionality and encapsulates the models around a customized interface that performs the translation between the two bus implementations domains. Figure 1 shows how this is done for the PLB master model.

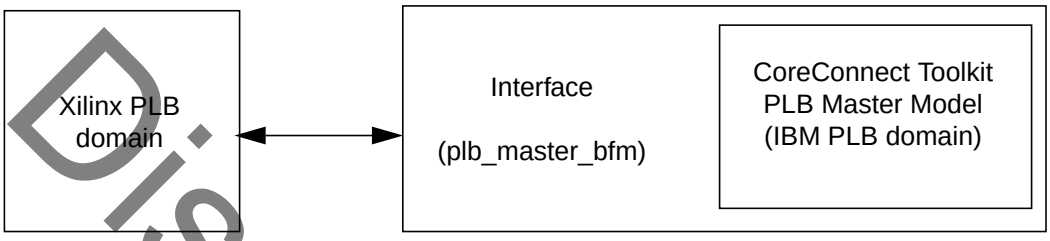

Figure 1: **Xilinx to IBM PLB domain interface**

MPD Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral s parameters that are fixed at FPGA configuration time. The parameters are described in Table 1.

Table 1: **MPD Parameters**

Parameter	Description	Allowable Values	Type
PLB_MASTER_NUM	ID number	0b0000 - 0b1111	std_logic_vector
PLB_MASTER_ADDR_LO_0	PLB Master base address 0(1)	Valid PLB Address	std_logic_vector
PLB_MASTER_ADDR_HI_0	PLB Master high address 0(1)	Valid PLB Address	std_logic_vector
PLB_MASTER_ADDR_LO_1	PLB Master base address 1(1)	Valid PLB Address	std_logic_vector
PLB_MASTER_ADDR_HI_1	PLB Master high address 1(1)	Valid PLB Address	std_logic_vector

Notes:

1. Master address ranges are only used when the device is configured to automatically generate bus transactions by setting master_auto_mode to true in the BFL file. When the master model is configured for automatic mode, there is no need to initialize read/write commands since they are ignored.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
4/30/04	1.0	Initial Xilinx release