





**Table 1: SDRAM Controller Design Parameters (Continued)**

Grouping / Number	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G4	Target FPGA family	C_FAMILY	spartan2 spartan2e virtex virtexe virtex2 virtex2p	virtex2p	string
SDRAM Device Features	G5	Load Mode Register command cycle time (Tck)	C_SDRAM_TMRD	2	integer
	G6	Write Recovery Time(1) (ps)	C_SDRAM_TWR	15000	integer
	G7	Read/Write Command to Read/Write command (Tck)	C_SDRAM_TCCD	1	integer
	G8	Delay after ACTIVE command before PRECHARGE command (ps)	C_SDRAM_TRAS	40000	integer
	G9	Delay after ACTIVE command before another ACTIVE or AUTOREFRESH command (ps)	C_SDRAM_TRC	65000	integer
	G10	Delay after AUTOREFRESH before another command(ps)	C_SDRAM_TREFC	75000	integer
	G11	Delay after ACTIVE command before READ/WRITE command(ps)	C_SDRAM_TRCD	20000	integer
	G12	Delay after ACTIVE command for a row before an ACTIVE command for another row (ps)	C_SDRAM_TRRD	15000	integer
	G13	Delay after a PRECHARGE command (ps)	C_SDRAM_TRP	20000	integer
	G14	Refresh command interval (ms)	C_SDRAM_TREF	64	integer
	G15	Number of Rows in a Refresh Period <sup>(3)</sup>	C_SDRAM_REFRESH_NUMROWS	2048, 4096, 8192, 16384	integer
	G16	CAS Latency	C_SDRAM_CAS_LAT	2,3	integer
	G17	Total data width of devices <sup>(4)</sup>	C_SDRAM_DWIDTH	8, 16, 32, 64	integer





































