PLB 16450 UART (v1.00c)

DS432 (v2.3) July 9, 2003 **Product Overview**

Introduction

This document provides the specification for the PLB Universal Asynchronous Receiver/Transmitter (UART) Intellectual Property (IP).

The UART described in this document has been designed incorporating the features described in *National Semiconductor PC16550D UART with FIFOs* data sheet (June, 1995), (http://www.national.com/pf/PC/PC16550D.html).

The National Semiconductor PC16550D data sheet is referenced throughout this document and should be used as the authoritative specification. Differences between the National Semiconductor implementation and the OPB UART Point Design implementation are highlighted and explained in Specification Exceptions.

Features

- Hardware and software register compatible with all standard 16450 UARTs
- Implements all standard serial interface protocols
  - 5, 6, 7, or 8 bits per character
  - Odd, Even, or no parity detection and generation
  - 1, 1.5, or 2 stop bit detection and generation
  - Internal baud rate generator and separate receiver clock input
  - Modem control functions
  - False start bit detection and recovery
  - Prioritized transmit, receive, line status, and modem control interrupts
  - Line break detection and generation
  - Internal loop back diagnostic functionality
- Registers
  - Receiver Buffer Register (Read Only)
  - Transmitter Holding Register (Write Only)
  - Interrupt Enable Register
  - Interrupt Identification Register (Read Only)
  - Line Control and Line Status Registers
  - Modem Control and Modem Status Registers
  - Scratch Register
  - Divisor Latch (least and more significant byte)
- System clock frequency of 100 MHz

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex™-II	
Version of Core	plb_uart16450	v1.00c
Resources Used		
	Min	Max
Slices	432	432
LUTs	487	487
FFs	410	410
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

UART Background

The PLB 16450 performs parallel to serial conversion on characters received from the CPU and serial to parallel conversion on characters received from a modem or microprocessor peripheral. The PLB 16450 is capable of transmitting and receiving 8, 7, 6, or 5 bit characters, with 2, 1.5 or 1 stop bits and odd, even or no parity.

The PLB 16450 can transmit and receive independently. The device can be configured and it's status monitored via the internal register set. The PLB 16450 is capable of signaling receiver, transmitter and modem control interrupts. These interrupts can be masked, are prioritized and can be identified by reading an internal register.

16450 UART Design Parameters

To allow you to obtain an PLB UART that is uniquely tailored for your system, certain features can be parameterized in the PLB UART design. This allows you to have a design that only utilizes the resources required by your system and runs at the best possible performance. The features that can be parameterized in the Xilinx PLB UART design are shown in Table 1.

Table 1: **Design Parameters**

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
PLB Interface	G1	PLB UART Base Address	C_BASEADDR	Valid Word Aligned Address	A0000000	std_logic_vector
	G2	PLB Data Bus Width	C_PLB_DWIDTH	64	64	integer
	G3	PLB Address Bus Width	C_PLB_AWIDTH	16 - 32	32	integer
	G4	Device Block ID	C_DEV_BLK_ID	0-255	0	integer
	G5	Module Identification Register (1)	C_DEV_MIR_ENABLE	0,1.	0	integer
	G6	PLB UART High Address	C_HIGHADDR	C_HIGHADDR -C_BASEADDR must be a power of 2 >= to C_BASEADDR+1FFFF	A0001FFF	std_logic_vector
	G7	Number of PLB Masters	C_PLB_NUM_MASTERS	1-16	8	integer
	G8	Width of Master ID Bus	C_PLB_MID_WIDTH	log2(C_PLB_NUM_MASTERS)	3	integer
	G9	FPGA Architecture Type	C_FAMILY	spartan2, spartan2e, virtex, virtexe, virtex2, virtex2p	virtex2p	string
UART Features	G10	External XIN	C_HAS_EXTERNAL_XIN	0,1	0	integer
	G11	External RCLK	C_HAS_EXTERNAL_RCLK	0,1	0	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

UART I/O Signals

The I/O signals for the UART are listed in Table 2. The interfaces referenced in this table are shown in Figure 1 in the UART block diagram.

Table 2: **UART I/O Signals**

Grouping		Signal Name	Interface	I/O	Description
PLB Slave Signals	P1	PLB_abort	PLB	I	PLB abort bus request indicator
	P2	PLB_ABus(0:C_PLB_AWIDTH-1)	PLB	I	PLB address bus
	P3	PLB_BE(0:(C_PLD_DWIDTH / 8) -1)	PLB	I	PLB byte enables
	P4	PLB_busLock	PLB	I	PLB bus lock
	P5	PLB_compress	PLB	I	PLB compressed data transfer indicator
	P6	PLB_guarded	PLB	I	PLB guarded transfer indicator
	P7	PLB_lockErr	PLB	I	PLB lock error indicator
	P8	PLB_masterID(0:C_PLB_MID_WIDTH-1)	PLB	I	PLB current master indicator
	P9	PLB_ordered	PLB	I	PLB synchronize transfer indicator
	P10	PLB_PAValid	PLB	I	PLB primary address valid indicator
	P11	PLB_rdBurst	PLB	I	PLB burst read transfer indicator
	P12	PLB_rdPrim	PLB	I	PLB secondary to primary read request indicator
	P13	PLB_RNW	PLB	I	PLB read not write
	P14	PLB_SAValid	PLB	I	PLB secondary address valid indicator
	P15	PLB_size(0:3)	PLB	I	PLB transfer size
	P16	PLB_type(0:2)	PLB	I	PLB transfer type
	P17	PLB_wrBurst	PLB	I	PLB burst write transfer indicator
	P18	PLB_wrDBus(0:C_PLB_DWIDTH -1)	PLB	I	PLB write data bus
	P19	PLB_wrPrim	PLB	I	PLB secondary to primary write request indicator
	P20	PLB_MSize(0:1)	PLB	I	PLB master data bus size
	P21	PLB_pendReq	PLB	I	PLB pending bus request indicator
	P22	PLB_pendPri(0:1)	PLB	I	PLB pending request priority
	P23	PLB_reqPri(0:1)	PLB	I	PLB current request priority
	P24	Sl_addrAck	PLB	O	Slave address acknowledge
	P25	Sl_MBusy(0:C_NUM_MASTERS-1)	PLB	O	Slave busy indicator
	P26	Sl_MErr(0:C_NUM_MASTERS-1)	PLB	O	Slave error indicator

Table 2: **UART I/O Signals *(Continued)***

Grouping		Signal Name	Interface	I/O	Description
	P27	Sl_rdBTerm	PLB	O	Slave terminate read burst transfer
	P28	Sl_rdComp	PLB	O	Slave read transfer complete indicator
	P29	Sl_rdDAck	PLB	O	Slave read data acknowledge
	P30	Sl_rdDBus(0:C_PLB_DWIDTH -1)	PLB	O	Slave read bus
	P31	Sl_rdWdAddr(0:3)	PLB	O	Slave read word address
	P32	Sl_rearbitrate	PLB	O	Slave rearbitrate bus indicator
	P33	Sl_wait	PLB	O	Slave wait indicator
	P34	Sl_wrBTerm	PLB	O	Slave terminate write burst transfer
	P35	Sl_wrComp	PLB	O	Slave write transfer complete indicator
	P36	Sl_wrDAck	PLB	O	Slave write data acknowledge
	P37	Sl_SSize(0:1)	PLB	O	Slave data bus size
UART Signals	P38	baudoutN	Serial	O	Transmitter Clock
	P39	rclk	Serial	I	Receiver 16x Clock (Optional. May be driven by baudoutN under control of the C_HAS_EXTERNAL_RCLK parameter).
	P40	sin	Serial	I	Serial Data Input
	P41	sout	Serial	O	Serial Data Output
	P42	xin	Serial	I	Baud Rate Generator reference clock. (Optional. May be driven by SYS_plbClk under control of the C_HAS_EXTERNAL_XIN parameter).
	P43	xout	Serial	O	Inverted XIN
	P44	ctsN	Modem	I	ClearToSend (active low)
	P45	dcdN	Modem	I	Data Carrier Detect (active low)
	P46	dsrN	Modem	I	Data Set Ready (active low)
	P47	dtrN	Modem	O	Data Terminal Ready (active low)
	P48	riN	Modem	I	Ring Indicator (active low)
	P49	rtsN	Modem	O	Request To Send (active low)
	P50	ddis	User	O	Driver Disable. Low when CPU is reading PLB UART
	P51	out1N	User	O	User controlled output
	P52	our2N	User	O	User controlled output
	P53	rxrdyN	User	O	DMA control signal
	P54	txrdyN	User	O	DMA control signal

Table 2: **UART I/O Signals *(Continued)***

Grouping		Signal Name	Interface	I/O	Description
System	P55	SYS_plbClk	System	I	System clock
	P56	SYS_plbReset	System	I	System Reset (active high)
	P57	Freeze	System	I	Freezes UART for software debug (active high)
	P58	IP2INTC_Irpt	System	O	UART Interrupt output

Parameter - Port Dependencies

The width of many of the PLB UART signals depends on parameter. In addition, when certain features are parameterized away, the related input signals are unconnected . The dependencies between the PLB UART design parameters and I/O signals are shown in Table 3. parameters and I/O signals are shown in the following table.

Table 3: **Parameter-Port Dependencies**

		Name	Affects	Depends	Relationship Description
Design Parameters	G1	C_BASEADDR		G3	Bus width affects maximum allowable address.
	G2	C_PLB_DWIDTH	P3, P18, P30		Affects number of bits in bus.
	G3	C_PLB_AWIDTH	P2		Affects number of bits in bus.
	G4	C_DEV_BLK_ID			
	G5	C_DEV_MIR_ENABLE			
	G6	C_HIGHADDR		G3	Bus width affects maximum allowable address.
	G7	C_PLB_NUM_MASTERS	G8, P25, P26		Number of masters affects the number of Master IDs , the size of the Sl_Merr signal and the size of the Sl_Mbusy signal.
	G8	C_PLB_MID_WIDTH	P8	G7	Affects number of Master ID bits required
	G9	C_FAMILY			
	G10	C_HAS_EXTERNAL_XIN	P42		Connects XIN to SYS_plbClk
	G11	C_HAS_EXTERNAL_RCLK	P39		Connects RCLK to baudoutN
I/O Signals	P1	PLB_abort			
	P2	PLB_ABus(0:C_PLB_AWIDTH-1)		G3	Width varies with the size of the PLB Address bus.
	P3	PLB_BE(0:(C_PLD_DWIDTH / 8) -1)		G2	Width varies with the size of the PLB Data bus.

Table 3: **Parameter-Port Dependencies *(Continued)***

		Name	Affects	Depends	Relationship Description
	P4	PLB_busLock			
	P5	PLB_compress			
	P6	PLB_guarded			
	P7	PLB_lockErr			
	P8	PLB_masterID(0:C_PLB_MID_WIDTH-1)		G8	Number of Masters affects the number of ID bits
	P9	PLB_ordered			
	P10	PLB_PAValid			
	P11	PLB_rdBurst			
	P12	PLB_rdPrim			
	P13	PLB_RNW			
	P14	PLB_SAValid			
	P15	PLB_size(0:3)			
	P16	PLB_type(0:2)			
	P17	PLB_wrBurst			
	P18	PLB_wrDBus(0:C_PLB_DWIDTH -1)		G2	
	P19	PLB_wrPrim			
	P20	PLB_MSize(0:1)			
	P21	PLB_pendReq			
	P22	PLB_pendPri(0:1)			
	P23	PLB_reqPri(0:1)			
	P24	Sl_addrAck			
	P25	Sl_MBusy(0:C_NUM_MASTERS-1)		G7	Number of Masters affects the number of bits.
	P26	Sl_MErr(0:C_NUM_MASTERS-1)		G7	Number of Masters affects the number of bits.
	P27	Sl_rdBTerm			
	P28	Sl_rdComp			
	P29	Sl_rdDAck			
	P30	Sl_rdDBus(0:C_PLB_DWIDTH -1)		G2	Width varies with the size of the PLB Data bus.
	P31	Sl_rdWdAddr(0:3)			
	P32	Sl_rearbitrate			
	P33	Sl_wait			

Table 3: **Parameter-Port Dependencies *(Continued)***

		Name	Affects	Depends	Relationship Description
	P34	SI_wrBTerm			
	P35	SI_wrComp			
	P36	SI_wrDAck			
	P37	SI_SSize(0:1)			
	P38	baudoutN			
	P39	rclk		G11, P38	This input is unconnected and UART receiver clock is connected to baudoutN ii C_HAS_EXTERNAL_RCLK=0 .
	P40	sin			
	P41	sout			
	P42	xin		G10, P55	This input is unconnected and UART reference clock is connected to SYS_plbClk if C_HAS_EXTERNAL_XIN=0.
	P43	xout			
	P44	ctsN			
	P45	dcdN			
	P46	dsrN			
	P47	dtrN			
	P48	riN			
	P49	rtsN			
	P50	ddis			
	P51	out1N			
	P52	our2N			
	P53	rxrdyN			
	P54	txrdyN			
System	P55	SYS_plbClk			
	P56	SYS_plbReset			
	P57	Freeze			
	P58	IP2INTC_Irpt(1)			

UART Register Definition

UART Interface (IPIF)

The PLB memory map location of the PLB 16450 UART is determined by setting the parameter C_BASEADDR, in the IPIF interface module. The internal registers of the PLB 16450 UART are offset from the C_BASEADDR base address. Additionally, some of the internal registers are accessible only when bit 7of the Line Control Register (LCR) is set. The UART internal register set is described in Table 4. .

Table 4: **UART Registers**

Register Name	LCR(7)[1]+ C_BASEADDR + Address	Access
Receiver Buffer Register (RBR)	0 + C_BASEADDR + 0x1000	Read
Transmitter Holding Register (THR)	0 + C_BASEADDR + 0x1000	Write
Interrupt Enable Register (IER)	0 + C_BASEADDR + 0x1004	Read/Write
Interrupt Identification Register (IIR)	0 + C_BASEADDR + 0x1008	Read
Line Control Register (LCR)	X + C_BASEADDR + 0x100C	Read/Write
Modem Control Register (MCR)	X + C_BASEADDR + 0x1010	Read/Write
Line Status Register (LSR)	X + C_BASEADDR + 0x1014	Read/Write
Modem Status Register (MSR)	X + C_BASEADDR + 0x1018	Read/Write
Scratch Register (SCR)	X + C_BASEADDR + 0x101C	Read/Write
Divisor Register (DLL)	1 + C_BASEADDR + 0x1000	Read/Write
Divisor Register (DLM)	1 + C_BASEADDR + 0x1004	Read/Write

Notes:
1. X denotes don't care

UART Register Logic

This section tabulates the internal UART registers, including their reset values (if any).

Please refer to the National Semiconductor PC16550D UART with FIFOs data sheet (June, 1995), (http://www.national.com/pf/PC/PC16550D.html) for a more detailed description of the register behavior.

Receiver Buffer Register

As shown in Table 5, the Receiver Buffer Register contains the last received character.

Table 5: **Receiver Buffer Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	RBR	Read	"00000000"	RBR. Last received character

Transmitter Buffer Register

As shown in Table 6, the Transmitter Holding Register contains the character to be transmitted next.

Table 6: **Transmitter Holding Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	THR	Write	“11111111”	THR. Holds the character to be transmitted next

Interrupt Enable Register

As shown in Table 7, the Interrupt Enable Register contains the bits which enable interrupts.

Table 7: **Interrupt Enable Register Bit Definitions[1]**

Bit Location	Name	Access	Reset Value	Description
7-4		Read/Write	“**0**"	
3	EDSSI	Read/Write	"0"	Enable Modem Status Interrupt. "0" -> Disables Modem Status Interrupts. "1" -> Enables Modem Status Interrupts.
2	ELSI	Read/Write	"0"	Enable Receiver Line Status Interrupt. "0" -> Disables Receiver Line Status Interrupts. "1" -> Enables Receiver Line Status Interrupts.
1	ETBEI	Read/Write	"0"	Enable Transmitter Holding Register Empty Interrupt. "0" -> Disables Transmitter Holding Register Empty Interrupts. "1" -> Enables Transmitter Holding Register Interrupts.
0	ERBFI	Read/Write	"0"	Enable Received Data Available Interrupt. "0" -> Disables Received Data Available Interrupts. "1" -> Enables Received Data Available Interrupts.

Notes:
1. Bold faced bits are permanently low. Writing to these bits is allowed. Reading always returns "0".

Interrupt Identification Register

As shown in Table 8, the Interrupt Identification Register contains the priority interrupt identification.

Table 8: **Interrupt Identification Register Bit Definitions [1]**

Bit Location	Name	Access	Reset Value	Description
7-4		Read	“**0000**"	Always returns "0000"
3-1	INTID2	Read	“000"	**Interrupt ID.** [2] "011" -> Receiver Line Status (Highest). "010" -> Received Data Available (Second). "110" -> Character Timeout (Second). "001" -> Transmitter Holding Register Empty (Third). "000" -> Modem Status (Fourth).
0	INTPEND	Read	“1"	**Interrupt Pending**. Interrupt is pending when cleared.

Notes:
1. Bold faced bits are permanently low. Reading these bits always return "0"
2. If bit 0 is cleared. See National Semiconductor PC16550D data sheet for more detail.

Line Control Register

As shown in Table 9, the Line Control Register contains the serial communication configuration bits.

Table 9: **Line Control Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7	DLAB	Read/Write	“0”	Divisor Latch Access Bit. "1" -> Allows access to the Divisor Latch Registers and reading of the FIFO Control Register.
6	Set Break	Read/Write	“0”	Set Break. "1" -> Sets SOUT to "0".
5	Stick Parity	Read/Write	“0”	Stick Parity. "1" -> Forces parity to "1" or "0" based on bits 3 and 4.
4	EPS	Read/Write	“0”	Even Parity Select. 1 -> Selects Even parity. 0-> Selects Odd parity.

Table 9: **Line Control Register Bit Definitions *(Continued)***

Bit Location	Name	Access	Reset Value	Description
3	PEN	Read/Write	“0”	Parity Enable. "1" -> Enables parity.
2	STB	Read/Write	“0”	Number of Stop Bits. "0" -> 1 Stop bit. "1" -> 2 Stop bits or 1.5 if 5 bits/character selected).
1-0	WLS	Read/Write	“00”	Word Length Select. "00" -> 5 bits/character. "01" -> 6 bits/character. "10" -> 7 bits/character. "11" -> 8 bits/character.

Modem Control Register

As shown in Table 10, the Modem Control Register contains the modem signaling configuration bits.

Table 10: **Modem Control Register Bit Definitions [1]**

Bit Location	Name	Access	Reset Value	Description
7-5		Read/Write	“**000**"	
4	Loop	Read/Write	"0"	Loop Back. "1" -> Enables loop back.
3	Out2	Read/Write	"0"	User Output 2. "1" -> Drives OUT2N low. "0" -> Drives OUT2N high.
2	Out1	Read/Write	"0"	User Output 1. "1" -> Drives OUT1N low. "0" -> Drives OUT1N high.
1	RTS	Read/Write	"0"	Request To Send. "1" -> Drives RTSN low. "0" -> Drives RTSN high.
0	DTR	Read/Write	"0"	Data Terminal Ready. "1" -> Drives DTRN low. "0" -> Drives DTRN high.

Notes:
1. Bold faced bits permanently low.

Line Status Register

As shown in Table 11, the Line Status Register contains the current status of the receiver and transmitter.

Table 11: **Line Status Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7	Error in RCVR FIFO	Read/Write	“0”	Error in RCVR FIFO. RCVR FIFO contains at least one receiver error.
6	TEMT	Read/Write	“0”	Transmitter Empty.
5	THRE	Read/Write	“1”	Transmitter Holding Register Empty.
4	BI	Read/Write	“1”	Break Interrupt. Set when SIN is held low for an entire character time.
3	FE	Read/Write	“0”	Framing Error. Character missing a stop bit. Receiver resynchs with next character, if possible.
2	PE	Read/Write	“0”	Parity Error.
1	OE	Read/Write	“0”	Overrun Error. RBR not read before next character is received.
0	DR	Read/Write	“0”	Data Ready.

Modem Status Register

As shown in Table 12, the Modem Status Register contains the current state of the Modem interface.

Table 12: **Modem Status Register Bit Definitions** [1]

Bit Location	Name	Access	Reset Value	Description
7	DCD	Read/Write	“X”	Data Carrier Detect. Complement of DCDN input.
6	RI	Read/Write	"X"	Ring Indicator. Complement of RIN input.
5	DSR	Read/Write	"X"	Data Set Ready. Complement of DSRN input.
4	CTS	Read/Write	"X"	Clear To Send. Complement of CTSN input.

Table 12: **Modem Status Register Bit Definitions *(Continued)*[1]**

Bit Location	Name	Access	Reset Value	Description
3	DDCD	Read/Write	"0"	Delta Data Carrier Detect. Change in DCDN since last MSR read.
2	TERI	Read/Write	"0"	Trailing Edge Ring Indicator. RIN has changed from a low to a high.
1	DDSR	Read/Write	"0"	Delta Data Set Ready. Change in DSRN since last MSR read.
0	DCTS	Read/Write	"0"	Delta Clear To Send. Change in CTSN since last MSR read.

Notes:
1. X represents bit driven by external input.

Scratch Register

As shown in Table 13, the Scratch Register can be used to hold user data.

Table 13: **Scratch Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	Scratch	Read/Write	“00000000”	Scratch.

Divisor (Least Significant Byte) Register

As shown in Table 14, the Divisor (Least Significant Byte) Register holds the least significant byte of the baud rate generator counter.

Table 14: **Divisor (Least Significant Byte) Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	DLL	Read/Write	“00000000”	Divisor Least Significant Byte.

Divisor (Most Significant Byte) Register

As shown in Table 15, the Divisor (Most Significant Byte) Register holds the most significant byte of the baud rate generator counter.

Table 15: **Divisor (Most Significant Byte) Register Bit Definitions**

Bit Location	Name	Access	Reset Value	Description
7-0	DLM	Read/Write	“00000000”	Divisor Most Significant Byte.

UART Block Diagram

The top-level block diagram for the UART is shown in Figure 1.

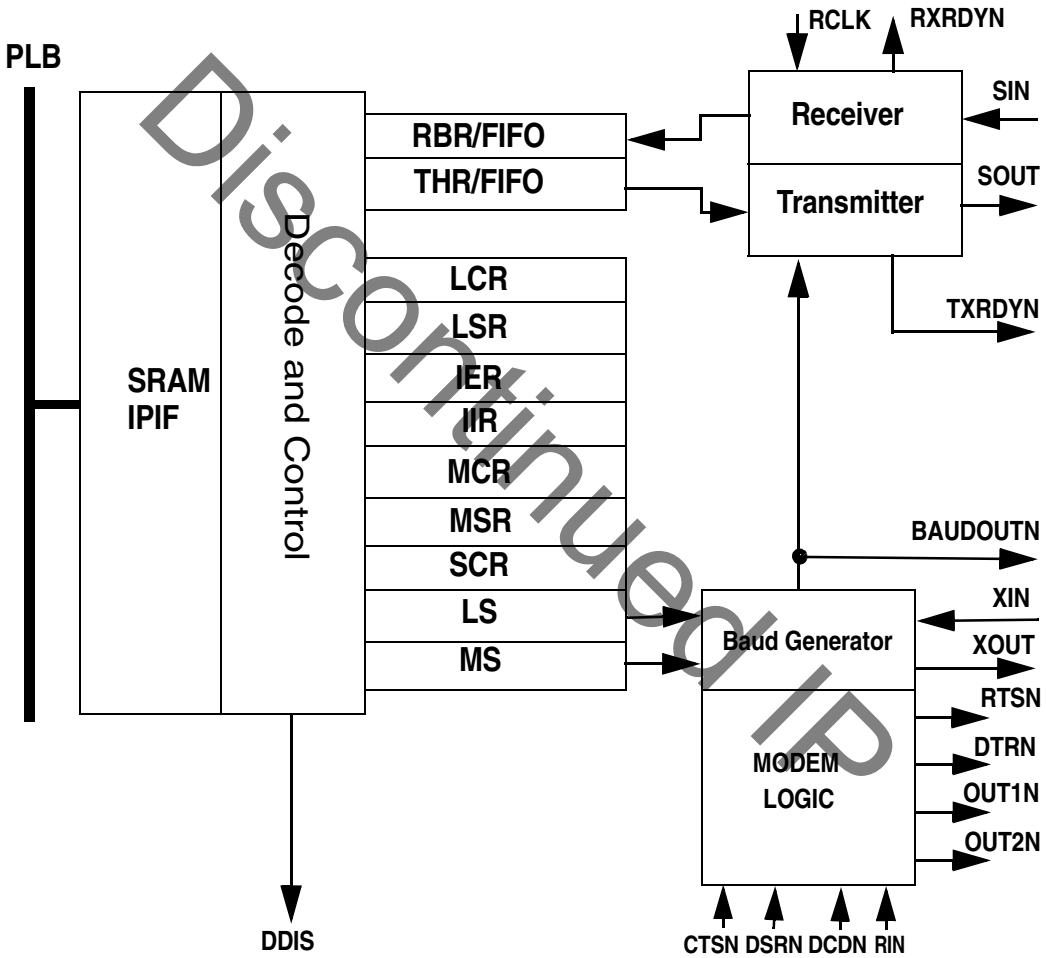

Figure 1: **UART Top-level Block Diagram**

Design Implementation

Device Utilization and Timing

All clocks, PLB_Clk, XIN, and RCLK are capable of running at 100 MHz. For best performance the USELOWSKEWLINES constraint should be placed on BAUDOUTn. If XIN and RCLK are provided as external inputs (C_HAS_EXTERNAL_XIN=1, C_HAS_EXTERNAL_RCLK=1) these signals should also use the USELOWSKEWLINES constraint.

Performance Benchmarks

Table 16: **Performance and Resource Utilization Benchmarks**

Parameter Values	Device Resources			f_{MAX} (MHz)
	Slices	Slice Flip-Flops	LUTs	f_{MAX}
OPB UART 16450	432	N/A	487	N/A

Specification Exceptions

System Clock

The asynchronous microprocessor interface of the National Semiconductor PC16550D is synchronized to the system clock input of the UART.

Register Addresses

All internal registers reside on a 32 bit word boundary not on 8 bit byte boundaries.

Reference Documents

The following documents contain reference information important to understanding the UART design:

- National Semiconductor PC16550D UART with FIFOs data sheet (June, 1995). (http://www.national.com/pf/PC/PC16550D.html)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/17/02	1.0	Initial Xilinx release.
05/28/02	1.1	Update to EDK 1.0
07/23/02	1.2	Add XCO parameters for System Generator
12/04/02	2.0	Rev to version c
01/09/03	2.1	Update for EDK SP3
05/15/03	2.2	Update LS and MS signal names
07/09/03	2.3	Update to new template