PLBv46 Monitor BFM

DS625 (v2.0) April 30, 2007 **Product Overview**

Introduction

The PLBv46 Monitor Bus Functional Model is a simulation hardware component that connects to a PLBv46 bus and continously samples the bus signals.

The component contains logic to automatically check for bus compliance or violations of the PLBv46 architecture and reports warnings and errors.

The model maintains an internal memory which can be initialized through the bus functional language and may be dynamically checked during simulation, or when all bus transactions have completed.

Features

- Xilinx PLBv46 bus interface
- Checks for bus compliance or violations
- Reports warnings and errors
- Behavior configured in a Bus Functional Language (BFL) file

More Information

For detailed information on the IBM PLB Bus Functional Model Toolkit, you may register for the **CoreConnect Lounge** on the Xilinx web site to get access to the IBM CoreConnect documentation.

Core Facts

Core Specifics		
Supported Device Family	All	
Version of Core	plbv46_ monitor_bfm	v1.00.a
Resources Used		
	Min	Max
I/O	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	This document	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	EDK 9.2 or later ISE 9.2 or later	
Verification	N/A	
Simulation	ModelSim SE/EE 6.1e or later	
Synthesis	N/A	
Support		
Support provided by Xilinx, Inc.		

Implementation

The PLB is a full-featured bus architecture with many features that increase bus performance. To obtain an efficient use of FPGA resource, Xilinx uses a subset of the PLB for Xilinx-developed PLBv46 devices.

The CoreConnect PLB monitor model has an interface to a full-featured PLB bus. Xilinx has created an interface to the Core-Connect Toolkit components for them to be used within the Xilinx implementation of the PLBv46 bus.

The CoreConnect PLB CoreConnect Toolkit contains standard Bus Functional Models and a Bus Functional Compiler for a rich Bus Functional Language specification. Xilinx utilizes these to provide the functionality and encapsulates the models around a customized interface that performs the translation between the two bus implementations domains. Figure 1 shows how this is done for the PLB monitor model.

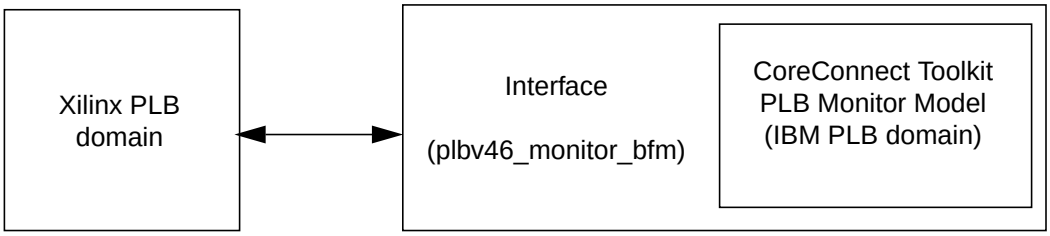

Figure 1: **Xilinx PLBv46 to IBM PLB domain interface**

MPD Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral s parameters that are fixed at simulation time. The parameters are described in Table 1.

Table 1: **MPD Parameters**

Parameter	Description	Allowable Values	Type
PLB_SLAVE_NUM	ID number	0b0000 - 0b1111	std_logic_vector
PLB_SLAVEn_ADDR_LO_0	PLB Slave n base address 0, where n = [0..7]	Valid PLB Address	std_logic_vector
PLB_SLAVEn_ADDR_HI_0	PLB Slave n high address 0, where n = [0..7]	Valid PLB Address	std_logic_vector
PLB_SLAVEn_ADDR_LO_1	PLB Slave n base address 1, where n = [0..7]	Valid PLB Address	std_logic_vector
PLB_SLAVEn_ADDR_HI_1	PLB Slave n high address 1, where n = [0..7]	Valid PLB Address	std_logic_vector
C_PLBV46_NUM_MASTERS	Number of Masters in the PLB bus	1-16	integer
C_PLBV46_NUM_SLAVES	Number of Slaves in the PLB bus	1-16	integer
C_PLBV46_MID_WIDTH	PLB Master ID width	1-4	integer

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
4/30/07	1.0	Initial Xilinx release