Processor System Reset Module (v1.00a)

DS406 August 10, 2004 **Product Specification**

Introduction

This specification defines the architecture and interface requirements for this module.

The Xilinx Processor System Reset Module design allows the customer to tailor the design to suit their application by setting certain parameters to enable/disable features. The parameterizable features of the design are discussed in Processor System Reset Module Design Parameters.

Features

- Asynchronous external reset input is synchronized with clock
- Asynchronous auxiliary external reset input is synchronized with clock
- Both the external and auxiliary reset inputs are selectable active high or active low
- Selectable minimum pulse width for reset inputs to be recognized
- Selectable load equalizing
- DCM Locked input
- Power On Reset generation
- Sequencing of reset signals coming out of reset:
  - First - bus structures come out of reset
    - PLB and OPB Arbiter and bridges for example
  - Second - Peripheral(s) come out of reset 16 clocks later
    - UART, SPI, IIC for example
  - Third - the CPU(s) come out of reset 16 clocks after the peripherals

Processor System Reset Module Circuit Description

The Processor System Reset Module has seven inputs and a minimum of five outputs. Also, there are six generics that can be set by the user. Additional outputs can be generated through the use of the generics C_NUM_BUS_RST and C_NUM_PERP_RST.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	proc_sys_reset	v1.00a
Resources Used		
	Min	Max
I/O	1	2
LUTs	37	57
FFs	52	82
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	Alliance Tool Suite	
Verification	N/A	
Simulation	N/A	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

Figure 1 shows the Processor System Reset Module timing when an Ext_Reset_In occurred. The timing diagram is identical for an occurrence of Aux_Reset_In.

For this example C_EXT_RST_WIDTH is set to 5 and C_EXT_RESET_HIGH is set to '0', active low.

Generic and Signal Description:

C_EXT_RST_WIDTH sets how wide, in number of Slowest_sync_clk clocks, a change on Ext_Reset_In must be before the change is detected and used by the Processor System Reset Module. For example if C_EXT_RST_WIDTH is set to 5, then the Ext_Reset_In must become active and stay active for at least five clocks before a reset is initiated.

There is a one or two clock latency caused by the meta-stability circuit. Since the Ext_Reset_In does not have be synchronous with the input clock the exact number of clocks can not be determined. The reset becomes active in six or seven clocks after the input has gone active and stayed active for five clocks.

After Ext_Reset_In has gone inactive for five clocks the sequencing to come out of reset begins. If, during the sequencing, Ext_Reset_In goes active for five or more clocks all outputs become active again.

C_AUX_RST_WIDTH sets the number of clocks wide a change on Aux_Reset_In must be before the change is detected and used by the Processor System Reset Module. Aux_Reset_In performs exactly the same as Ext_Reset_In.

C_EXT_RESET_HIGH is used to set the value for which Ext_Reset_In causes a reset. If this generic is set to a '1' then when Ext_Reset_In is high on a rising edge of clock then a reset is initiated.

C_AUX_RESET_HIGH is used to set the value for which Aux_Reset_In causes a reset. If this generic is set to a '0' then when Aux_Reset_In is low a reset is initiated.

C_NUM_BUS_RST is used to generate additional Bus_Struct_Reset signals. This helps with signal loading and routing. In general each bus may have its own Bus_Struct_Reset signal. For example, if a system has one PLB and two OPB's then C_NUM_BUS_RST may be set to three. However, the C_NUM_BUS_RST may be set to one and the three reset inputs can be driven be the same output. The Bus_Struct_Reset output(s) should reset the arbiter(s) and bridges located on the bus.

C_NUM_PERP_RST is used to generate additional Peripheral_Reset signals. This helps with signal loading and routing. In general every peripheral may have its own Peripheral_Reset signal. For example, if there is one ATM on the PLB and two UARTs, one 10/100 Ethernet controller and one IIC on the OPB, then C_NUM_PERP_RST may be set to five. However, the C_NUM_PERP_RST may be set to one and all peripheral resets can be driven by the same output.

DCM_Locked is an input to the reset module, if the system does not use any DCM's this input should be tied high. If the system uses one DCM to generate system clocks the output from the DCM should be connected to the input on the reset module. If the system contains more than one DCM to generate system clocks, the DCM output that achieves lock last should be connected to the input.

The Slowest_Sync_Clk input should be connected to the slowest synchronous clock used in the system. This is typically the OPB clock, however, it could be any of the bus or CPU clocks.

The Core_Reset_Request, Chip_Reset_Request, and System_Reset_Request inputs are signals generated by the 405 core. Each of these resets can be generated by a JTAG command, or by the second expiration of the watchdog timer or by writing a non-zero value to the reset (RST) field of the Debug Control Register 0 (DBCR0). The Core_Reset_Request only activates the Rst405resetcore, no other logic is reset.

The Chip_Reset_Request causes the Rst405resetcore, the Rstc405resetchip, the Bus_Struct_Reset and the Peripheral_Reset to occur. A System_Reset_Request causes all the above and the Rstc405resetsys.

A Core_Reset_Request is stretched such that the output remains active for at least 15 clocks (see Figure 2). A Chip_Reset_Request is stretched such that the outputs remain active for 48 clocks (see Figure 3). A System_Reset_Request is stretched such that the outputs remain active for at least 61 clocks (see Figure 4).

All outputs go active on the same edge of the clock. However, there is sequencing that occurs when releasing the reset signal. The first reset to go inactive is the Bus_Struct_Reset, 16 clocks later the Peripheral_Reset will go inactive, 16 clocks later the 405 core, chip (and system, if a system reset was commanded) will go inactive. At this point all the resets are inactive and processing can begin.

Both the Ext_Reset_In and Aux_Reset_In will cause a Rstc405resetsys, a Rstc405resetchip and a Rst405resetcore.

The Power On Reset condition will cause all the reset outputs to become active within the first two clocks of a power up and remain active for 16 clocks. The resets will then begin the sequencing as shown in Figure 1.

.

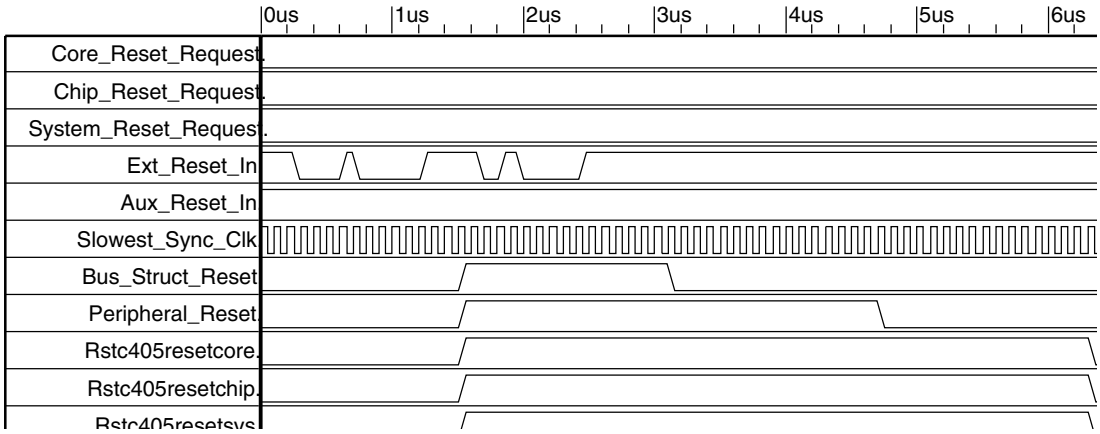

Figure 1: ***Processor System Reset Module - Ext_Reset_In (active low)***

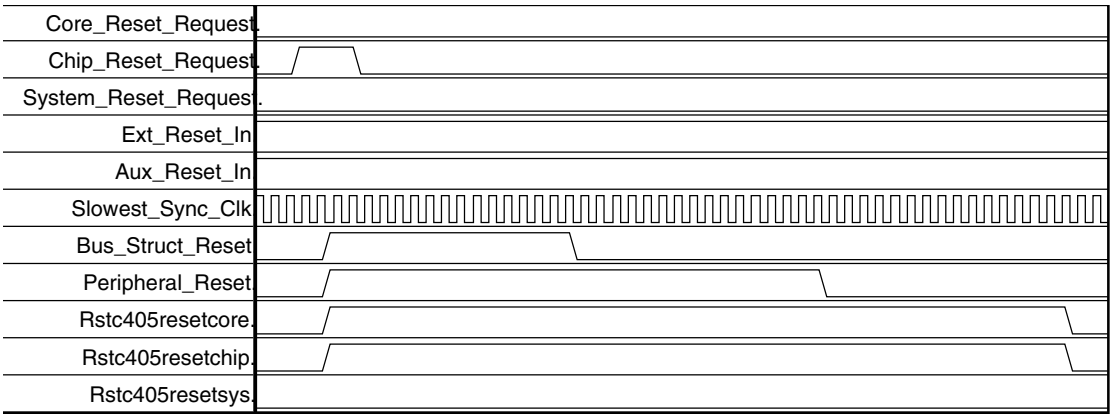

Figure 2: ***Processor System Reset Module - Chip_Reset_Request***

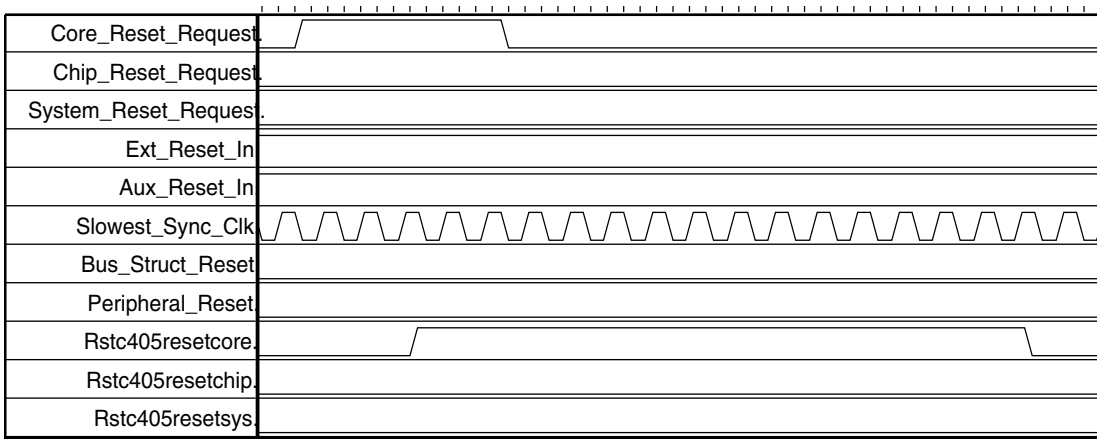

Figure 3: **Processor System Reset Module - Core_Reset_Request**

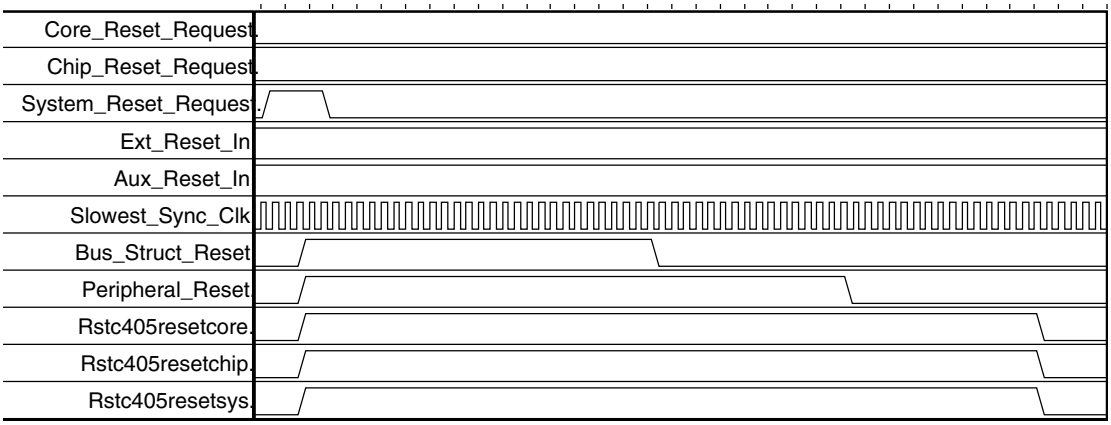

Figure 4: **Processor System Reset Module - System_Reset_Request**

Processor System Reset Module Design Parameters

To allow you to obtain a Processor System Reset Module that is uniquely tailored for your system, certain features can be parameterized in the Processor System Reset Module design. This allows you to have a design that utilizes only the resources required by your system and runs at the best possible performance. The features that can be parameterized in the Xilinx Processor System Reset Module design are shown in the following table:

Table 1: **Processor System Reset Module Design Parameters**

Grouping / Number		Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Processor System Reset Module Features	G1	Number of clocks before input change is recognized on the external reset input	C_EXT_RST_WIDTH	1 - 16	4	integer
	G2	Number of clocks before input change is recognized on the auxiliary reset input	C_AUX_RST_WIDTH	1 - 16	4	integer
	G3	Defines the active state of the external reset input	C_EXT_RESET_HIGH	'1' = Reset generated when external reset = '1' '0' = Reset generated when external reset = '0'	1	std_logic
	G4	Defines the active state of the auxiliary reset input	C_AUX_RESET_HIGH	'1' = Reset generated when external reset = '1' '0' = Reset generated when external reset = '0'	1	std_logic
	G5	Number of bus structure reset registered outputs. In general, may equal number of instantiated buses.	C_NUM_BUS_RST	1 - 8	1	integer
	G6	Number of peripheral reset registered outputs. In general, may equal number of peripherals.	C_NUM_PERP_RST	1 - 16	1	integer

Processor System Reset Module I/O Signals

The I/O signals for the Processor System Reset Module are listed in Table 2. The interfaces referenced in this table are shown in Figure 5 the Processor System Reset Module block diagram.

Table 2: **Processor System Reset Module I/O Signals**

Grouping		Signal Name	Interface	I/O	Description
System	P1	Slowest_sync_clk	System	I	Slowest Synchronous Clock - Typically OPB clock
	P2	Ext_Reset_In	System	I	External Reset Input - Active high or low based upon the generic C_EXT_RESET_HIGH
	P3	Aux_Reset_In	System	I	Auxiliary Reset Input - Active high or low based upon the generic C_AUX_RESET_HIGH
	P4	Core_Reset_Req	System	I	405 requesting a core reset
	P5	Chip_Reset_Req	System	I	405 requesting a chip reset
	P6	System_Reset_Req	System	I	405 requesting a system reset
	P7	Dcm_locked	System	I	DCM locked will cause all outputs to remain active until Dcm_locked goes high which will cause the resets to sequence to their inactive state.
	P8	rstc405resetcore	System	O	405 core reset - active high
	P9	rstc405resetchip	System	O	405 chip reset - active high
	P10	rstc405resetsys	System	O	405 system reset - active high
	P11	Bus_Struct_Reset(0 to C_NUM_BUS_RST - 1)(1)	System	O	Bus Structures reset - e.g. arbiters for PLB, OPB or Bridges ... etc. (active high)
	P12	Peripheral_Reset(0 to C_NUM_PERP_RST - 1)(2)	System	O	Peripheral reset is for all peripherals attached to any bus that is synchronous with the Slowest_sync_clk. (active high)

Notes:

1. To help equalize loading on this signal, there can be from 1 to 8 copies generated with each copy being individually registered through a D-flip flop. In general each unique bus should receive a different copy of this signal.
2. To help equalize loading on this signal, there can be from 1 to 16 copies generated with each copy being individually registered through a D-flip flop. In general each peripheral should receive a different copy of this signal.

Processor System Reset Module Port Dependencies

The width of some of the Processor System Reset Module signals depends on parameters set by generic inputs to the design. The dependencies between the Processor System Reset Module design parameters and I/O signals are shown in Table 3.

Table 3: **ParameterPort Dependencies**

		Name	Affects	Depends	Relationship Description
Design Parameters	G5	C_NUM_BUS_RST	P11		The number of bus structure reset outputs is set by this generic
	G6	C_NUM_PERP_RST	P12		The number of peripheral reset outputs is set by this generic
I/O Signals	P11	Bus_Struct_Reset(0 to C_NUM_BUS_RST - 1)		G5	Width varies with the size of the C_NUM_BUS_RST.
	P12	Peripheral_Reset(0 to C_NUM_PERP_RST - 1)		G6	Width varies with the size of the C_NUM_PERP_RST.

Processor System Reset Module Block Diagram

The top-level block diagram for the Processor System Reset Module is shown in Figure 5.

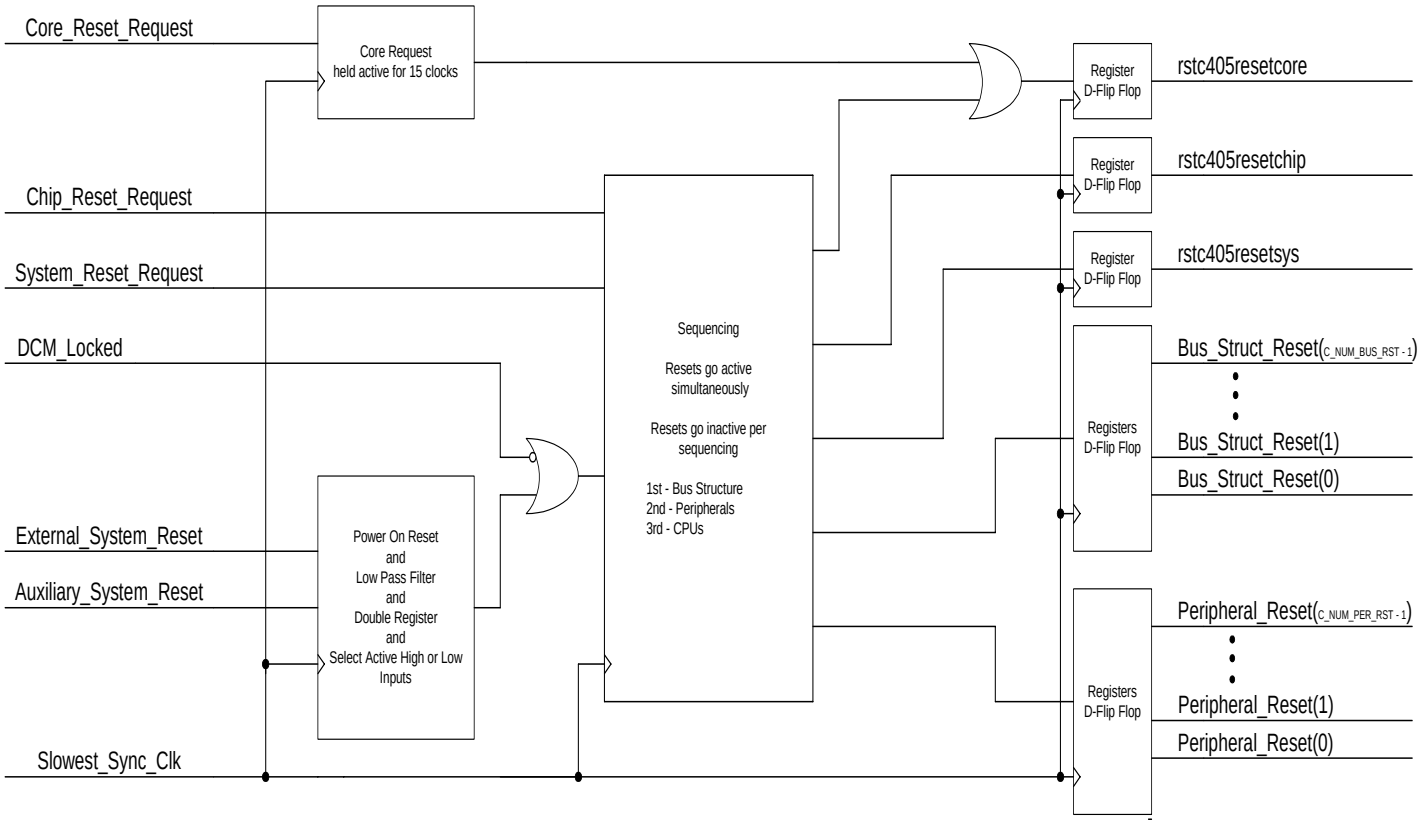

Figure 5: ***Processor System Reset Module*** **Top-level Block Diagram**

Design Implementation

Target Technology

The intended target technology is a Virtex-II FPGA.

Device Utilization and Performance Benchmarks

Since the Processor System Reset Module will be used with other design pieces in the FPGA, the utilization and timing numbers reported in this section are just estimates. As the Processor System Reset Module is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the Processor System Reset Module design will vary from the results reported here.

In order to analyze the Processor System Reset Module timing within the FPGA, a design was created that instantiated the Processor System Reset Module with the following parameters set.

The Processor System Reset Module benchmarks are shown in Table 4 for a Virtex-II XC2V250-5CS144 FPGA.

Table 4: **Processor System Reset Module FPGA Performance and Resource Utilization Benchmarks (Virtex-II -5)**

Parameter Values (For Example)						Device Resources			f_{MAX}
C_EXT_RST_WIDTH	C_AUX_RST_WIDTH	C_EXT_RESET_HIGH	C_AUX_RESET_HIGH	C_NUM_BUS_RST	C_NUM_PERP_RST	Slices	Slice Flip-Flops	4-input LUTs	MHz
1	1	1	1	1	1	53	52	37	290
4	4	1	1	1	1	59	58	41	290
16	16	0	0	8	16	79	82	57	290

Notes:

1. These benchmark designs contain only the Processor System Reset Module without any additional logic. Benchmark numbers approach the performance ceiling rather than representing performance under typical user conditions.

Revision History

Date	Version	Revision
11/05/01	1.0	Initial Xilinx release.
02/27/02	1.1	Added DCM locked as an input and Power On Reset.
06/04/02	1.2	Update to EDK 1.0
07/22/02	1.3	Add XCO parameters for SysGen
01/07/03	1.4	Update for EDK SP3
07/08/03	1.5	Update to new template
11/19/03	1.5.1	Edit for CR 179061
8/10/04	1.6	Update to EDK Gmm. Updated trademarks, supported devices families listing, made minor content and formatting edits, updated legal info footer on 1st page.