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The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/30/04	1.0	Initial Xilinx release.
11/11/04	1.1	Updated document with changes to performance numbers of the dynamic phase alignment configuration of the core.
04/28/05	1.2	Updated document to indicate support for Xilinx ISE Foundation v7.1i.
08/31/05	2.0	Added SP 3 to Xilinx ISE v7.1i, section about Global Clocking with DCM edited, various copy edits.
01/18/06	3.0	Updated ISE to v8.1i, revised dynamic alignment section.
07/13/06	4.0	Added support for Virtex-5, Updated ISE to v8.2i, release date.
09/21/06	4.1	Added new DPA-related signals. Updated for IP2i minor release.
02/15/07	4.2	Updated for IP1Jade release.
8/08/07	4.3	Updated for the IP1 Jade Minor release. Added SnkldelayCtlRdy Input signal.
03/24/08	4.4	Modified description of ScerAFTHresAssert[8:0] signal in Table 12, updated supported tools and core version.
09/19/08	4.5	Updated for the ISE service pack 3 release.
04/24/09	5.0	Updated core version to 9.1 and ISE to version 11.1. Added support for Virtex-6 devices.
06/24/09	5.5	Updated core version to 9.2 and ISE to version 11.2.
09/16/09	6.0	Updated core version to 9.3 and ISE to version 11.3. Added support for Virtex-6-1L and Virtex-6-XT devices.
04/22/10	7.0	Updated core version to 10.1 and ISE version to 12.1; added support for Spartan-6 devices.
09/21/10	8.0	Updated core version to 10.2 and ISE version to 12.3.
12/14/10	9.0	Updated core version to 10.3 and ISE version to 12.4; removed Spartan-6 support and updated Virtex-6 performance numbers and supported clocking scheme.
3/1/11	10.0	Updated core version to 10.4 and ISE version to 13.1.

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