3GPP Turbo Encoder v5.0

LogiCORE IP Product Guide

Vivado Design Suite

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XILINX

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Appendix C: Additional Resources and Legal Notices

Introduction

This version of the Turbo Convolution Code (TCC) encoder is designed to meet the 3GPP mobile communication system specification [Ref 1], [Ref 2]. Optional outputs for code rate 1/5 are provided for additional flexibility.

Features

- Implements the 3GPP/UMTS specification [Ref 1] [Ref 2]
- Core contains the full 3GPP interleaver
- Full 3GPP block size range 40 - 5114 supported
- Up to 16 simultaneous data channels
- Double-buffered symbol memory for maximum throughput
- Rate 1/3 parity outputs for 3GPP and optional outputs for rate 1/5 for additional error correction capability
- Flexible interfacing using optional control signals
- External RAM option
- External address generator option enables interfacing to customer-designed interleaver

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Versal™ ACAP UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 SoC, 7 Series
Supported User Interfaces	N/A
Resources	Performance and Resource Utilization web page
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	VHDL Behavioral VHDL and Verilog Structural
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 54472
All Vivado IP Change Logs	Master Vivado IP Change Logs: 72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of third-party tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

- **Hardware, IP, and Platform Development:** Creating the PL IP blocks for the hardware platform, creating PL kernels, subsystem functional simulation, and evaluating the Vivado timing, resource and power closure. Also involves developing the hardware platform for system integration. Topics in this document that apply to this design process include:
  - Port Descriptions
  - Clocking
  - Resets
  - Customizing and Generating the Core

Core Overview

The theory of operation of the Turbo Codes is described in the paper by Berrou, Glavieux, and Thitimajshima. [Ref 3].

The 3GPP Turbo Encoder input and output ports are shown in Figure 1-1 and the internal architecture is shown in Figure 1-2. It is a block-based processing unit where blocks of between 40 and 5114 bits are input using the DATA_IN port and processed. Each block of data is processed in two identical Recursive Systematic Convolutional (RSC) encoders, which generate high-weight codes. RSC1 processes the raw input data while RSC2 processes an interleaved version of the input data. The coding operates on the principle that if an input symbol is corrupted in the sequence from RSC1, then it is unlikely also to be corrupted in the re-ordered sequence from RSC2, and vice versa.

The delay shown in Figure 1-2 is used to indicate that the input data is delayed before passing through RSC1. This ensures that the systematic data from RSC1 and RSC2 are block-aligned at the output.

For the 3GPP standard [Ref 1] [Ref 2], a rate 1/3 turbo encoder is specified. In this case only the systematic and parity0 signals are generated for each RSC. For additional flexibility and error correction capability, you can select a rate 1/5 option, in which case the two parity1 outputs are made available.

Often some of the encoded output bits need not be transmitted, so they are omitted, or *punctured* from the output stream. Puncturing offers a dynamic trade-off between code rate and error performance. When the channel is noisy or the data requires more protection, extra redundancy can be added, therefore lowering the code rate. Puncturing is not implemented as part of the core; all outputs are provided by the core which allows you maximum flexibility.

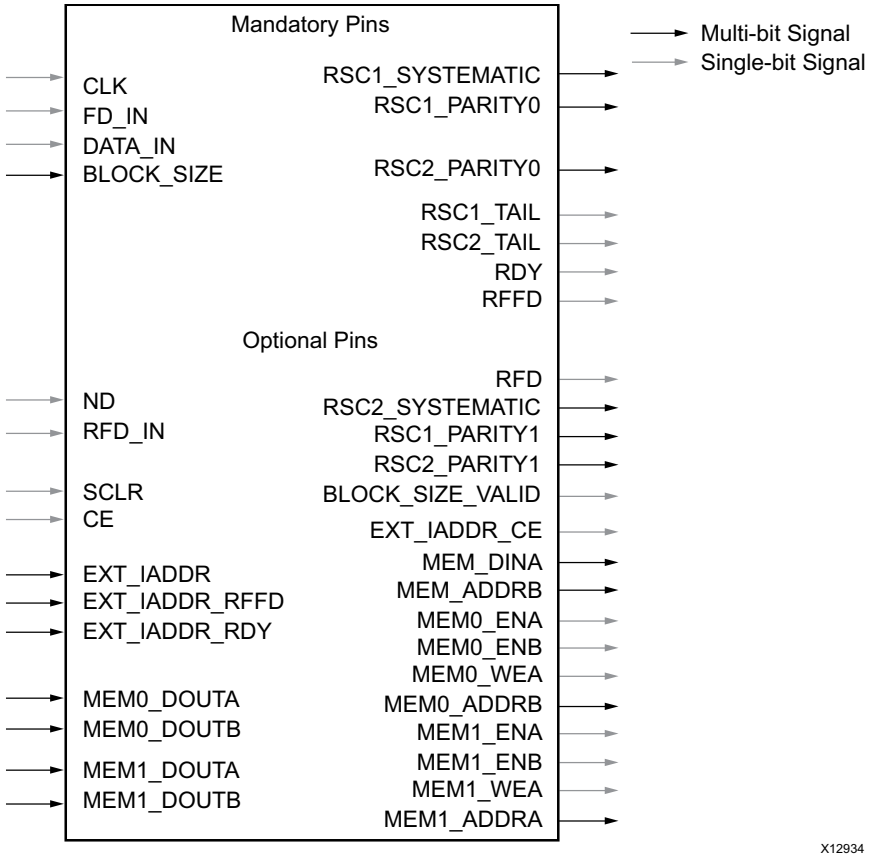

Figure 1-1: **TCC Encoder Structure**

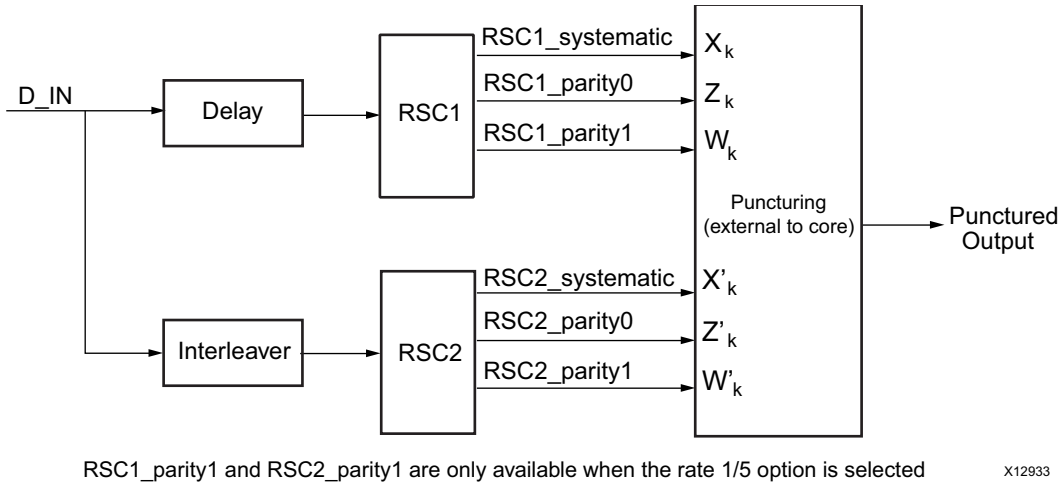

Figure 1-2: **TCC Encoder Structure**

Applications

This version of the Turbo Convolution Code encoder is designed to meet the 3GPP mobile communication system specification. Generally, this encoder is used with a corresponding decoder to provide a high performance error correction system.

Licensing and Ordering

This Xilinx LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado® Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. To generate a full license, visit the product licensing web page. Evaluation licenses and hardware timeout licenses might be available for this core or subsystem. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, visit the Turbo Encoder product web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

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France Telecom R&D
VAT/TURBOCODES 38
rue du Général Leclerc
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Cedex 9
France

License Checkers

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado design tools: Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Product Specification

Standards

This version of the Turbo Convolution Code (TCC) encoder is designed to meet the following 3GPP module communication system specifications:

- *3G TS.25.222 V5.5.0 Multiplexing and Channel Coding (TDD) specification* [Ref 1]
- *3G TS.25.212 V6.0.0 Multiplexing and Channel Coding (FDD) specification* [Ref 2]

Resource Utilization

For full details about performance and resource utilization, visit the Performance and Resource Utilization web page.

Port Descriptions

The I/O ports are summarized and described in the following sections:

- Basic Configuration
- External Address Generator Option
- External RAM Option

Basic Configuration

The I/O ports for the basic configuration are summarized and described in Table 2-1.

Table 2-1: **I/O Ports, Basic Configuration**

Pin	Sense	Port Width (bits)	Description
FD_IN	Input	1	**First Data** - When this is asserted (High) on a valid clock edge, the encoding process is started.
ND	Input (optional)	1	**New Data** - When this is asserted (High) on a valid clock edge, a new input value is read from the DATA_IN port.
SCLR	Input (optional)	1	**Synchronous Clear** - When this is asserted (High) on an active clock edge, the encoder is reset.
CE	Input (optional)	1	**Clock Enable** - When this is deasserted (Low), rising clock edges are ignored and the core is held in its current state.
CLK	Input	1	**Clock** - All synchronous operations occur on the rising edge of the clock signal.
BLOCK_SIZE	Input	13	**Block Size** - The block size of the current encode operation.
DATA_IN	Input	1 to 16	**Data Input** - The data to be encoded.
RSC1_SYSTEMATIC	Output	1 to 16	**RSC1_systematic** - The systematic output from RSC1.
RSC1_PARITY0	Output	1 to 16	**RSC1_parity0** - The parity0 output from RSC1.
RSC1_PARITY1	Output (optional)	1 to 16	**RSC1_parity1** - The parity1 output from RSC1.
RSC2_SYSTEMATIC	Output (optional)	1 to 16	**RSC2_systematic** - The systematic output from RSC2.
RSC2_PARITY0	Output	1 to 16	**RSC2_parity0** - The parity0 output from RSC2.
RSC2_PARITY1	Output (optional)	1 to 16	**RSC2_parity1** - The parity1 output from RSC2.
RSC1_TAIL	Output	1	**RSC1_tail** - Indicates that the tail bits are being output on RSC1 when asserted (High).
RSC2_TAIL	Output	1	**RSC2_tail** - Indicates that the tail bits are being output on RSC2 when asserted (High).
RFFD	Output	1	**Ready For First Data** - When this is asserted (High), the core is ready to start another encoder operation.
RFD	Output (optional)	1	**Ready For Data** - When this is asserted (High), the core is ready to accept input on the DATA_IN port.
RDY	Output	1	**Ready** - Indicates that there is valid data on the systematic and parity outputs when asserted (High).
BLOCK_SIZE_VALID	Output (optional)	1	**Block Size Valid** - Indicates that the block size which was sampled on the BLOCK_SIZE port on the last valid-FD is a valid 3GPP block size in the range 40 through 5114. The BLOCK_SIZE_VALID port is not available if the external address generator option is selected.

Clock (CLK)

With the exception of asynchronous clear, all operations of the core are synchronized to the rising edge of CLK. If the optional CE pin is enabled, an active rising clock edge occurs only when CE is High, and if CE is Low, the core is held in its current state.

Data In (DATA_IN)

The DATA_IN port is a mandatory input port which carries the unencoded data. The input process is started with a valid-FD signal, and data is read serially into the DATA_IN port on a clock-by-clock basis. Block size clock cycles are, therefore, required to input each block. DATA_IN can be qualified by the optional ND port. See New Data (ND).

First Data (FD_IN)

FD_IN is a mandatory input port which is used to start the encoder operation. FD_IN is qualified by the optional ND input. If ND is not selected, a *valid-FD* means that FD_IN is sampled High on an active rising clock edge. If ND is selected, a *valid-FD* means that FD_IN and ND are both sampled High on an active rising clock edge.

When a *valid-FD* occurs, the first data is read from the DATA_IN port, and the block size is read from the BLOCK_SIZE port. The core then continues loading data, until a complete block has been input.

The FD_IN input should only be asserted when the RFFD output is High. See Ready For First Data (RFFD).

Block Size (BLOCK_SIZE)

This port determines the size of the block of data that is about to be written into the encoder. The block size value is sampled on an active rising clock edge when FD_IN is High and ND (if selected) is High. If an invalid block size, (that is, not in the range 40-5114) is sampled, the behavior of the core is not specified.

Ready For First Data (RFFD)

When this signal is asserted High, it indicates that the core is ready to accept an FD_IN signal to start a new encoding operation. When a valid-FD signal is sampled, the RFFD signal goes Low and remains Low until it is safe to start another block.

RSC1 Systematic Output (RSC1_SYSTEMATIC)

RSC1_SYSTEMATIC is a mandatory output port, which is a delayed version of the uninterleaved input data. During trellis termination, the RSC1_SYSTEMATIC port also carries systematic and parity tail bits.

RSC1 Parity0 Output (RSC1_PARITY0)

RSC1_PARITY0 is a mandatory output port, which is the Y0 output from RSC1. (See Figure 1-1 and Figure 1-2.)

During trellis termination, the RSC1_PARITY0 port also carries systematic and parity tail bits.

RSC1 Parity1 Output (RSC1_PARITY1)

RSC1_PARITY1 is an optional output port, which is the Y1 output from RSC1. This port is enabled if Code Rate 1/5 is enabled. (See Figure 1-1 and Figure 1-2.)

RSC2 Systematic Output (RSC2_SYSTEMATIC)

RSC2_SYSTEMATIC, if enabled, is a delayed and interleaved version of the input data. This port is disabled when the Multiplexed Tail Bits option is selected. (See Figure 1-1 and Figure 1-2.)

RSC2 Parity0 Output (RSC2_PARITY0)

RSC2_PARITY0 is a mandatory output port, which is the Y0 output from RSC2. (See Figure 1-2.)

During trellis termination, the RSC2_PARITY0 port also carries systematic and parity tail bits.

RSC2 Parity1 Output (RSC2_PARITY1)

RSC2_PARITY1 is an optional output port, which is the Y1 output from RSC2. This port is enabled if Code Rate 1/5 is enabled. (See Figure 1-1 and Figure 1-2.)

RSC1 Tail Output (RSC1_TAIL)

RSC1_TAIL is a mandatory output port, which is asserted High at the end of each output block to indicate trellis termination of RSC1. RSC1_TAIL goes High for two clock cycles for multiplexed tail bits, or three clock cycles for non-multiplexed tail bits.

RSC2 Tail Output (RSC2_TAIL)

RSC2_TAIL is a mandatory output port, which is asserted High at the end of each output block to indicate trellis termination of RSC2. RSC2_TAIL goes High for two clock cycles for multiplexed tail bits, or three clock cycles for non-multiplexed tail bits.

Ready (RDY)

This signal is asserted High when there is valid data on the SYSTEMATIC and PARITY output ports, including the tail bits. RDY is asserted for block size+four clock cycles for multiplexed tail bits, or block size+six clock cycles for non-multiplexed tail bits.

Multichannel Operation

Up to 16 simultaneous data channels can be supported.

If multichannel operation is selected, then the width of the DATA_IN, SYSTEMATIC and PARITY ports are increased to *N*, where *N* is the number of data channels. Multichannel mode assumes that the *N* channels are of identical block size and are block-aligned. Control signals CE, ND, FD_IN, and RFD_IN have the same effect on all *N* channels. If the external RAM option is selected, the external memory data input and output ports also have width N.

External Address Generator Option

The I/O ports for the external address generator option are described in Table 2-2and should be connected as shown in Figure 2-1.

Table 2-2: **I/O Ports for External Address Generator Option**

Pin	Sense	Port Width (bits)	Description
EXT_IADDR	Input	min 6 max 13	**External Interleaved Address -** can be configured to have any width from 6 through 13 bits.
EXT_IADDR_RFFD	Input	1	**External Address Generator Ready For FD** - Indicates that the external address generator has finished processing the current block, and is ready to start calculating the addresses for a new block. If the external address generator needs time to calculate the first interleaved address of a block, EXT_IADDR_RFFD can be asserted early to achieve maximum throughput.
EXT_IADDR_RDY	Input	1	**External Interleaved Address Ready** - Indicates that a valid address is on the EXT_IADDR port.
EXT_IADDR_CE	Output	1	**External Address Generator Clock Enable** - Indicates that the encoder is ready to receive an address from the external address generator. It depends on the state of the encoder and the CE and RFD_IN inputs, if selected.

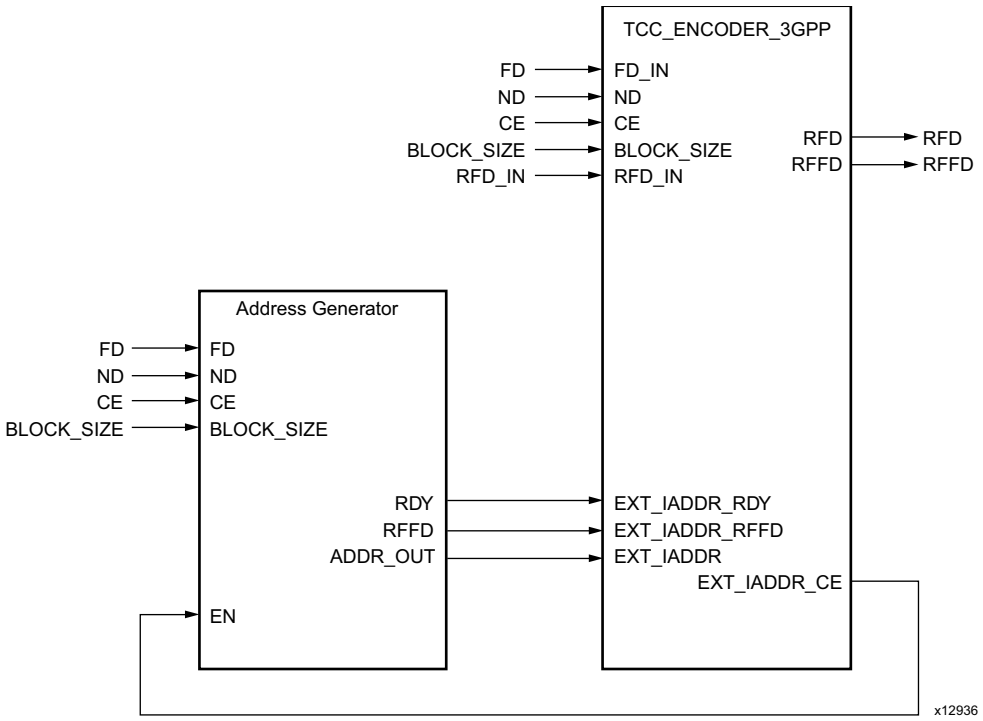


Figure 2-1: **External Address Generator Option**

External RAM Option

The I/O ports for the external RAM option are summarized in Table 2-3 and should be connected as shown in Figure 2-2.

Table 2-3: **I/O Ports for External RAM Option**

Pin	Sense	Port Width (bits)	Description
MEM_DINA	Output	1 to 16	**Data inputs, Port A -** Common to both external RAMs.(1)
MEM_ADDRB	Output	6 to 13	**Port B address** - Common to both external RAMs. This is the Interleaved read address.(2)
MEM0_ENA	Output	1	**Port A Enable, MEM0**
MEM0_ENB	Output	1	**Port B Enable, MEM0**
MEM0_WEA	Output	1	**Port A Write Enable, MEM0**(3)
MEM0_ADDRA	Output	6 to 13	**Port A address for MEM0 -** Alternately carries the write address and the uninterleaved read address.(2)
MEM0_DOUTA	Input	1 to 16	**Data Outputs, Port A -** Uninterleaved systematic data for RSC1. Active when outputting from MEM0.(1)
MEM0_DOUTB	Input	1 to 16	**Data Outputs, Port B** - Interleaved systematic data for RSC2. Active when outputting from MEM0.(1)
MEM1_ENA	Output	1	**Port A Enable, MEM1**

Table 2-3: **I/O Ports for External RAM Option *(Cont'd)***

Pin	Sense	Port Width (bits)	Description
MEM1_ENB	Output	1	**Port B Enable, MEM1**
MEM1_WEA	Output	1	**Port A Write Enable, MEM1**(3)
MEM1_ADDRA	Output	6 to 13	**Port A address for MEM1 -** Alternately carries the write address and the uninterleaved read address.(2)
MEM1_DOUTA	Input	1 to 16	**Data Outputs, Port A -** Uninterleaved systematic data, for RSC1. Active when outputting from MEM1.(1)
MEM1_DOUTB	Input	1 to 16	**Data Outputs, Port B** - Interleaved systematic data, for RSC2. Active when outputting from MEM1.(1)

Notes:

1. Width of memory data buses equals the number of channels.
2. Width of memory address buses is 13 if the address generator is internal, or is equal to the width of the external address generator.
3. Port B is read only, so the WEB ports of both external RAMs should be connected to logic 0, and the DINB ports can be left unconnected.

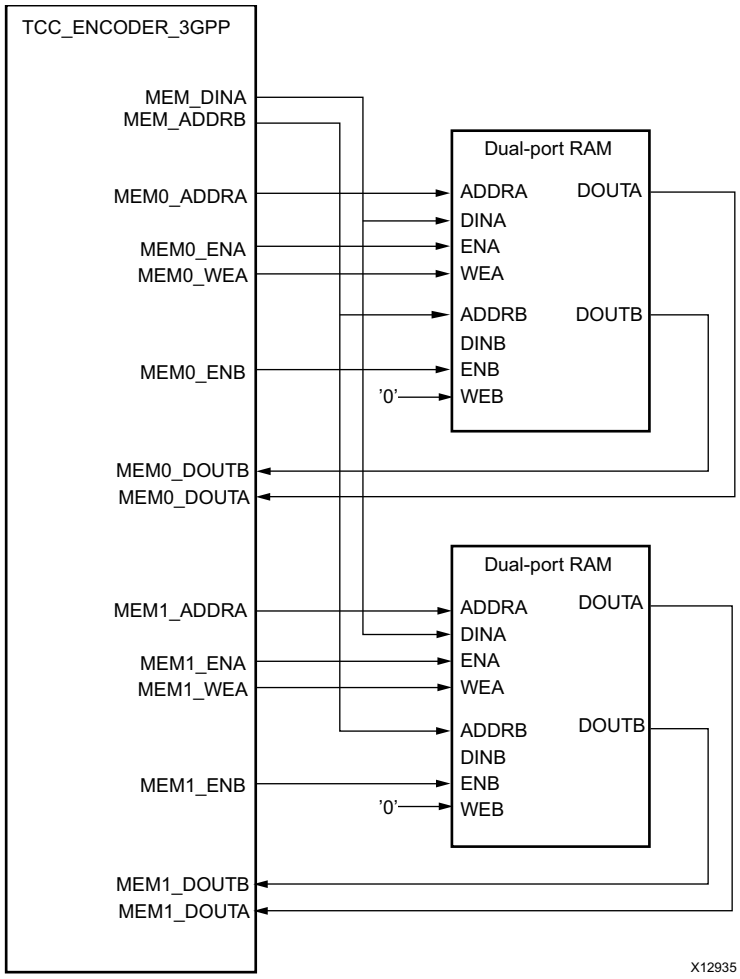


Figure 2-2: **External RAM Option**

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

Recursive Systematic Convolution (RSC) Encoder Structure

The schematic for each of the two RSCs and the transfer functions for the outputs are shown in Figure 3-1. Parity1(Y_1) can be optionally enabled if a rate 1/5 encoder is desired. This is not required by the 3GPP specification [Ref 1] [Ref 2].

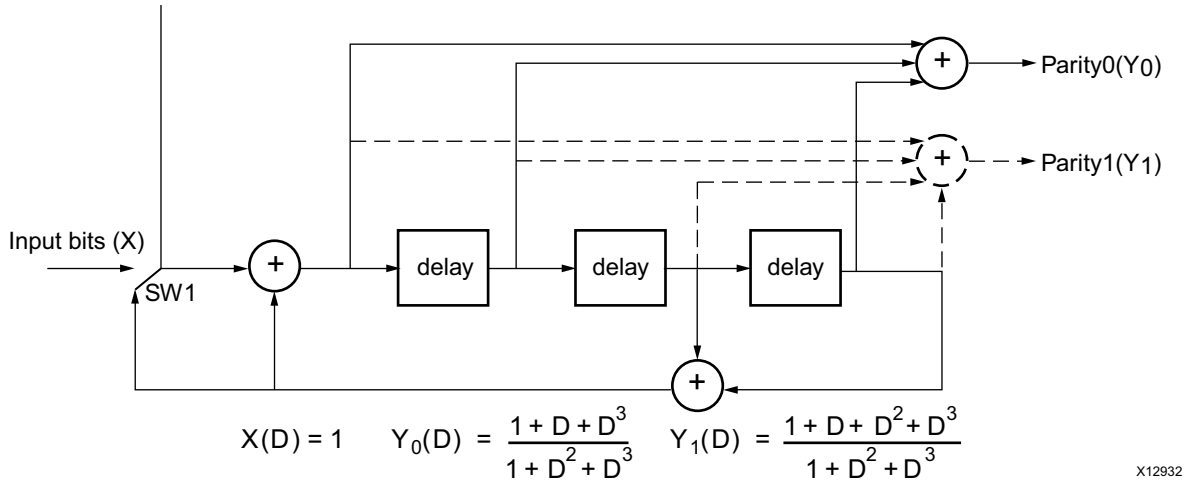


Figure 3-1: **TCC RSC Structure**

After a block of input data has been coded, the RSCs must return to the initial zero state. To force the RSC back to the all zero state, the input value is set equal to the feedback value by setting the control switch, SW1, to the lower position for three clock cycles. During the first three tail bit periods, RSC2 is disabled, and the control switch of RSC1 is set to the lower position to output the RSC1 tail bits on the RSC1 systematic and parity outputs. During the last three tail bit periods, RSC1 is disabled and the control switch of RSC2 is set to the lower position to output the RSC2 tail bits on the RSC2 systematic and parity outputs.

The RSC2 systematic tail bits are also output on the RSC1 Systematic output. This avoids the need for you to connect the RSC2_SYSTEMATIC port.

Clocking

See Clock (CLK).

Resets

See Data In (DATA_IN).

Functional Description

Double-Buffering

Figure 3-2 illustrates the LOAD and OUTPUT operations.

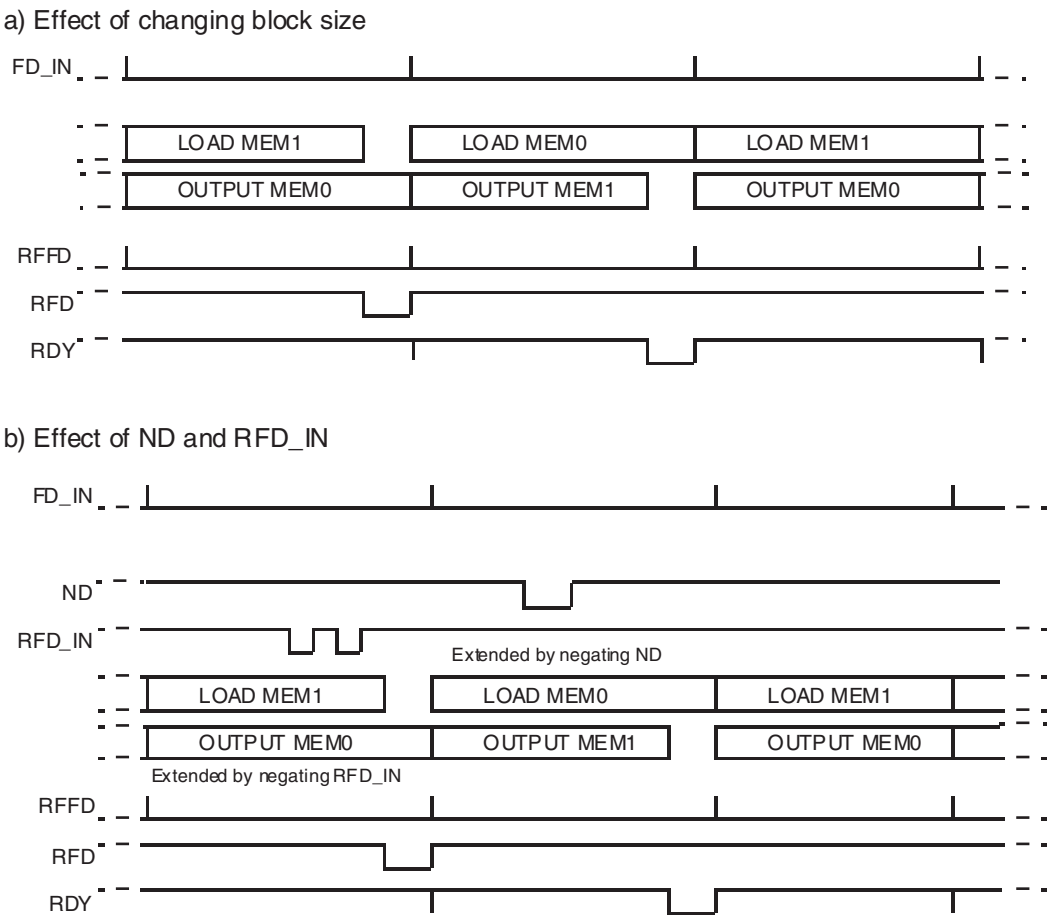


Figure 3-2: **Double-Buffered Mode Data Throughput**

Data blocks are written alternately to the two symbol memories, MEM0 and MEM1, and also read out alternately, thereby maximizing the data throughput.

If the block size increases, or the core is inhibited by negating ND, the LOAD operation might take longer than the OUTPUT operation, in which case the RDY output port can be driven low to indicate the OUTPUT operation is complete. Similarly, If the block size decreases, or the core is inhibited by negating RFD_IN, the OUTPUT operation might take longer than the LOAD operation, in which case the RFD port can be driven low to indicate that the LOAD operation is complete, and the core is no longer ready for data. The effect of changing the block size is shown in Figure 3-2(a), and the effects of ND and RFD_IN are shown in Figure 3-2(b).

Due to pruning (omitted addresses) in the internal interleaver, RDY goes Low for a few cycles between blocks; however, when an OUTPUT operation has started, RDY only goes Low again after the last tail bit has been output.

Input Control Signals

Figure 3-3 shows the signals associated with the data input side of the core. If, on an active rising edge of CLK, FD_IN and ND (if selected) are both sampled High, this is known as a valid-FD, or valid First Data signal.

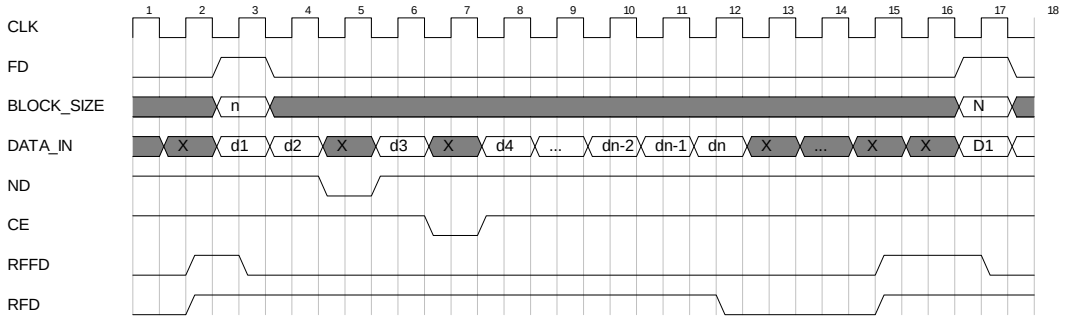


Figure 3-3: **Input Timing**

When a valid-FD is sampled, the RFFD signal is driven Low to indicate that the core is no longer waiting for FD_IN. The block size, in this case *n*, of the current input block is sampled on the BLOCK SIZE port, and the first data symbol, *d1*, is sampled on the DATA_IN port.

A High on the ND port indicates that the value on the DATA_IN port is new data. If ND is sampled Low, then the DATA IN port is not sampled, and the internal write address does not advance.

The core continues to input data, until *n* new data samples have been accepted, whereupon RFD (if selected) is normally driven Low to indicate that the core is no longer ready for data, and the core stops sampling the DATA_IN port.

When the core is ready to accept a new block of data, RFFD and RFD are both driven High. The time at which this occurs is determined by how long it takes the core to output the current output block, and this depends on its block size, and on whether or not the output side of the core is inhibited by negating RFD_IN. If the input operation completes and the output cycle is already complete, it is possible for RFFD to be asserted, and a new input cycle to be started without RFD going Low.

After asserting RFFD, the core waits until the next valid-FD is sampled, whereupon a write cycle is started, in this case, with block size *N*.

The behavior of the core is not specified if, on a valid-FD, an invalid block size is sampled, or RFFD is sampled Low (core not ready for a new block). If either of these conditions occurs, the core must be reset by asserting SCLR.

Trellis Termination

When the Multiplex Trellis Termination Bits option is selected, as is the case for 3GPP systems, the trellis termination bits of RSC1 and RSC2 are remultiplexed, over four clock cycles, onto the RSC1_SYSTEMATIC, RSC1_PARITY0 and RSC2_PARITY0 output ports. These bits are then transmitted in the following sequence:

```
xn+1, zn+1, xn+2, zn+2, xn+3, zn+3, x'n+1, z'n+1, x'n+2, z'n+2, x'n+3, z'n+3.
```

When the Multiplexed Tail Bits option is not selected, the RSC2 tail bit data is switched to the RSC1_SYSTEMATIC output and, therefore, overrides the RSC1_SYSTEMATIC values. Typically, the parallel output of the systematic and parity bits from each encoder are serialized before transmission. Also, in general, the RSC2_SYSTEMATIC data is only transmitted during the tail bit period, so by multiplexing the RSC2_SYSTEMATIC data onto the RSC1_SYSTEMATIC port, there is no need to output RSC2_SYSTEMATIC.

Output Control Signals

The RDY signal is driven High to indicate that there is valid data on the systematic and parity ports. In addition, the RSC1_TAIL and RSC2_TAIL outputs are provided to indicate trellis termination of RSC1 and RSC2, respectively. A High on RSC1_TAIL indicates that RSC1 tail bits are being output, and a High on RSC2_TAIL indicates that RSC2 tail bits are being output. The output timing for 3GPP compliant multiplexed tail bits is shown in Figure 3-4. Output timing for optional parallel output of tail bits is shown in Figure 3-5.

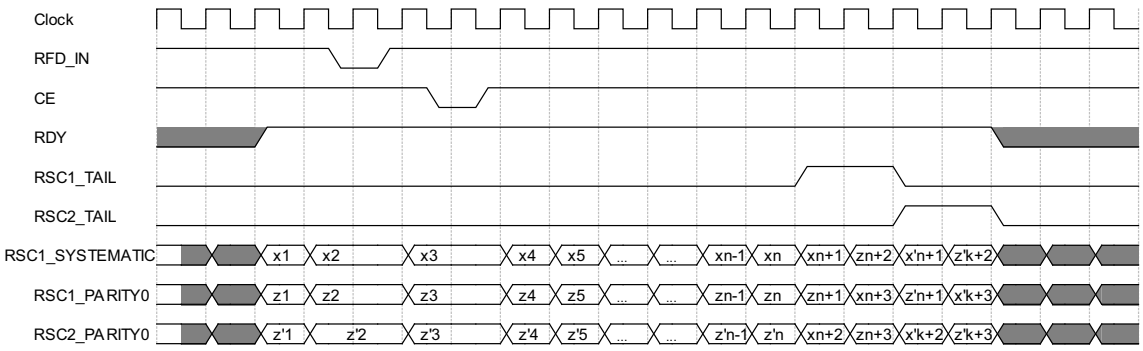
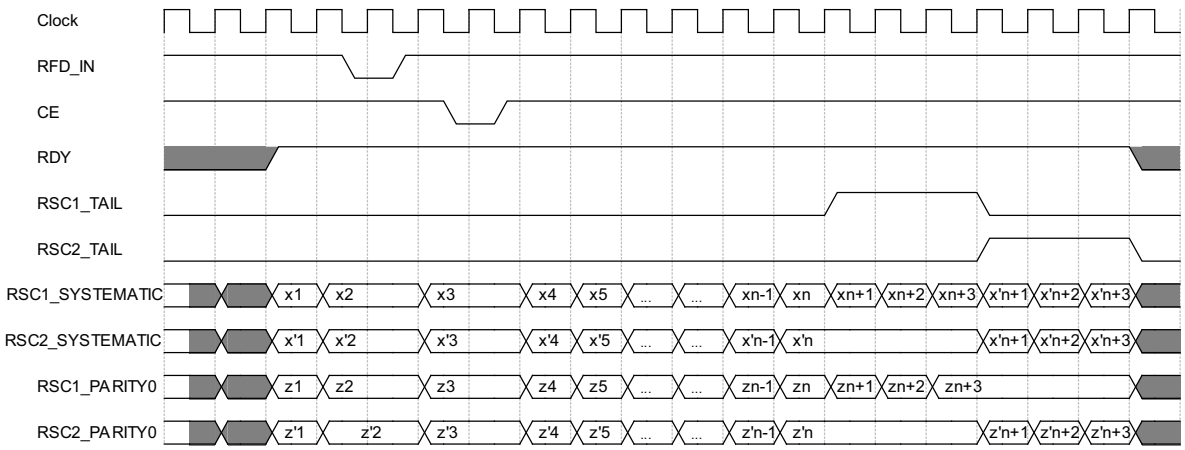


Figure 3-4: **Output Timing (Multiplexed Tail Bits)**



x1...xn are the uninterleaved input bits, delayed, for block size n
x'1...x'n are the interleaved input bits
z1...zn+3 are the RSC1 Parity0 output bits
z'1...z'n+3 are the RSC2 Parity0 output bits

Figure 3-5: **Output Timing (Non-Multiplexed Tail Bits)**

Flow control on the output side can be implemented with the optional RFD_IN input port. If the RFD_IN port is sampled Low on an active rising clock edge, the RSC output ports, RDY, and the internal circuitry associated with these outputs are frozen.

The input side of the core is not directly affected by the RFD_IN port. However, if RFD_IN is deasserted often enough, the time taken to output a block can be extended such that the assertion of RFFD is delayed, which acts to prevent overrun on the input side.

If rate 1/5 is selected, the RSC1_PARITY1 and RSC2_PARITY1 outputs are enabled. These have the same timing as RSC1_PARITY0 and RSC2_PARITY0, respectively.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 6]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 7]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 4] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl Console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 6].

Component Name: The name of the core component to be instantiated. The name must begin with a letter and be composed of the following characters: a to z, A to Z, 0 to 9 and '_'.

Encoder Options Tab

Trellis Termination

When the Multiplex Trellis Termination Bits option is selected, as is the case for 3GPP systems, the trellis termination bits of RSC1 and RSC2 are remultiplexed, over four clock cycles, onto the RSC1_SYSTEMATIC, RSC1_PARITY0 and RSC2_PARITY0 output ports. (See Trellis Termination for more information).

Encoder Options

Number of Channels: Sets the number of supported data channels; for information on when more than one channel is selected see Multichannel Operation.

Coding Rate: Is automatically set the 1/3 (3GPP standard) when the Multiplex Trellis Termination Bits option is checked. When set to 1/5, no specific trellis multiplexing is performed.

Memory Options

External RAM: Checking this option allows you to connect external RAM to the core for data storage. The I/O ports for the external RAM option are described in External RAM Option. Data is stored internally when this option is not checked.

Address Generator Options

Address Generator: Set to Internal to use the 3GPP standard for the interleaving function. To use a different interleaving function, set to External and provide the interleaving sequence as described in External Address Generator Option.

Address Width: If Address Generator is set to External you can define the length of the interleaving sequence using this field. See External Address Generator Option for more information.

Optional Pins Tab

New Data (ND)

The optional ND signal is used to indicate that there is new input data to be read from the DATA_IN port. For example, if the input block size is 100, then 100 active-High *ND-samples* are required to load a block of data into the encoder. ND is also used to qualify the FD_IN input. See First Data (FD_IN).

Clock Enable (CE)

Clock enable is an optional input pin that is used to enable the synchronous operation of the core. When CE is High, a rising edge of CLK is acted upon by the core, but if CE is Low, the core remains in its current state. An active rising clock edge is on one which CE (if enabled) is sampled High.

Synchronous Clear (SCLR)

The SCLR signal is optional. When it is asserted High on a valid clock edge, the core is reset to its initial state, that is., the core is ready to process a new block. Following the initial configuration of the FPGA, the core is automatically in the reset state, so no further SCLR is required before an encoding operation can take place. If the CE input port is selected, SCLR is ignored if CE is Low.

Ready For Data In (RFD_IN)

RFD_IN is an optional pin which can be used to inhibit the output of the core while allowing current input operations to continue. RFD_IN is intended to be used as a means for a downstream system using the encoded data to indicate that it is not ready to handle any further data. If RFD_IN is Low, all systematic and parity outputs, RSC1_TAIL, RSC2_TAIL, and RDY outputs are inhibited. The operation of RFD_IN is described in further detail later in this document.

Ready For Data (RFD)

When this optional pin is asserted High, it indicates that the core is ready to accept new input data. If RFD is selected, then it is High during the period that a particular block is input. When *block size* samples of data have been input, the RFD signal goes Low to indicate that the core is no longer ready to accept data.

Block Size Valid

Indicates that the block size which was sampled on the BLOCK_SIZE port on the last valid-FD is a valid 3GPP block size in the range 40 through 5114. The BLOCK_SIZE_VALID port is not available if the external address generator option is selected.

User Parameters

Table 4-1 shows the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console).

All parameters are visible in the IP integrator. No parameters are set automatically.

Table 4-1: **Vivado IDE Parameter to User Parameter Relationship**

Vivado IDE Parameter	User Parameter	Default Value
Number of channels	number_of_channels	1
Multiplex Trellis Termination Bits	multiplex_tail_bits	True
Coding Rate	coding_rate	1/3
External Ram	external_ram	False
Address Generator	address_generator	Internal
Address Width	address_width	13
BLOCK SIZE VALID	block_size_valid	False
ND	nd	False
RFD	rfd	False
RFD IN	rfd_in	False
CE	ce	False
SCLR	sclr	False

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 7].

IMPORTANT: *For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 5].

Upgrading

This appendix contains information about upgrading to a more recent version of the IP core.

Migrating to the Vivado Design Suite

For information about migrating to the Vivado Design Suite, *see the ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 8].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade to a more current version of this IP core in the Vivado Design Suite.

Parameter Changes

No changes.

Port Changes

No changes.

Other Changes

No changes.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

TIP: *If the IP generation halts with an error, there might be a license issue. See License Checkers in Chapter 1 for more details.*

Finding Help on Xilinx.com

To help in the design and debug process when using the 3GPP Turbo Encoder, the Xilinx Support web page (Xilinx Support web page) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the 3GPP Turbo Encoder. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords, such as:

- Product name
- Tool messages
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the 3GPP Turbo Encoder

AR: 54472

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address 3GPP Turbo Encoder design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 9].

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. 3G TS.25.222 V5.5.0 (2003-06), Multiplexing and Channel Coding (TDD), Technical Specification Group Radio Access Network, 3rd Generation Partnership Project.
2. 3G TS.25.212 V6.0.0 (2003-12), Multiplexing and Channel Coding (FDD), Technical Specification Group Radio Access Network, 3rd Generation Partnership Project.
3. Near Shannon Limit Error-correcting Coding and Decoding Turbo Codes, C. Berrou, A. Glavieux, and P. Thitimajshima, IEEE Proc 1993 Int Conf. Comm., pp1064-1070.
4. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
5. *Vivado Design Suite User Guide: Designing with IP* (UG896)
6. *Vivado Design Suite User Guide: Getting Started* (UG910)
7. *Vivado Design Suite User Guide - Logic Simulation* (UG900)
8. *ISE® to Vivado Design Suite Migration Guide* (UG911)
9. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
10. *Vivado Design Suite User Guide: Implementation* (UG904)
11. *Vivado Design Suite User Guide: Designing with IP* (UG896)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/04/2021	5.0	• Added Versal ACAP support.
11/18/2015	5.0	• Added support for UltraScale+ families. • Updated link to resource utilization data.
04/02/2014	5.0	• Added link to resource utilization figures • Updated template
12/18/2013	5.0	• Revision number advanced to 5.0 to align with core version number. • Added UltraScale™ architecture support. • Template updated.
03/20/2013	1.0	• Initial release as a product guide. Replaces *LogiCORE IP 3GPP Turbo Encoder Data Sheet* (DS319).

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