LogiCORE IP Tri-Mode Ethernet MAC v4.5

DS297 March 1, 2011

Product Specification

Introduction

The LogiCORE™ IP Tri-Mode Ethernet Media Access Controller (TEMAC) solution comprises the 10/100/1000 Mb/s Ethernet MAC, 1 Gb/s Ethernet MAC and the 10/100 Mb/s Ethernet MAC IP core. All cores support half-duplex and full-duplex operation.

Features

- Designed to the *IEEE 802.3-2008* specification
- Configurable half-duplex and full-duplex operation
- Optional support for full-duplex only
- Supports 10/100 Mb/s only, 1 Gb/s only or full 10/100/1000 Mb/s IP Cores
- Internal GMII physical-side (PHY) that can be connected to
  - LogiCORE IP Ethernet 1000BASE-X PCS/PMA using transceiver
  - LogiCORE IP Ethernet SGMII
  - IOBs to provide an external GMII/MII [5]
  - A shim to provide an external RGMII [2]
- Configured and monitored through an optional independent microprocessor-neutral interface
- Configurable flow control through MAC Control pause frames
- Optional MDIO interface to managed objects in PHY layers (MII Management)
- Optional Address Filter with selectable number of address table entries
- Support of VLAN frames designed to *IEEE 802.3-2008*
- Configurable support of jumbo frames of any length
- Configurable interframe gap adjustment

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]	Virtex-6, Virtex-5, Virtex-4, Spartan-6, Spartan-3, Spartan-3E[2] Spartan-3A/3AN/3A DSP				
Supported User Interfaces	LocalLink (using supplied example design FIFO) Host				
Performance	10 Mb/s, 100 Mb/s, 1 Gb/s[3]				
Core Highlights					
Designed to IEEE specification 802.3-2008				Hardware Verified	
Resources[4]					
Configuration	**Slices**	**LUTs**	**FFs**	**DCM**	**BUFG**
	445-1850	700-2080	815-1510	0-2	2-6
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	NGC Netlist				
Example Design	Tri-Mode Ethernet MAC with MII, GMII/MII[5] or RGMII interface				
Test Bench	Demonstration Test Bench, Scripts				
Constraints File	User Constraints File (UCF)				
Simulation Model	VHDL or Verilog				
Tested Design Tools					
Design Entry Tools	ISE® software v13.1				
Simulation	Mentor Graphics ModelSim v6.6d Cadence Incisive Enterprise Simulator (IES) v10.2 Synopsys VCS and VCS MX 2010.06[6]				
Synthesis Tools	XST 13.1				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.
   Virtex-6 and Virtex-5 devices: -1 speed grade;
   Virtex-4 devices: -10 speed grade;
   Spartan-6 devices: -2 speed grade;
   All other listed Spartan devices support speed grade -4
2. Spartan-3E devices support only the MII or GMII protocols.
3. Performance is subject to device support. See Performance, page 21.
4. See Tables 22 to 25; precise number depends on user configuration and family.
5. Virtex-6 devices support GMII and MII at 2.5V only; see the Virtex-6 FPGA Data Sheet: DC and Switching Characteristics for more information. Virtex-5, Virtex-4, Spartan-6 and Spartan-3 devices support MII and GMII at 3.3V or lower.
6. Scripts provided for listed simulators only.

Features (Continued)

- Configurable in-band FCS field passing on both transmit and receive paths
- Available under the terms of the SignOnce IP Site License agreement

Applications

Typical applications for the TEMAC solution include the following: [6]

- Ethernet 1000BASE-X Port
- Ethernet Tri-Speed BASE-T Port (MII/GMII or RGMII)
- Ethernet Tri-Speed BASE-T Port (SGMII)

Ethernet 1000BASE-X Port

Figure 1 illustrates a typical 1 Gb/s MAC application. The TEMAC solution can be generated with both 1 Gb/s only and full-duplex only to remove unnecessary logic. The PHY side of the core is connected to internally integrated serial transceivers, available in certain families, to connect to an external off-the-shelf GBIC or SFP optical transceiver. The 1000BASE-X logic can be provided by the Ethernet 1000BASE-X PCS/PMA or SGMII core.

The client side of the core is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO, delivered with the TEMAC solution to complete a single Ethernet port. This port is shown connected to a Switch or Routing matrix, which can contain several ports.

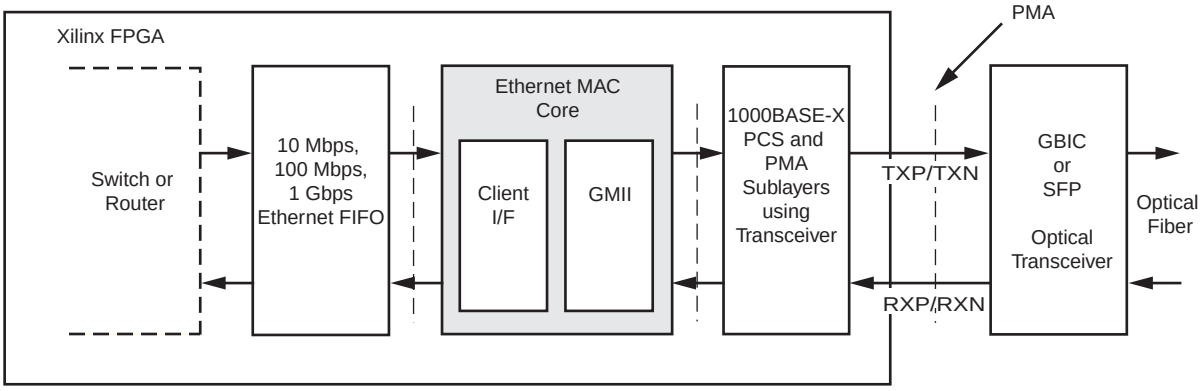

Figure 1: **Typical MAC 1000BASE-X Application**

Ethernet Tri-Speed BASE-T Port (MII/GMII or RGMII)

Figure 2 illustrates a typical application for the TEMAC (10/100/1000 Mb/s) core. The PHY side of the core is implementing an external GMII/MII by connecting it to IOBs. The external GMII/MII is connected to an off-the-shelf Ethernet PHY device, which performs the BASE-T standard at 1 Gb/s, 100 Mb/s, and 10 Mb/s speeds. Alternatively, the external GMII/MII can be replaced with an RGMII using a small logic shim. HDL example designs are provided with the core to demonstrate external GMII or RGMII.

The client side of the TEMAC is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO (delivered with the example design) to complete a single Ethernet port. This port is shown connected to a Switch or Routing matrix, which can contain several ports.

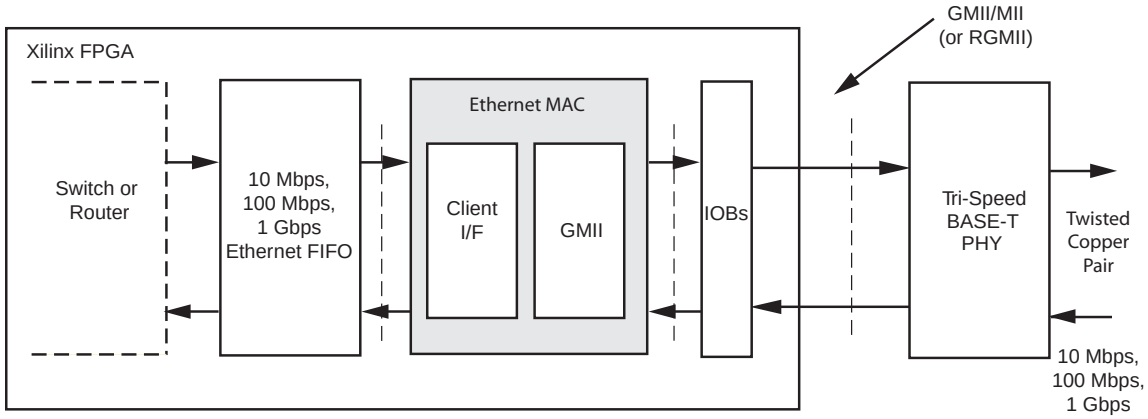

Figure 2: **Typical BASE-T Application for TEMAC Core: MII/GMII/RGMII**

Ethernet Tri-Speed BASE-T Port (SGMII)

Figure 3 illustrates a typical application for the TEMAC(10/100/1000 Mb/s) core. The PHY side of the core is connected to internally integrated SGMII logic using the device-specific transceiver to connect to an off-the-shelf Ethernet PHY device, which performs the BASE-T standard at 1 Gb/s, 100 Mb/s, and 10 Mb/s speeds. The SGMII logic can be provided by the Ethernet 1000BASE-X PCS/PMA or SGMII core using transceivers. See the Ethernet 1000BASE-X PCS/PMA or SGMII user guide for more information.

The client side of the core is shown connected to the 10 Mb/s, 100 Mb/s, 1 Gb/s Ethernet FIFO, delivered with the TEMAC core, to complete a single Ethernet port. This port is shown connected to a Switch or Routing matrix, which can contain several ports.

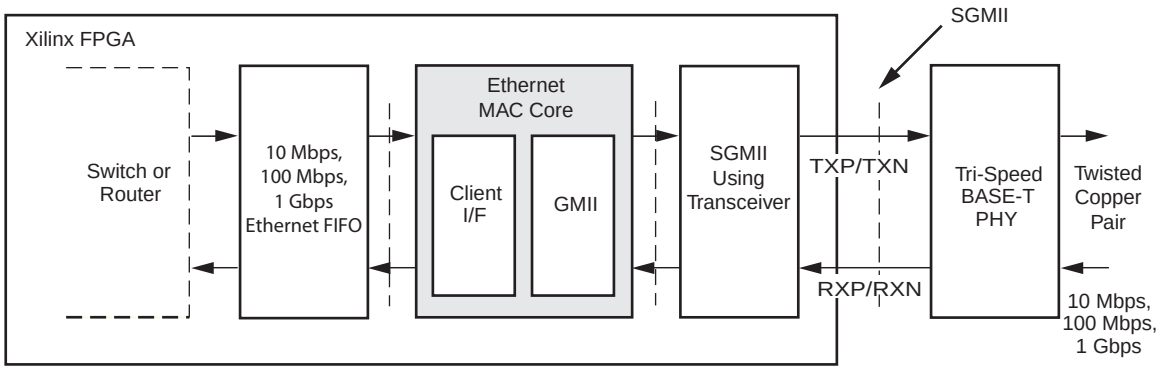

Figure 3: **Typical BASE-T Application for TEMAC Core: SGMII**

Ethernet Architecture Overview

The MAC sublayer provided by this core is part of the Ethernet architecture displayed in Figure 4. The portion of the architecture, from the MAC to the right, is defined in *IEEE 802.3*. This figure also illustrates where the supported interfaces fit into the architecture.

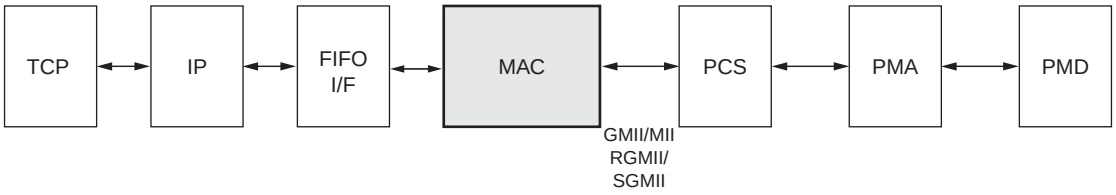

Figure 4: **Typical Ethernet Architecture**

MAC

The Ethernet Medium Access Controller (MAC) is defined in *IEEE 802.3-2008* clauses 2, 3, and 4. A MAC is responsible for the Ethernet framing protocols and error detection of these frames. The MAC is independent of, and can be connected to, any type of physical layer.

GMII / MII

The Gigabit Media Independent Interface (GMII) is defined in *IEEE 802.3-2008* clause 35. At 10 Mb/s and 100 Mb/s, the Media Independent Interface (MII) is used as defined in *IEEE 802.3-2008* clause 22. These are parallel interfaces connecting a MAC to the physical sublayers (PCS, PMA, and PMD).

RGMII

The Reduced Gigabit Media Independent Interface (RGMII) is an alternative to the GMII. RGMII achieves a 50-percent reduction in the pin count, compared with GMII, and for this reason is preferred over GMII by PCB designers. This is achieved with the use of double-data-rate (DDR) flip-flops. No change in the operation of the core is required to select between GMII and RGMII. However, the clock management logic and IOB logic around the core will change. HDL example designs are provided with the core which implement either the GMII or RGMII protocols.

SGMII

The Serial-GMII (SGMII) is an alternative interface to the GMII, which converts the parallel interface of the GMII into a serial format, radically reducing the I/O count (and for this reason often favored by PCB designers).

The TEMAC solution can be extended to include SGMII functionality by internally connecting its PHY side GMII to the Ethernet 1000BASE-X PCS/PMA or SGMII core from Xilinx. See the *Tri-Mode Ethernet MAC User Guide*.

PCS, PMA, and PMD

The combination of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) sublayer comprise the physical layers of the Ethernet protocol.

Two main physical standards are specified for Ethernet:

- BASE-T, a copper standard using twisted pair cabling systems
- BASE-X, usually a fibre optical physical standard using short and long wavelength laser

BASE-T devices, supporting 10 Mb/s, 100 Mb/s, and 1 Gb/s Ethernet speeds, are readily available as off-the-shelf parts. As illustrated in Figure 2, these can be connected using GMII/MII, RGMII, or SGMII to provide a tri-speed Ethernet port.

The 1000BASE-X architecture illustrated in Figure 1 can be provided by connecting the TEMAC core to the Ethernet 1000BASE-X PCS/PMA or SGMII core.

Core Overview

Figure 5 identifies the major functional blocks of the TEMAC solution. Descriptions of the functional blocks and interfaces are provided in the subsequent sections.

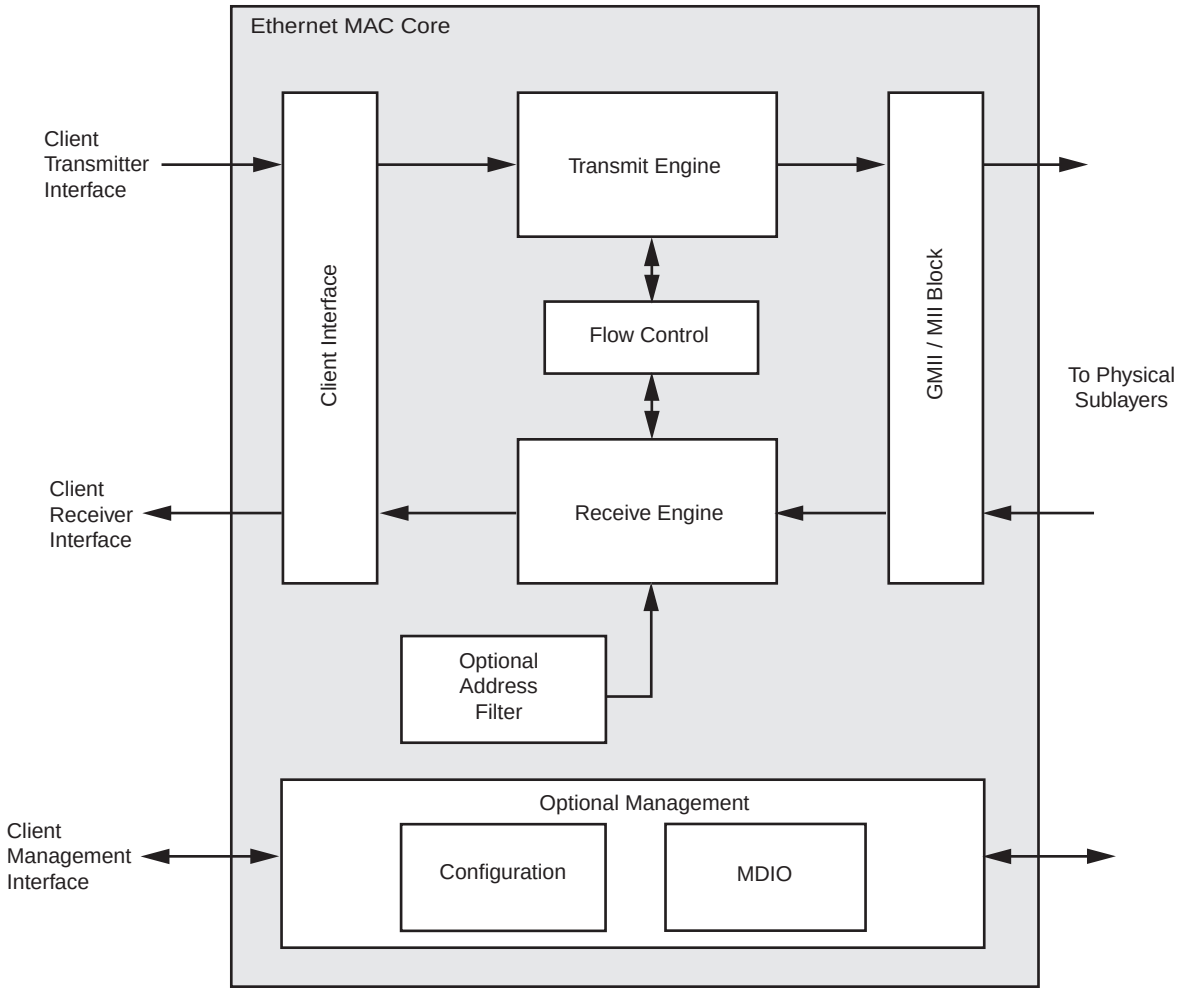

Figure 5: **TEMAC Functional Block Diagram**

Client Interface

The client interface is designed for maximum flexibility in matching to a client switching logic or network processor interface. The data pathway is 8-bits wide in both the transmit and receive directions. Each pathway is synchronous to `txgmiimiiclk` and `rxgmiimiiclk` respectively with transmit and receive enable inputs being driven to control the data throughput.

Transmit Engine

The transmit engine takes data from the client and converts it to GMII format. Preamble and frame check sequence fields are added and the data is padded if necessary. The transmit engine also provides the transmit statistics vector for each packet and transmits the pause frames generated by the flow control module.

Receive Engine

The receive engine takes the data from the GMII/MII interface and checks it for compliance to the *IEEE 802.3*. Padding fields are removed and the client is presented with the data along with a good or bad frame indicator. The receive engine also provides the receive statistics vector for each received packet.

Flow Control

The flow control block is designed to *IEEE 802.3-2008* clause 31. The MAC can be configured to send pause frames with a programmable pause value and to act on their reception. These two behaviors can be configured asymmetrically.

GMII/MII Block

The GMII/MII interface takes the data from the transmitter and converts it to MII format if the device is operating at speeds under 1 Gb/s. The received data is converted into GMII format. At 1 Gb/s, the data is passed through.

Management Interface

The optional Management Interface is a processor-independent interface with standard address, data, and control signals. It is used for the configuration and monitoring of the MAC and for access to the MDIO Interface. It can be used as is or a wrapper can be applied (not supplied) to interface to common bus architectures. This interface is optional. If it is not present, the device can be configured using a configuration vector.

MDIO Interface

The optional MDIO interface can be written to and read from using the Management Interface. The MDIO is used to monitor and configure PHY devices. The MDIO Interface is defined in *IEEE 802.3* clause 22.

Address Filter

The TEMAC solution can be implemented with an optional address filter. If the address filter is enabled, the device does not pass frames that do not contain one of a set of known addresses to the client.

Interface Descriptions

All ports of the core are internal connections in the FPGA logic. An example HDL design, provided in both VHDL and Verilog, is delivered with each core. The example design connects the core to a FIFO-based loopback example design and adds IOB flip-flops to the external signals of the GMII/MII (or RGMII).

All clock management logic is placed in this example design, allowing you more flexibility in implementation (for example, in designs using multiple cores). For information about the example design, see the *Tri-Mode Ethernet MAC User Guide*.

Transmitter Client Side Interface

Signal Definition

Table 1 defines the client-side transmit signals of the core, which are used to transmit data from the client to the core.

Table 1: **Transmit Client Interface Signal Pins (With Optional Clock Enables)**

Signal	Direction	Clock Domain	Description
clientemactxd[7:0]	Input	txgmiimiiclk	Frame data to be transmitted.
clientemactxdvld	Input	txgmiimiiclk	Control signal for clientemactxd port.
clientemactxenable	Input	txgmiimiiclk	Transmitter clock enable signal. This signal is present when: The TEMAC solution is generated for 10/100 Mb/s only ethernet speed support. The TEMAC solution is generated for tri-speed ethernet support when using the optional clock enables.
clientemactxifgdelay[7:0]	Input	txgmiimiiclk	Control signal for configurable interframe gap adjustment.
emacclienttxack	Output	txgmiimiiclk	Handshaking signal. Asserted when the current data on clientemactxd has been accepted.
clientemactxunderrun	Input	txgmiimiiclk	Asserted by client to force MAC core to corrupt the current frame.
emacclienttxcollision	Output	txgmiimiiclk	Asserted by the MAC core to signal a collision on the medium and that any transmission in progress should be aborted. Always 0 when the MAC core is in full-duplex mode.
emacclienttxretransmit	Output	txgmiimiiclk	When asserted at the same time as the emacclienttxcollision signal, this signals to the client that the aborted frame should be resupplied to the MAC core for retransmission. Always '0' when the MAC core is in full-duplex mode.
emacclienttxstats[31:0]	Output	txgmiimiiclk	A statistics vector that gives information on the last frame transmitted.
emacclienttxstatsvld	Output	txgmiimiiclk	Asserted at end of frame transmission, indicating that the emacclienttxstats is valid.

Note: All signals are active high.

Transmitter Client Interface Timing

Figure 6 displays a typical frame transmission at the client interface. All signals are synchronous to the `txgmiimiiclk` clock (not shown). The vertical dotted lines represent either a rising edge of the `txgmiimiiclk` clock (when clock enables are not in use), or a clock-enabled cycle (when clock enables are in use). If used, `clientemactxenable` is the clock enable signal. See the User Guide for further information.

To transmit a frame the client asserts `clientemactxdvld` and puts the first byte of frame data on the `clientemactxd` bus. The client then waits until the core asserts `emacclienttxack` before sending the rest of the data. At the end of the frame, `clientemactxdvld` is deasserted.

At 1 Gb/s, each clock-enabled cycle is 8 ns apart; at 100 Mb/s, each clock-enabled cycle is 80 ns apart; at 10 Mb/s, each clock-enabled cycle is 800 ns apart.

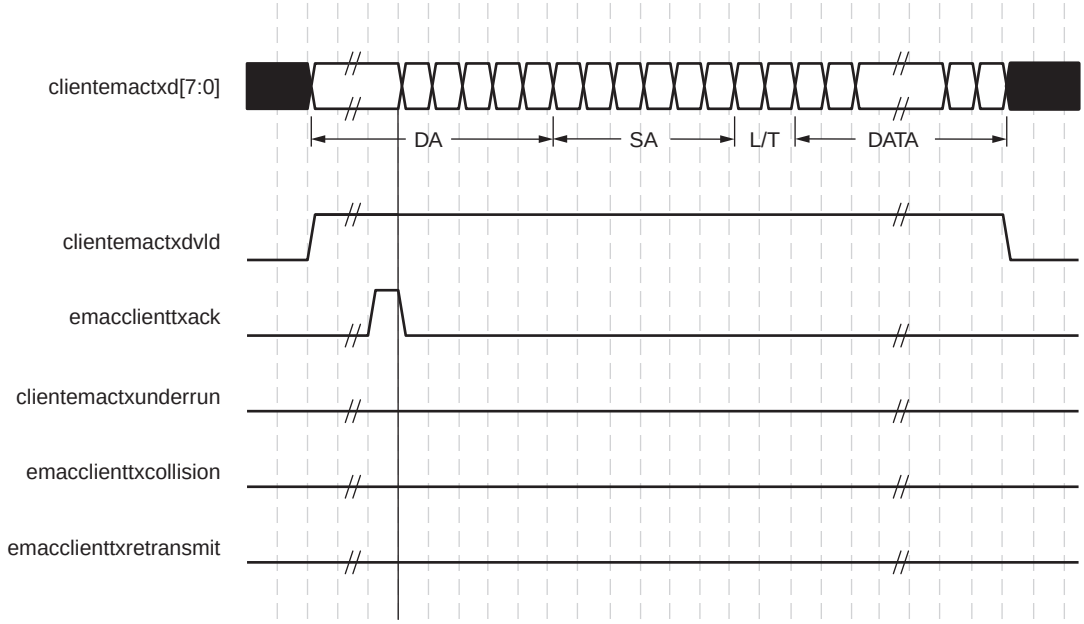

Figure 6: **Normal Frame Transmission across Client interface**

Receiver Client Side Interface

Signal Definition

Table 2 describes the client-side receive signals used by the core to transfer data to the client.

Table 2: **Receive Client Interface Signal Pins**

Signal	Direction	Clock Domain	Description
emacclientrxd[7:0]	Output	rxgmiimiiclk	Frame data received is supplied on this port.
emacclientrxdvld	Output	rxgmiimiiclk	Control signal for the emacclientrxd port.
clientemacrxenable	Input	rxgmiimiiclk	Receiver clock enable signal. This signal is present when: The TEMAC solution is generated for 10/100 Mb/s only ethernet speed support. The TEMAC solution is generated for tri-speed ethernet support when using the optional clock enables.
emacclientrxgoodframe	Output	rxgmiimiiclk	Asserted at end of frame reception to indicate that the frame should be processed by the MAC client.
emacclientrxbadframe	Output	rxgmiimiiclk	Asserted at end of frame reception to indicate that the frame should be discarded by the MAC client.
emacclientrxstats[27:0]	Output	rxgmiimiiclk	Provides information about the last frame received.
emacclientrxstatsvld	Output	rxgmiimiiclk	Asserted at end of frame reception, indicating that the emacclientrxstats is valid.

Note: All signals are active high.

Receiver Client Interface Timing

Figure 7 displays the reception of a good frame at the client interface. All signals are synchronous to the `rxgmiimiiclk` clock (not shown). The vertical dotted lines represent either a single clock period of the `rxgmiimiiclk` clock (when clock enables are not in use), or a clock-enabled cycle (when clock enables are in use). If used, `clientemacrxenable` is the clock enable signal. See the User Guide for further information.

When receiving a frame, the core asserts `emacclientdvld` for the duration of the frame data. At the end of the frame, the `emacclientrxgoodframe` signal is asserted to indicate that the frame passed all error checks.

At 1 Gb/s, each clock-enabled cycle is 8 ns apart; at 100 Mb/s, each clock-enabled cycle is 80 ns apart; at 10 Mb/s, each clock-enabled cycle is 800 ns apart.

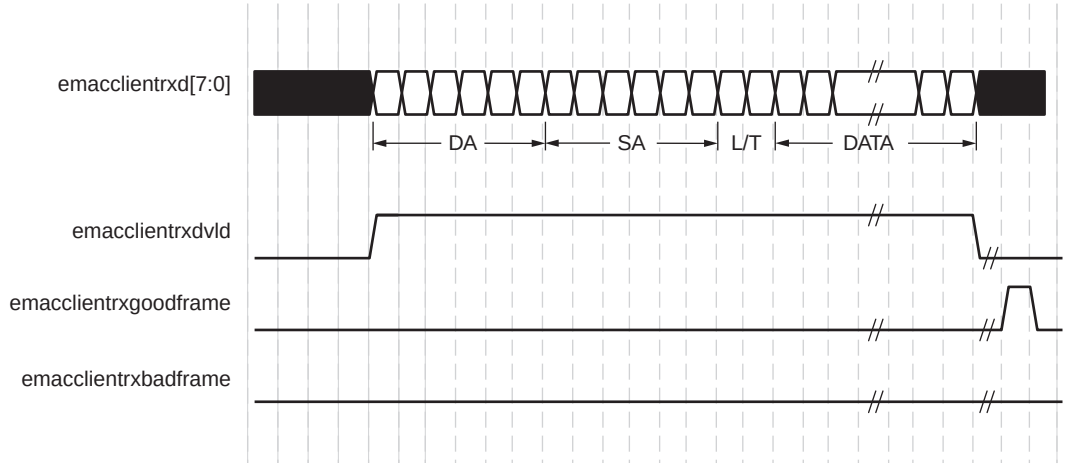

Figure 7: **Normal Frame Reception at Client Interface**

Flow Control Client Side Interface Signal Definition

Table 3 describes the signals used by the client to request a flow-control action from the transmit engine. Valid flow control frames received by the MAC are automatically handled (if the MAC is configured to do so). The pause value in the received frame is used to inhibit the transmitter operation for the time defined in *IEEE 802.3-2008*. The frame is then passed to the client with `emacclientrxbadframe` asserted to indicate to the client that it should be dropped.

Table 3: **Flow Control Interface Signal Pinout**

Signal	Direction	Description
clientemacpausereq	Input	Pause request: Upon request the MAC transmits a pause frame upon the completion of the current data packet.
clientemacpauseval[15:0]	Input	Pause value: inserted into the parameter field of the transmitted pause frame.

Note: All signals are active high.

Management Interface Signal Definition

Table 4 describes the optional signals used by the client to access the management features of the MAC core, including configuration, status and MDIO access.

Table 4: **Optional Management Interface Signal Pinout**

Signal	Direction	Clock Domain	Description
hostclk	Input	N/A	Clock for Management Interface.
hostopcode[1:0]	Input	hostclk	Defines operation to be performed over MDIO interface. Bit 1 is also used in configuration register access.
hostaddr[9:0]	Input	hostclk	Address of register to be accessed.
hostwrdata[31:0]	Input	hostclk	Data to write to register.
hostrddata[31:0]	Output	hostclk	Data read from register.
hostmiimsel	Input	hostclk	When asserted, the MDIO interface is accessed. When deasserted, the MAC internal configuration is accessed.
hostreq	Input	hostclk	Used to signal a transaction on the MDIO interface or to read from the statistic registers.
hostmiimrdy	Output	hostclk	When high, the MDIO interface has completed any pending transaction and is ready for a new transaction.

Note: All signals are active high.

Configuration Registers

After power up or reset, the client might reconfigure the core parameters from their defaults, such as flow control support. Configuration changes can be written at any time. Both the receiver and transmitter logic only sample configuration changes at the start of frame transmission/reception. The exceptions to this are the configurable resets which take effect immediately.

Configuration of the core is performed through a register bank accessed through the Management Interface. The configuration registers available in the core are detailed in Table 5. As can be seen, the address has some implicit don't care bits; any access to an address in the ranges shown performs a 32-bit read or write from the same configuration word.

Table 5: **Configuration Registers**

Address	Description
0x200-0x23F	Receiver Configuration (Word 0)
0x240-0x27F	Receiver Configuration (Word 1)
0x280-0x2BF	Transmitter Configuration
0x2C0-0x2FF	Flow Control Configuration
0x300-0x31F	MAC Speed Configuration
0x320-0x33F	Reserved
0x340-0x37F	Management Configuration
0x380-0x383	Unicast Address (Word 0) (if address filter is present)
0x384-0x387	Unicast Address (Word 1) (if address filter is present)
0x388-0x38B	Address Table Configuration (Word 0) (if address filter is present)
0x38C-0x38F	Address Table Configuration (Word 1) (if address filter is present)
0x390-0x3BF	Address Filter Mode (if address filter is present)

Configuration Register Definition

Receiver Configuration

The register contents for the two receiver configuration words can be seen in Table 6 and Table 7.

Table 6: **Receiver Configuration Word 0**

Bit	Default Value	Description
31-0	All 0s	**Pause frame MAC Source Address[31:0]** This address is used by the MAC to match against the destination address of any incoming flow control frames. It is also used by the flow control block as the source address (SA) for any outbound flow control frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Address[47:0] as 0xFFEEDDCCBBAA.

Table 7: **Receiver Configuration Word 1**

Bit	Default Value	Description
15-0	All 0s	**Pause frame MAC Source Address[47:32]** See description in Table 6.
23-16	N/A	Reserved
24	0	**Control Frame Length Check Disable** When this bit is set to '1,' the core does not mark control frames as 'bad' if they are greater than the minimum frame length.
25	0	**Length/Type Error Check Disable** When this bit is set to '1,' the core does not perform the length/type field error checks as described in the *Tri-Mode Ethernet MAC User Guide*. When this bit is set to '0,' the length/type field checks is performed: this is normal operation.
26	0	**Half Duplex** If '1,' the receiver operates in half- duplex mode. If '0,' the receiver operates in full- duplex mode.
27	0	**VLAN Enable** When this bit is set to '1,' VLAN tagged frames are accepted by the receiver.
28	1	**Receiver Enable** If set to '1,' the receiver block is operational. If set to '0,' the block ignores activity on the physical interface RX port.
29	0	**In-band FCS Enable** When this bit is '1,' the MAC receiver passes the FCS field up to the client as described in the *Tri-Mode Ethernet MAC User Guide*. When it is '0,' the client is not passed to the FCS. In both cases, the FCS is verified on the frame.
30	0	**Jumbo Frame Enable** When this bit is set to '1,' the MAC receiver accepts frames over the specified *IEEE 802.3-2008* maximum legal length. When this bit is '0,' the MAC only accepts frames up to the specified maximum.
31	0	**Reset** When this bit is set to '1,' the receiver is reset. The bit then automatically reverts to '0.' This reset also sets all of the receiver configuration registers to their default values.

Transmitter Configuration

The register contents for the Transmitter Configuration Word are described in Table 8.

Table 8: **Transmitter Configuration Word**

Bit	Default Value	Description
24-0	N/A	Reserved
25	0	**Interframe Gap Adjust Enable** If '1,' the transmitter reads the value on the port clientemactxifgdelay at the start of frame transmission and adjusts the interframe gap following the frame accordingly (see *Tri-Mode Ethernet MAC User Guide*). If '0,' the transmitter outputs a minimum interframe gap of at least twelve clock cycles, as specified in *IEEE 802.3-2008*.
26	0	**Half Duplex** If '1,' the transmitter operates in half-duplex mode.
27	0	**VLAN Enable** When this bit is set to '1,' the transmitter recognizes the transmission of VLAN tagged frames.
28	1	**Transmit Enable** When this bit is '1,' the transmitter is operational. When it is '0,' the transmitter is disabled.
29	0	**In-band FCS Enable** When this bit is '1,' the MAC transmitter expects the FCS field to be passed in by the client as described in the *Tri-Mode Ethernet MAC User Guide*. When this bit is '0,' the MAC transmitter appends padding as required, computes the FCS and appends it to the frame.
30	0	**Jumbo Frame Enable** When this bit is set to '1,' the MAC transmitter sends frames that are greater than the specified *IEEE 802.3-2008* maximum legal length. When this bit is '0,' the MAC only sends frames up to the specified maximum.
31	0	**Reset** When this bit is set to '1,' the transmitter is reset. The bit then automatically reverts to '0.' This reset also sets all of the transmitter configuration registers to their default values.

Flow Control Configuration

The register contents for the Flow Control Configuration Word are described in Table 9.

Table 9: **Flow Control Configuration Word**

Bit	Default Value	Description
28-0	N/A	Reserved
29	1	**Flow Control Enable (RX)** When this bit is '1,' received flow control frames inhibits the transmitter operation as described in the *Tri-Mode Ethernet MAC User Guide*. When this bit is '0,' received flow control frames are always passed up to the client.
30	1	**Flow Control Enable (TX)** When this bit is '1,' asserting the `clientemacpausereq` signal sends a flow control frame out from the transmitter as described in the *Tri-Mode Ethernet MAC User Guide*. When this bit is '0,' asserting the clientemacpausereq signal has no effect.
31	N/A	Reserved

MDIO Configuration

The register contents for the MDIO Configuration Word are described in Table 10.

Table 10: **MDIO Configuration Word**

Bits	Default Value	Description
5-0	All 0s	**Clock Divide[5:0]** See *Tri-Mode Ethernet MAC User Guide*.
6	0	**MDIO Enable** When this bit is '1,' the MDIO interface can be used to access attached PHY devices. When this bit is '0,' the MDIO interface is disabled and the MDIO signals remain inactive. A write to this bit only takes effect if Clock Divide is set to a non-zero value.
31-7	N/A	Reserved

TEMAC Operational Speed Configuration

The register contents for the MAC Speed Configuration Word, when the TEMAC solution has been generated with tri-speed support, are described in Table 11.

When the TEMAC solution has been generated for only 1 Gb/s speed support, bits 31-30 are hard-coded to the value "10".

When the TEMAC solution has been generated for only 10 Mb/s and 100 Mb/s speed support, bits 31-30 only accept the values of "00" to configure for 10 Mb/s operation, or "01" to configure for 100 Mb/s operation.

Table 11: **MAC Speed Configuration Word**

Bits	Default Value	Description
29-0	N/A	Reserved
31-30	"10"	MAC Speed Configuration "00" - 10 Mb/s "01" - 100 Mb/s "10" - 1 Gb/s

Note: The setting of the MAC Speed Configuration register is not affected by a reset.

Address Filter Configuration

Table 12 through Table 16 describe the registers used to access the optional Address Filter configuration when the TEMAC solution is implemented with an Address Filter. If no address filter is present, these registers will not exist and will return 0s for a read from the stated addresses.

Unicast Address Configuration

The register contents for the two unicast address registers are described in Table 12 and Table 13.

Table 12: **Unicast Address (Word 0)**

Bits	Default Value	Description
31-0	tieemacunicastaddr[31-0]	Address filter unicast address[31:0]. This address is used by the MAC to match against the destination address of any incoming frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Address[47:0] as 0xFFEEDDCCBBAA.

Table 13: **Unicast Address (Word 1)**

Bits	Default Value	Description
15-0	tieemacunicastaddr[47 downto 32]	Address filter unicast address[47:32]. See description in Table 12.
31-16	N/A	Reserved

Optional Address Table

In addition to the unicast address, broadcast address and pause addresses, the address filter can optionally be generated to respond to up to four additional separate addresses. These are stored in an address table within the address filter. See *Tri-Mode Ethernet MAC User Guide*. Table 14 and Table 15 show how the contents of the table are set.

If the TEMAC solution is generated without Address Table functionality then the following registers will not exist and will return 0s for a read from the stated addresses.

Table 14: **Address Table Configuration (Word 0)**

Bits	Default Value	Description
31-0	All 0s	**MAC Address[31:0].** The lower 31 bits of MAC address that is to be written to the address table. The MAC address is ordered so that the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Address[47:0] as 0xFFEEDDCCBBAA.

Table 15: **Address Table Configuration (Word 1)**

Bits	Default Value	Description
15-0	All 0s	**MAC Address[47:32]**. The upper 16 bits of MAC address: see the description in Table 14.
17-16	All 0s	The location in the address table that the MAC address is to be written to or read from. There are up to 4 entries in the table (Location 0 to 3).
22-18	N/A	Reserved
23	0	**Read not write** This bit is set to '1' to read from the address table. If it is set to '1,' the contents of the table entry that is being accessed by bits 17-16 is output on the hostrddata bus in consecutive cycles (Least Significant Word first). If it is set to '0,' the data on bits 15-0 is written into the table at the address specified by bits 17-16.
31-24	N/A	Reserved

The contents of the address table mode register are described in Table 16.

Table 16: **Address Filter Mode**

Bits	Default Value	Description
31	1	**Promiscuous Mode** If this bit is set to '1,' the address filter is set to operate in promiscuous mode. All frames are passed to the receiver client regardless of the destination address.
30-0	N/A	Reserved

Configuration Vector Signal Definition

Table 17 describes the configuration vector, which uses direct inputs to the core to replace the functionality of the MAC configuration bits when the Management Interface is not used. The configuration settings described in Tables 6 through 9, Tables 11 through 13, and Table 16 are included in the vector. See the *Tri-Mode Ethernet MAC User Guide* for detailed information.

Table 17: **Alternative to the Optional Management Interface: Configuration Vector Signal Pinout**

Signal	Direction	Description
tieemacconfigvec[67:0]	Input	The Configuration Vector is used to replace the functionality of the MAC Configuration Registers when the Management Interface is not used.

Note: All bits of `tieemacconfigvec` are registered on input but can be treated as asynchronous inputs.

Address Filter Signal Definition

Table 18 describes the address filter unicast address input.

Table 18: **Address Filter Unicast Address**

Signal	Direction	Description
tieemacunicastaddr[47:0]	Input	Vector used to set the default address for the MAC.

Clock, Speed Indication, and Reset Signal Definition

Table 19 describes the reset signal, the clock signals that are input to the core, and the outputs that can be used to select between the three operating speeds. The clock signals are generated in the top-level wrapper provided with the core.

Table 19: **Clock and Speed Indication Signals**

Signal	Direction	Description
reset	Input	Asynchronous reset for entire core.
txgmiimiiclk	Input	Clock for the transmission of data on the physical interface. 125 MHz at 1 Gb/s, 25 MHz at 100 Mb/s, and 2.5 MHz at 10 Mb/s. This clock should be used to clock the physical interface transmit circuitry. If the core is generated with the clock enable option, this clock is also used to clock the client transmit circuitry.
rxgmiimiiclk	Input	Clock for the reception of data on the physical interface. 125 MHz at 1 Gb/s, 25 MHz at 100 Mb/s, and 2.5 MHz at 10 Mb/s. This clock should be used to clock the physical interface receive circuitry. If the core is generated with the clock enable option, this clock is also used to clock the client receiver circuitry.
speedis100	Output	Output asserted when the core is operating at 100 Mb/s. It is derived from a configuration register (if the optional Management Interface is present) or from the tieemacconfigvec configuration vector (if the optional Management Interface is not present).
speedis10100	Output	This output is asserted when the core is operating at either 10 Mb/s or 100 Mb/s. It is derived from a configuration register (if the optional Management Interface is present) or from the tieemacconfigvec configuration vector (if the optional Management Interface is not present).

Physical Interface Signal Definition

Table 20 describes the MDIO (MII Management) interface signals of the core, which are typically connected to the MDIO port of a PHY device, either off-chip or an SoC-integrated core. The MDIO format is defined in *IEEE 802.3-2008* clause 22.

Table 20: **MDIO Interface Signal Pinout**

Signal	Direction	Description
emacphymclkout	Output	MDIO Management Clock: derived from hostclk on the basis of supplied configuration data when the optional Management Interface is used.
emacphymdin	Input	Input data signal for communication with PHY configuration and status. Tie high if unused.
emacphymdout	Output	Output data signal for communication with PHY configuration and status.
emacphymdtri	Output	3-state control for MDIO signals; '0' signals that the value on MDIO_OUT should be asserted onto the MDIO bus.

Table 21 describes the GMII/MII signals of the core, which are typically attached to a PHY module, either off-chip or internally integrated. The GMII is defined in *IEEE 802.3-2008* clause 35, and MII is defined in *IEEE 802.3-2008* clause 22.

Table 21: **Optional GMII Interface Signal Pinout**

Signal	Direction	Clock Domain	Description
phyemactxenable	Input	gmiimiitxclk	Transmitter clock enable signal for the GMII/MII logic within the core. This signal is present when: The TEMAC solution is generated for 10/100 Mb/s only ethernet speed support. The TEMAC solution is generated for tri-speed ethernet support when using the optional clock enables.
emacphytxd[7:0]	Output	gmiimiitxclk	Transmit data to PHY
emacphytxen	Output	gmiimiitxclk	Data Enable control signal to PHY
emacphytxer	Output	gmiimiitxclk	Error control signal to PHY
phyemaccrs	Input	N/A	Control signal from PHY
phyemaccol	Input	N/A	Control signal from PHY
phyemacrxd[7:0]	Input	gmiimiirxclk	Received data from PHY
phyemacrxdv	Input	gmiimiirxclk	Data Valid control signal from PHY
phyemacrxer	Input	gmiimiirxclk	Error control signal from PHY

Verification

The TEMAC solution has been verified with extensive simulation and hardware testing, as detailed in this section.

Simulation

A highly parameterizable transaction-based test bench was used to test the core. Tests include:

- Register Access
- MDIO Access
- Frame Transmission and Error Handling
- Frame Reception and Error Handling
- Address Filtering

Hardware Verification

The TEMAC solution has been tested in a variety of hardware test platforms at Xilinx to address specific parameterizations, including the following:

- Testing with the Ethernet 1000BASE-X PCS/PMA or SGMII core, as illustrated in the architecture displayed in Figure 3. A test platform was built around these cores, including a back-end FIFO capable of performing a simple ping function and a test pattern generator. Software running on the embedded PowerPC® processor was used to provide access to all configuration, status and statistical counter registers. Testing has been performed in Virtex®-4 and Virtex-5 devices.
- Testing with an external PHY device. The MAC has been connected to external BASE-T PHY devices using both GMII and RGMII interfaces, as illustrated in the architecture displayed in Figure 2. A test platform was built around the core, including a back-end FIFO capable of performing a simple ping function and a test pattern generator. Software running on an embedded processor (PowerPC or MicroBlaze™) was used to provide access to all configuration, status and statistical counter registers. Testing has been performed in Virtex-4, Virtex-5 and Spartan®-3A DSP devices.

Device Utilization

The Virtex-6, Virtex-5 and Spartan-6 FPGA families contain six input LUTs; all other families contain four input LUTs. For this reason, the device utilization for these families are listed separately. See either of the following sections:

- New Device Families (Six input LUT)
- Other Device Families

New Device Families (Six input LUT)

Table 22 provides approximate utilization figures for various core options when a single instance of the core is instantiated in a Virtex-5 device. Other families (Spartan-6, Virtex-6) have similar utilization figures.

Note: Virtex-6 devices support GMII and MII at 2.5V only; see the *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*. Virtex-5, Virtex-4, Spartan-6 and Spartan-3 devices support MII and GMII at 3.3V or lower.

Utilization figures are obtained by implementing the block level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

Table 22 does not differentiate between 10/100/1000 Mb/s support and 1 Gb/s only support for GMII and RGMII Physical Interfaces. The numbers quoted are for 10/100/1000 Mb/s support; 1 Gb/s only support Slice, LUT and FF figures will be slightly reduced.

Table 23 gives utilization numbers for the 10/100 Mb/s only configuration.

BUFG usage:

- does not consider multiple instantiations of the core, where clock resources can often be shared.
- does not include the reference clock required for IDELAYCTRL. This clock source can be shared across the entire device and is not core specific.

Table 22: **10/100/1000 Mb/s and 1 Gb/s Device Utilization for New Device Families**

Core Parameters					Device Resources			
Physical Interface	Management Interface	Half-Duplex support	Address Filter	Addr Table Entries	Slices	LUTs	FFs	BUFGs
GMII	Yes	No	Yes	4	740	1190	1200	3
GMII	Yes	No	Yes	0	665	990	1150	3
GMII	Yes	No	No	N/A	590	850	1010	3
GMII	No	No	Yes	0	510	780	890	2
GMII	No	No	No	N/A	490	720	840	2
GMII	Yes	Yes	Yes	4	950	1540	1420	3
GMII	Yes	Yes	Yes	0	830	1340	1365	3
GMII	Yes	Yes	No	N/A	800	1200	1230	3
GMII	No	Yes	Yes	0	690	1130	1100	2
GMII	No	Yes	No	N/A	675	1070	1050	2
RGMII	Yes	No	Yes	4	741	1220	1220	3
RGMII	Yes	No	Yes	0	610	1010	1160	3
RGMII	Yes	No	No	N/A	600	880	1030	3
RGMII	No	No	Yes	0	515	810	905	2
RGMII	No	No	No	N/A	490	750	740	2
RGMII	Yes	Yes	Yes	4	900	1580	1435	3
RGMII	Yes	Yes	Yes	0	775	1400	1380	3
RGMII	Yes	Yes	No	N/A	775	1230	1245	3
RGMII	No	Yes	Yes	0	685	1160	1120	2
RGMII	No	Yes	No	N/A	642	1095	1070	2

Table 23: **10/100 Mb/s only Device Utilization for New Device Families**

Core Parameters					Device Resources			
Physical Interface	Management Interface	Half-Duplex support	Address Filter	Addr Table Entries	Slices	LUTs	FFs	BUFGs
MII	Yes	No	Yes	4	700	1180	1180	3
MII	Yes	No	Yes	0	620	1010	1125	3
MII	Yes	No	No	N/A	560	830	990	3
MII	No	No	Yes	0	475	760	865	2
MII	No	No	No	N/A	445	700	815	2

Table 23: **10/100 Mb/s only Device Utilization for New Device Families *(Cont'd)***

Core Parameters					Device Resources			
MII	Yes	Yes	Yes	4	880	1530	1400	3
MII	Yes	Yes	Yes	0	800	1355	1340	3
MII	Yes	Yes	No	N/A	795	1180	1210	3
MII	No	Yes	Yes	0	670	1095	1080	2
MII	No	Yes	No	N/A	610	1040	1030	2

Other Device Families

Table 24 provides approximate utilization figures for various core options when a single instance of the core is instantiated in a Spartan-3A device. Other devices (Virtex-4, Spartan-4, Spartan-3E, Spartan-3A DSP) have similar utilization figures.

Utilization figures are obtained by implementing the block-level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

Table 24 does not differentiate between 10/100/1000 Mb/s support and 1 Gb/s only support for GMII and RGMII Physical Interface. The numbers quoted are for 10/100/1000 Mb/s support; 1 Gb/s only support Slice, LUT and FF figures will be slightly reduced.

Table 25 gives utilization numbers for the 10/100 Mb/s only configuration.

BUFG usage does not consider multiple instantiations of the core, where clock resources can often be shared.

Table 24: **10/100/1000 Mb/s and 1 Gb/s Device Utilization for Spartan-3 and Virtex-4 Families**

Core Parameters					Device Resources				
Physical Interface	Management Interface	Half-Duplex support	Address Filter	Addr Table Entries	Slices	LUTs	FFs	BUFGs	DCM
GMII	Yes	No	Yes	4	1470	1610	1230	3	1
GMII	Yes	No	Yes	0	1260	1190	1170	3	1
GMII	Yes	No	No	N/A	1180	1040	1040	3	1
GMII	No	No	Yes	0	970	930	915	2	1
GMII	No	No	No	N/A	955	895	860	2	1
GMII	Yes	Yes	Yes	4	1725	2045	1445	3	1
GMII	Yes	Yes	Yes	0	1670	1660	1390	3	1
GMII	Yes	Yes	No	N/A	1420	1470	1255	3	1
GMII	No	Yes	Yes	0	1310	1360	1130	2	1
GMII	No	Yes	No	N/A	1255	1300	1075	2	1
RGMII	Yes	No	Yes	4	1605	1645	1295	4	2
RGMII	Yes	No	Yes	0	1370	1260	1240	4	2
RGMII	Yes	No	No	N/A	1260	1080	1100	4	2
RGMII	No	No	Yes	0	1040	970	980	3	2
RGMII	No	No	No	N/A	1030	1000	930	3	2

Table 24: **10/100/1000 Mb/s and 1 Gb/s Device Utilization for Spartan-3 and Virtex-4 Families *(Cont'd)***

Core Parameters					Device Resources				
RGMII	Yes	Yes	Yes	4	1850	2080	1510	4	2
RGMII	Yes	Yes	Yes	0	1750	1660	1455	4	2
RGMII	Yes	Yes	No	N/A	1550	1510	1320	4	2
RGMII	No	Yes	Yes	0	1390	1400	1195	3	2
RGMII	No	Yes	No	N/A	1355	1340	1140	3	2

Table 25: **10/100 Mb/s only Device Utilization for Spartan-3 and Virtex-4 Families**

Core Parameters					Device Resources				
Physical Interface	**Management Interface**	**Half-Duplex support**	**Address Filter**	**Addr Table Entries**	**Slices**	**LUTs**	**FFs**	**BUFGs**	**DCM**
MII	Yes	No	Yes	4	1410	1600	1180	3	0
MII	Yes	No	Yes	0	1250	1205	1125	3	0
MII	Yes	No	No	N/A	1070	1020	990	3	0
MII	No	No	Yes	0	930	915	870	2	0
MII	No	No	No	N/A	900	855	820	2	0
MII	Yes	Yes	Yes	4	1730	2000	1400	3	0
MII	Yes	Yes	Yes	0	1565	1620	1345	3	0
MII	Yes	Yes	No	N/A	1420	1440	1210	3	0
MII	No	Yes	Yes	0	1225	1335	1080	2	0
MII	No	Yes	No	N/A	1210	1275	1030	2	0

Performance

Performance in Virtex-6 Lower Power Devices

Ethernet MAC limitations:

- Use of the GMII physical interface for 1 Gb/s operation will not meet the receiver setup and/or hold time requirements of the GMII specification by a total of at least 165 ps. Sufficient system margin and IODELAY tap settings are necessary for correct operation. See Xilinx Answer Record 40028 for more details.
- Use of the RGMII physical interface for 1 Gb/s operation is marginal with respect to the RGMII receiver timing specification. Sufficient system margin and IODELAY tap settings are necessary for correct operation. See Xilinx Answer Record 40028 for more details.

Performance in Spartan 6 Devices

Ethernet MAC limitation:

- Use of the GMII physical interface for 1 Gb/s operation will not meet the receiver setup and/or hold time requirements of the GMII specification. Sufficient system margin and IODELAY tap settings are necessary for correct operation. See Xilinx Answer Record 35336 for more details.

References

[1] Virtex-4, Virtex-5 and Virtex-6 FPGA User Guides

[2] Spartan-6, Spartan-3, Spartan-3E, Spartan-3A, Spartan-3AN, Spartan-3A DSP FPGA Data Sheets

[3] *IEEE 802.3-2008* specification

Support

For technical support, visit www.xilinx.com/support. Xilinx provides technical support for this product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation, if customized beyond that allowed in the product documentation, or if any changes are made in sections of design marked *DO NOT MODIFY*.

Ordering Information

The following table shows the bundle offerings.

Table 26: **TEMAC Bundle Offerings**

Part Number	License	IP Cores
EF-DI-TEMAC-SITE	SignOnce IP Site License	10/100/1000 Mb/s, 1Gb/s, 10/100 Mb/s
EF-DI-TEMAC-PROJ	SignOnce IP Project License	10/100/1000 Mb/s, 1Gb/s, 10/100 Mb/s
EF-DI-10-100-EMAC-SITE	SignOnce IP Site License	10/100 Mb/s

Two free evaluation licenses are provided: The Simulation Only license is provided with the CORE Generator™ software, and the Full-System Hardware Evaluation license, which lets you test your designs in hardware for a limited period of time, can be downloaded from the TEMAC product page.

For full access to all core functionality, both in simulation and in hardware, you must purchase the core. After purchasing, go to the TEMAC product page for more information on generating the relevant license key for use with the Xilinx Core Generator System v13.1.

Contact your local Xilinx sales representative for pricing and availability about Xilinx LogiCORE IP modules and software or see the Xilinx IP Center.

List of Acronyms

Table 1-1: **List of Acronyms**

Acronym	Spelled Out
DA	Destination Address
DCM	Digital Clock Manager
DDR	Double Data Rate
FCS	Frame Check Sequence
FF	flip-flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array.
GBIC	Gigabit Interface Converter
Gb/s	Gigabits per second
GMII	Gigabit Media Independent Interface
HDL	Hardware Description Language
IO	Input/Output
IOB	Input/Output Block
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mb/s	Megabits per second
MDIO	Management Data Input/Output
NGC	Native Generic Circuit
NGD	Native Generic Database
PCS	Physical Coding Sublayer
PHY	physical-side interface
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
RGMII	Reduced Gigabit Media Independent Interface
SA	Source Address
SFP	Small Form-Factor Pluggable
SGMII	Serial Gigabit Media Independent Interface
TEMAC	Tri-Mode Ethernet MAC
UCF	User Constraints File
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
VLAN	Virtual LAN (Local Area Network)

Revision History

Date	Version	Revision
7/06/04	1.0	Initial draft.
9/24/04	1.1	Initial Xilinx release.
4/28/05	2.0	Updated to version 2.1 of the core, Xilinx tools v7.1i, and support for Spartan-3E devices.
1/18/06	2.1	Updated to release date, version 2.2 of the core, and Xilinx tools 8.1i
7/13/06	3.1	Core version 3.1; Xilinx tools 8.2i.
9/21/06	3.2	Core version updated to 3.2, Spartan-3A device added to supported device family in Facts table.
2/15/07	3.3	Updated to version 3.3; Xilinx tools 9.1i.
8/8/07	3.4	Updated core to version 3.4; Xilinx tools v9.2i, Cadence US v5.8.
3/24/08	3.5	Update core to version 3.5; Xilinx tools v10.1; Cadence IUS v6.1.
4/24/09	3.6	Update core to version 4.1; Xilinx tools v11.1; Added Spartan-6 and Virtex-6 devices; Mentor Graphics ModelSim v6.4b; Cadence IUS v8.1-s009; Synopsys 2008.09
6/24/09	3.7	Update core to version 4.2; Xilinx tools v11.2. Added Virtex-6 CXT support.
09/16/09	3.8	Update core to version 4.3; Xilinx tools v11.3; Added licensing support for 10/100 Mb/s only core. Added Virtex-6 HXT and Virtex-6 -1L support.
12/02/09	3.8.1	Updated licensing information.
04/19/10	3.9	Update core to version 4.4; Xilinx tools v12.1.
03/01/11	4.0	Update core to version 4.5; Xilinx tools v13.1.

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