UHD-SDI GT v2.0

LogiCORE IP Product Guide

Vivado Design Suite

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Introduction

The Xilinx® UHD-SDI GT LogiCORE IP is designed to work with the Society of Motion Picture and Television Engineers (SMPTE) UHD-SDI Transmitter and Receiver Subsystems by providing a wizard to configure the UltraScale™ serial transceivers to interface directly to the subsystems.

Features

- Supports GTHE4 and GTYE4 transceiver configuration presets for industry standards for SMPTE UHD-SDI.
- Supports the following line rates as per standards compliance:
  - **SMPTE ST 259:** SD-SDI at 270 Mb/s
  - **SMPTE RP 165:** EDH for SD-SDI
  - **SMPTE ST 292:** HD-SDI at 1.485 Gb/s and 1.485/1.001 Gb/s
  - **SMPTE ST 372:** Dual Link HD-SDI
  - **SMPTE ST 424:** 3G-SDI with data mapped by any ST 425-x mapping at 2.97 Gb/s and 2.97/1.001 Gb/s
  - **SMPTE ST 2081-1:** 6G-SDI with data mapped by any ST 2081-x mapping at 5.94 Gb/s and 5.94/1.001 Gb/s
  - **SMPTE ST 2082-1:** 12G-SDI with data mapped by any ST 2082-x mapping at 11.88 Gb/s and 11.88/1.001 Gb/s
- Dual link and quad link 6G-SDI and 12G-SDI supported by instantiating two or four SMPTE UHD-SDI RX or TX subsystems.
- Transceiver can be configured as unidirectional and bidirectional.
- Transceiver site and reference clock selection interface.
- Transceivers can be configured with PICXO or FRACXO to provide advanced options to tune performance.
- Optional exposure of any transceiver port depending upon the selected configuration.
- Supports upto four links for SMPTE-SDI.
- Provides flexibility to configure GT data width and PLL types based on your requirement.

IP Facts

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family[1]	Kintex® UltraScale+™, Virtex® UltraScale+™ (GTHE4 & GTYE4), Zynq® UltraScale+™ MPSoC (GTHE4 & GTYE4), Zynq® UltraScale+™ RFSoC
Supported User Interfaces	Not Applicable
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	RTL
Example Design	Verilog
Test Bench	N/A
Constraints File	Xilinx® Design Constraints (XDC)
Simulation Model	N/A
Supported S/W Driver	Not Provided
Tested Design Flows[2]	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Release Notes and Known Issues	Master Answer Record: 70291
All Vivado IP Change Logs	Master Vivado IP Change Logs:72775
Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado® IP catalog.
2. For the supported versions of third-party tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Core Overview

The UHD-SDI GT core implements the use of one or more serial transceivers in a Xilinx® UltraScale+™ device. See Chapter 3: Product Specification for a detailed description of the core.

The information in this section is intended to supplement, not replace, the information in the *UltraScale Architecture GTH Transceivers User Guide* (UG576) and *UltraScale Architecture GTY Transceivers User Guide* (UG578). This information highlights features and operating requirements of the GTH/GTY transceivers that are of particular importance for UHD-SDI applications.

In the UHD-SDI GT core, the naming convention followed for GTH/GTY transceiver ports is same as used in the *UltraScale Architecture GTH Transceivers User Guide* (UG576) and *UltraScale Architecture GTY Transceivers User Guide* (UG578). This convention is to use only the base name of a port. When the UltraScale device transceiver wizard is used to create a GTH/GTY wizard module, all input ports names have a suffix of `_in` and all outputs have a suffix of `_out`. For example, when a port named `txpllclksel` is referred to in this document, the actual name of that port in the GTH/GTY wrapper is `txpllclksel_in`.

Applications

The UHD-SDI GT core is the supported method of configuring and using one or more serial transceivers in a Xilinx UltraScale device. This IP is intended to be used with the UHD SDI receiver and transceiver subsystems.

Unsupported Features

The following features of the standard are not supported in the core:

- Standalone use; it is designed to be used with the Xilinx® UHD-SDI receiver or transmitter subsystems. See *SMPTE UHD-SDI Transmitter Subsystem Product Guide* (PG289) and *SMPTE UHD-SDI Receiver Subsystem Product Guide* (PG290) for details.

- Fractional controlled crystal oscillator (FRACXO) mode can only be supported for GTYE transceivers not for GTHE transceivers.
- Phase interpolator controlled crystal (PICXO) or FRACXO mode can only be supported for use cases where `tx_clkout` and `rx_clkout` frequency from a GT Quad is same, hence cannot be used for RX only or TX only configurations.
- Multi-link support is available with the flexibility to choose the reference clock between QPLL0 or QPLL1, or CPLL. However, multi-link support with CPLL selection is not validated.

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado® Design Suite under the terms of the Xilinx End User License.

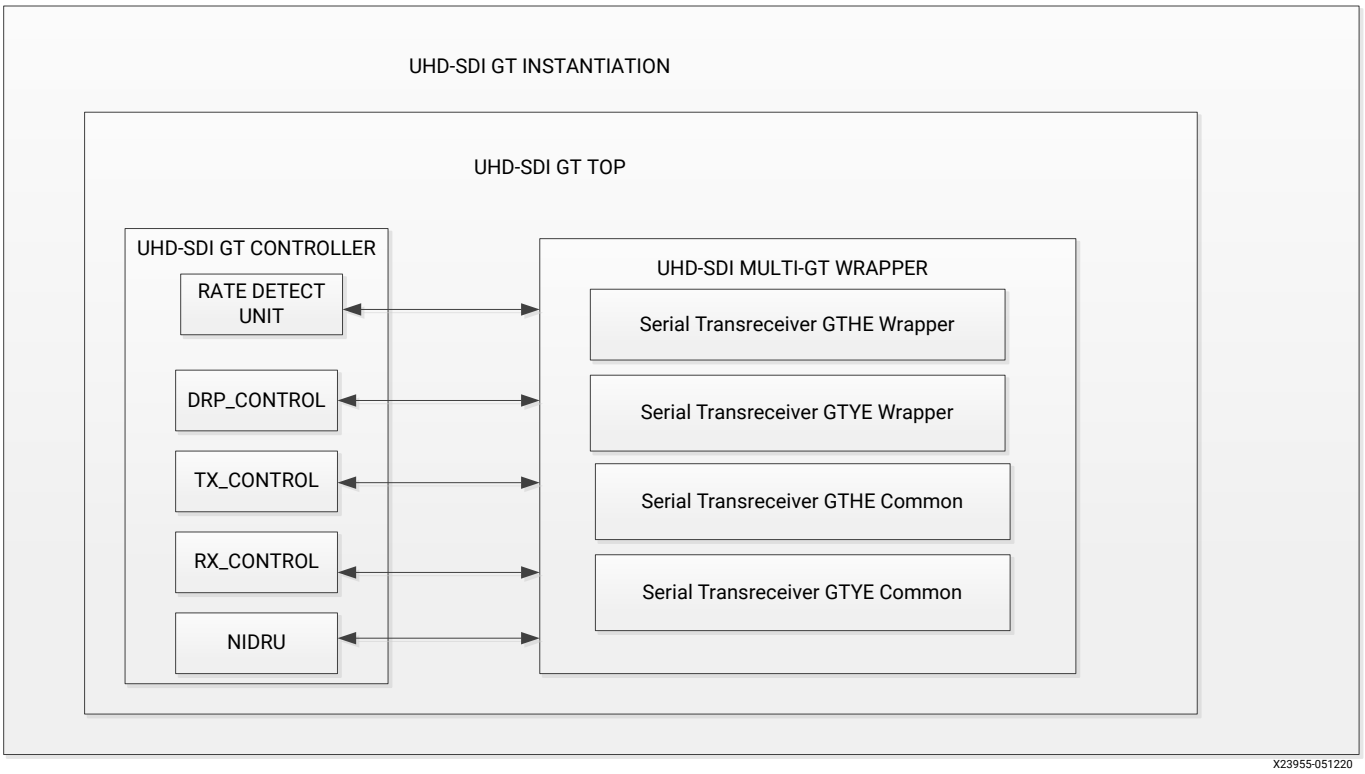
For more information about this core, visit the UHD-SDI GT product web page.

Information about other Xilinx® LogiCORE™ IP modules is available at the Xilinx Intellectual Property page. For information about pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

The Xilinx® UHD-SDI GT core is the supported method of configuring and using transceivers with Xilinx UHD-SDI subsystem IP cores. The core simplifies serial transceiver (GT) use by providing a standardized interface of serial transceiver functions. The functional block diagram of the core is shown in the following figure:

Figure 1: **UHD-SDI GT Core Block Diagram**



The UHD-SDI GT controller has the following blocks:

- **Rate Detect Unit:** This module is implemented to distinguishes between 1000/1000 and 1000/1001 bit rates of the incoming SDI signal by timing the RXUSRCLK relative to a fixed frequency clock. This module implements two counters. One driven by the reference clock and other driven by the recovered clock. The two counters help in the automatic recognition of the two SDI bit rates. This module looks for the clock frequency change and generates a "rate" signal output whenever there is asynchronous clock switching due to rate change or any other reason. It indicates whenever a drift is seen in the recovered clock beyond a threshold value. This module validates the number of changes before generating the rate_output or clock drift status signals.
- **Drp_Control:** The control module programs the transceiver using the DRP interface. For example, the serial clock divider value of each RX and TX unit can be changed dynamically through the DRP by using the `RXOUT_DIV` and `TXOUT_DIV` attributes.
- **TX_Control:** This module modifies attributes in the GTH and GTY transceivers in response to the changes in the TX SDI mode and bit rate. This module is specifically designed to support SDI interfaces implemented in GTH and GTY transceivers. It changes the `TXPLLCLKSEL`, `TXOUT_DIV`, `TXDATA_WIDTH`, and `TXINT_DATAWIDTH` attributes when the SDI mode and TXPLL input changes.
- **RX_Control:** This module modifies attributes in the GTH and GTY transceivers in response to the changes in the RX SDI mode and bit rate. This module is specifically designed to support SDI interfaces implemented in the GTH and GTY transceivers. It changes the `RXPLLCLKSEL`, `RXCDR_CFG`, `RXOUT_DIV`, `RX_DATA_WIDTH`, `RX_INT_DATA_WIDTH` attributes when the SDI mode and RXPLL input changes.
- **NIDRU:** This block is used in applications where lower line rates (those below the rates supported by the respective GTs) are needed. In SDI, the NI-DRU is enabled when the SD-SDI mode is selected. It over samples the data input vector by eleven times in the SD-SDI mode.

The UHD-SDI MULTI-GT wrapper includes the following blocks depending on the core configuration:

- **Serial Transreceiver GTHE Wrapper:** This block instantiates the serial transceivers of a single GTHE quad.
- **Serial Transreceiver GTYE Wrapper:** This block instantiates the serial transceivers of a single GTYE quad.
- **Serial Transreceiver GTYE Common:** This block controls the common primitive of the GTYE serial transceiver. It has the external PLL management and DRP access.
- **Serial Transreceiver GTHE Common:** This block controls the common primitive of the GTHE serial transceiver. It has the external PLL management and DRP access.

Performance

The Xilinx® UHD-SDI GT core is designed to operate in coordination with the performance characteristics of the transceiver primitives it instantiates. The following documents provide information about DC and AC switching characteristics. The frequency ranges specified in these documents must be adhered to for proper transceiver and core operation.

- *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
- *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
- *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
- *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)

Resource Use

For full details about performance and resource use, visit the Performance and Resource Use web page.

Port Descriptions

The following sections describe various ports of UHD-SDI GT core.

cmp_gt_ctrl Input Ports

The `cmp_gt_ctrl` input ports are control inputs used in the SMPTE UHD-SDI GT IP and/or transceiver including GT COMMON. See the respective transceiver user guide for more information.

Table 2: **cmp_gt_ctrl[63:0] Input Ports**

Bit	Description
0	GT COMMON QPLL0 reset
1	GT COMMON QPLL0 Power down
2	GT COMMON QPLL1 reset
3	GT COMMON QPLL1 Power down
6:4	GT COMMON QPLL0 REFCLKSEL
7	GT COMMON QPLL0 REFCLKSEL valid
10:8	GT COMMON QPLL1 REFCLKSEL

Table 2: **cmp_gt_ctrl[63:0] Input Ports** *(cont'd)*

Bit	Description
11	GT COMMON QPLL1 REFCLKSEL valid
12	Link 0 CPLL reset. Provide Link 0 CPLL Power down input along with CPLL reset input to reset CPLL properly.
13	Link 0 CPLL Power down
14	txclk_ready. Connect the signal that indicates that TX reference clock is stable for Link 0
15	rxclk_ready. Connect the signal that indicates that RX reference clock is stable for Link 0
18:16	CPLLREFCLKSEL port selection for Link 0. Input to dynamically select the input reference clock to the Channel PLL. 000: Reserved 001: GTREFCLK0 selected 010: GTREFCLK1 selected 011: GTNORTHREFCLK0 selected 100: GTNORTHREFCLK1 selected 101: GTSOUTHREFCLK0 selected 110: GTSOUTHREFCLK1 selected 111: GTGREFCLK selected.
19	To enable CPLLREFCLKSEL input for Link 0. For Link 0, when this bit is set to 1, only bits[18:16] of cmp_gt_ctrl will select the reference clock value for CPLL. The selected value is fed to the CPLLREFCLKSEL input of the GT Transceiver. If The bit is unset, the reference clock selection will be automatically handled by design.
22:20	Link 0 GT LOOPBACK
23	Unused
24	Link 1 CPLL reset. Provide Link 1 CPLL Power down input along with CPLL reset input to reset CPLL properly.
25	Link 1 CPLL Power down
26	txclk_ready. Connect the signal that indicates that TX reference clock is stable for Link 1
27	rxclk_ready. Connect the signal that indicates that RX reference clock is stable for Link 1
30:28	CPLLREFCLKSEL port selection for Link 1. Input to dynamically select the input reference clock to the Channel PLL. 000: Reserved 001: GTREFCLK0 selected 010: GTREFCLK1 selected 011: GTNORTHREFCLK0 selected 100: GTNORTHREFCLK1 selected 101: GTSOUTHREFCLK0 selected 110: GTSOUTHREFCLK1 selected 111: GTGREFCLK selected.
31	To enable CPLLREFCLKSEL input for Link 1. For Link 1, when this bit is set to 1, then only bits[30:28] of cmp_gt_ctrl are used to select the reference clock value for CPLL. The selected value is fed to the CPLLREFCLKSEL input of the GT Transceiver. If the bit is unset, the reference clock selection will be automatically handled by design.
34:32	Link 1 GT LOOPBACK
35	Unused
36	Link 2 CPLL reset. Provide Link 2 CPLL Power down input along with CPLL reset input to reset CPLL properly.
37	Link 2 CPLL Power down

Table 2: **cmp_gt_ctrl[63:0] Input Ports** *(cont'd)*

Bit	Description
38	txclk_ready. Connect the signal that indicates that TX reference clock is stable for Link 2
39	rxclk_ready. Connect the signal that indicates that RX reference clock is stable for Link 2
42:40	CPLLREFCLKSEL port selection for Link 2. Input to dynamically select the input reference clock to the Channel PLL. 000: Reserved 001: GTREFCLK0 selected 010: GTREFCLK1 selected 011: GTNORTHREFCLK0 selected 100: GTNORTHREFCLK1 selected 101: GTSOUTHREFCLK0 selected 110: GTSOUTHREFCLK1 selected 111: GTGREFCLK selected.
43	To enable CPLLREFCLKSEL input for Link 2. When this bit is set to 1, then only bits[42:40] of cmp_gt_ctrl will be used to select the reference clock value for CPLL for link 2. The selected value be fed to the CPLLREFCLKSEL input of the GT Transceiver. If The bit is unset, the reference clock selection will be automatically handled by design.
46:44	Link 2 GT LOOPBACK
47	Unused
48	Link 3 CPLL reset
49	Link 3 CPLL reset. Provide Link 3 CPLL Power down input along with CPLL reset input to reset CPLL properly.
50	txclk_ready. Connect the signal that indicates that TX reference clock is stable for Link 3
51	rxclk_ready. Connect the signal that indicates that RX reference clock is stable for Link 3
54:52	CPLLREFCLKSEL port selection for Link 3. Input to dynamically select the input reference clock to the Channel PLL. 000: Reserved 001: GTREFCLK0 selected 010: GTREFCLK1 selected 011: GTNORTHREFCLK0 selected 100: GTNORTHREFCLK1 selected 101: GTSOUTHREFCLK0 selected 110: GTSOUTHREFCLK1 selected 111: GTGREFCLK selected.
55	To enable CPLLREFCLKSEL input for Link 3. When this bit is set to 1, then only bits[54:52] of cmp_gt_ctrl will be used to select the reference clock value for CPLL Link3. The selected value be fed to the CPLLREFCLKSEL input of the GT Transceiver. If The bit is unset, the reference clock selection will be automatically handled by design.
58:56	Link 3 GT LOOPBACK
63:59	Unused

cmp_gt_sts Output Ports

These are transceiver ports connected to the `cmp_gt_sts` bus. See the respective transceiver user guide for more information. The status pins in the following table are connected when SDI_LINKS is 1.

Table 3: **cmp_gt_sts[63:0] Output Ports**

Bit	Description
0	QPLL0 LOCK
1	QPLL1 LOCK
3:2	Unused
4	Link 0 GT CPLL LOCK
5	Link 0 GT TXRESETDONE
6	tx_change_done. Link 0 GT TX configuration is success for the given UHD-SDI line rate
7	UHD-SDI TX IP fabric reset
8	Link 0 GT RXRESETDONE
9	rx_change_done. Link 0 GT RX configuration is success for the given UHD-SDI line rate
10	UHD-SDI RX IP fabric reset
11	Tied to Zero 1'b0
12	rx_mode_locked, this signal indicates high when receiver mode is locked 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
13	rx_level_b, this signal is high when received mode is 3G level B 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
14	Link 0 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
15	rx_ce, receiver clock enable
18:16	rx_mode[2:0], this signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is zero, the rx_mode port changes its values as the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
19	rx_change_fail. Link 0 GT RX configuration is not success for the given UHD-SDI line rate
22:20	rx_change_fail_code for Link 0.
23	tx_change_fail. Link 0 GT TX configuration is not success for the given UHD-SDI line rate
24	Link 0 GT DRP failure
27:25	tx_change_fail_code for Link 0.
63:28	Unused

cmp_gt_sts Output Ports

The status pins in the following table are connected when SDI_LINKS is 2:

Table 4: **cmp_gt_sts[63:0] Output Ports**

Bit	Description
0	QPLL0 LOCK
1	QPLL1 LOCK
3:2	Unused
4	Link 0 GT CPLL LOCK
5	Link 0 GT TXRESETDONE
6	tx_change_done. Link 0 GT TX configuration is success for the given UHD-SDI line rate
7	UHD-SDI TX IP fabric reset
8	Link 0 GT RXRESETDONE
9	rx_change_done. Link 0 GT RX configuration is success for the given UHD-SDI line rate
10	UHD-SDI RX IP fabric reset
11	Unused
12	rx_mode_locked for Link 0, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
13	rx_level_b for Link 0, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
14	Link 0 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
15	Link 0 rx_ce Used only in case of multi link SDI. Receiver clock enable Bit - 18:16
18:16	Link 0 rx_mode[2:0] - Used only in case of multi link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
19	Link 1 GT CPLL LOCK
20	Link 1 GT TXRESETDONE
21	tx_change_done. Link 1 GT TX configuration is success for the given UHD-SDI line rate
22	UHD-SDI TX IP fabric reset
23	Link 1 GT RXRESETDONE
24	rx_change_done. Link 1 GT RX configuration is success for the given UHD-SDI line rate
25	UHD-SDI RX IP fabric reset
26	Unused
27	rx_mode_locked for Link 1, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked

Table 4: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
28	rx_level_b for Link 1, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
29	Link 1 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
30	rx_ce for Link1. Used only in the case of multi-link SDI. Receiver clock enable Bit - 33:31.
33:31	rx_mode[2:0] for Link 1. Used only in the case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
63:34	Unused

cmp_gt_sts Output Ports

The status pins in the following table are connected when SDI_LINKS is 3:

Table 5: **cmp_gt_sts[63:0] Output Ports**

Bit	Description
0	QPLL0 LOCK
1	QPLL1 LOCK
3:2	Unused
4	Link 0 GT CPLL LOCK
5	Link 0 GT TXRESETDONE
6	tx_change_done. Link 0 GT TX configuration is success for the given UHD-SDI line rate
7	UHD-SDI TX IP fabric reset
8	Link 0 GT RXRESETDONE
9	rx_change_done. Link 0 GT RX configuration is success for the given UHD-SDI line rate
10	UHD-SDI RX IP fabric reset
11	Unused
12	rx_mode_locked for link 0, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
13	rx_level_b for link 0, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B

Table 5: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
14	Link 0 rx_bit_rate. 1'b0 Integer SDI line rate; 1'b1 Fractional SDI line rate
15	Link 0 rx_ce,, Used only in case of multi link SDI. Receiver clock enable.
18:16	Link 0 rx_mode[2:0] - Used only in case of multi link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
19	Link 1 GT CPLL LOCK
20	Link 1 GT TXRESETDONE
21	tx_change_done. Link 1 GT TX configuration is success for the given UHD-SDI line rate
22	UHD-SDI TX IP fabric reset
23	Link 1 GT RXRESETDONE
24	rx_change_done. Link 1 GT RX configuration is success for the given UHD-SDI line rate
25	UHD-SDI RX IP fabric reset
26	Unused
27	rx_mode_locked for Link 1, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
28	rx_level_b for Link 1, this signal is high when received mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
29	Link 1 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
30	rx_ce for Link1. Used only in the case of multi-link SDI. Receiver clock enable Bit - 33:31
33:31	rx_mode[2:0] for Link 1. Used only in the case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.

Table 5: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
34	Link 2 GT CPLL LOCK
35	Link 2 GT TXRESETDONE
36	tx_change_done. Link 2 GT TX configuration is success for the given UHD-SDI line rate
37	UHD-SDI TX IP fabric reset
38	Link 2 GT RXRESETDONE
39	rx_change_done. Link 2 GT RX configuration is success for the given UHD-SDI line rate
40	UHD-SDI RX IP fabric reset
41	Unused
42	rx_mode_locked for Link 2, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
43	rx_level_b for Link 2, this signal is high when received mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
44	Link 2 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
45	rx_ce for Link 2. Used only in the case of multi-link SDI. Receiver clock enable Bit - 48:46
48:46	rx_mode[2:0] for Link 2. Used only in case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
63:49	Unused

cmp_gt_sts Output Ports

The status pins in the following table are connected when SDI_LINKS is 4.

Table 6: **cmp_gt_sts[63:0] Output Ports**

Bit	Description
0	QPLL0 LOCK
1	QPLL1 LOCK
3:2	Unused

Table 6: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
4	Link 0 GT CPLL LOCK
5	Link 0 GT TXRESETDONE
6	`tx_change_done`. Link 0 GT TX configuration is success for the given UHD-SDI line rate
7	UHD-SDI TX IP fabric reset
8	Link 0 GT RXRESETDONE
9	`rx_change_done`. Link 0 GT RX configuration is success for the given UHD-SDI line rate
10	UHD-SDI RX IP fabric reset
11	Unused
12	`rx_mode_locked` for Link 0, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
13	`rx_level_b` for Link 0, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
14	Link 0 `rx_bit_rate`. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
15	Link 0 `rx_ce` Used only in case of multi-link SDI. Receiver clock enable.
18:16	Link 0 rx_mode[2:0] - Used only in case of multi link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and `rx_mode_locked` output is low, the `rx_mode` port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the `rx_mode_locked` output goes high.
19	Link 1 GT CPLL LOCK
20	Link 1 GT TXRESETDONE
21	`tx_change_done`. Link 1 GT TX configuration is success for the given UHD-SDI line rate
22	UHD-SDI TX IP fabric reset
23	Link 1 GT RXRESETDONE
24	`rx_change_done`. Link 1 GT RX configuration is success for the given UHD-SDI line rate
25	UHD-SDI RX IP fabric reset
26	Unused
27	`rx_mode_locked` for Link 1, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked

Table 6: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
28	rx_level_b for Link 1, this signal is high when received mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
29	Link 1 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
30	rx_ce for Link 1. Used only in the case of multi-link SDI. The receiver clock enables Bit - 33:31.
33:31	rx_mode[2:0] for Link 1. Used only in the case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
34	Link 2 GT CPLL LOCK
35	Link 2 GT TXRESETDONE
36	tx_change_done. Link 2 GT TX configuration is success for the given UHD-SDI line rate
37	UHD-SDI TX IP fabric reset
38	Link 2 GT RXRESETDONE
39	rx_change_done. Link 2 GT RX configuration is success for the given UHD-SDI line rate
40	UHD-SDI RX IP fabric reset
42	rx_mode_locked for Link 2, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
43	rx_level_b for Link 2, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
43:41	Unused
44	Link 2 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
45	rx_ce for Link 2. Used only in the case of multi-link SDI. The receiver clock enables Bit - 48:46.

Table 6: **cmp_gt_sts[63:0] Output Ports** *(cont'd)*

Bit	Description
48:46	rx_mode[2:0] for Link 2. Used only in the case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
49	Link 3 GT CPLL LOCK
50	Link 3 GT TXRESETDONE
51	tx_change_done. Link 3 GT TX configuration is success for the given UHD-SDI line rate
52	UHD-SDI TX IP fabric reset
53	Link 2 GT RXRESETDONE
54	rx_change_done. Link 3 GT RX configuration is success for the given UHD-SDI line rate
55	UHD-SDI RX IP fabric reset
56	Unused
57	rx_mode_locked for Link 3, this signal indicates high when receiver mode is locked. 1'b0 = Receiver mode is not locked 1'b1 = Receiver mode is locked
58	rx_level_b for Link 3, this signal is high when receiver mode is 3G level B. 1'b0 = Receiver mode is not 3G level B 1'b1 = Receiver mode is 3G level B
59	Link 3 rx_bit_rate. 1'b0: Integer SDI line rate 1'b1: Fractional SDI line rate
60	rx_ce for Link 3. Used only in the case of multi-link SDI. The receiver clock enables Bit - 63:61.
63:61	rx_mode[2:0] for Link 3. Used only in the case of multi-link SDI. This signal indicates the current SDI mode of the receiver: 000 = HD 001 = SD 010 = 3G 100 = 6G 101 = 12G 1000/1000 110 = 12G 1000/1001 When the receiver is not locked and rx_mode_locked output is low, the rx_mode port changes its values while the receiver searches for the correct SDI mode. When the receiver detects the correct SDI mode, the rx_mode_locked output goes high.
63:60	Unused

rx_change_fail_code Output Port Encoding

The following table describes rx_change_fail_code output port encoding:

Table 7: **rx_change_fail_code output port encoding**

Code	Description
0	Reserved
1	When a change of the RX SDI mode is requested that requires changing the RXCDR_CFG2 attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written RXCDR_CFG2 value and its actual content after retries, the sequence fails with this failure code
2	When a change of the RX SDI mode is requested that requires changing the RXOUT_DIV attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written RXCDR_CFG2 value and its actual content after retries, the sequence fails with this failure code
3	The gtwiz_reset_rx_datapath_in port of the GT Wizard IP is asserted after completing a series for DRP and GT port during a dynamic change to reset the GT RX portion. If the gtwiz_reset_rx_done_out port of GT Wizard IP failed to assert after retries, the sequence fails with this failure code
4	When a change of the RX SDI mode is requested that requires changing the RXDATA_WIDTH attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written RXDATA_WIDTH value and its actual content after retries, the sequence fails with this failure code
5	When a change of the RX SDI mode is requested that requires changing the RXINT_DATAWIDTH attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written RXINT_DATAWIDTH value and its actual content after retries, the sequence fails with this failure code
7-6	Reserved

tx_change_fail_code Output Port Encoding

The following table describes tx_change_fail_code output port encoding:

Table 8: **tx_change_fail_code Output Port Encoding**

Code	Description
0	Reserved
1	When a change of the TX SDI mode is requested that requires changing the TXDATA_WIDTH attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written TXDATA_WIDTH value and its actual content after retries, the sequence fails with this failure code.
2	When a change of the TX SDI mode is requested that requires changing the TXINTDATA_WIDTH attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written TXINTDATA_WIDTH value and its actual content after retries, the sequence fails with this failure code.

Table 8: **tx_change_fail_code Output Port Encoding** *(cont'd)*

Code	Description
3	When a change of the TX SDI mode is requested that requires changing the TXOUT_DIV attribute in the GT transceiver, the UHD-SDI control module attempts to do a DRP write cycle to change that attribute. If the UHD-SDI DRP control module detected a mismatch between the written TXOUT_DIV value and its actual content after retries, the sequence fails with this failure code.
4	The gtwiz_reset_tx_datapath_in port of the GT Wizard IP is asserted after completing a series for DRP and GT port during a dynamic change to reset the GT TX portion. If the gtwiz_reset_tx_done_out port of GT Wizard IP failed to assert after retries, the sequence fails with this failure code.
7-5	Reserved

RX_AXIS4S Interface Ports

The following table describes RX_AXIS4S interface ports:

Table 9: **RX_AXIS4S Interface Ports**

Signal	I/O	Description
intf0_rxoutclk	O	SMPTE SDI RX core clock
intf0_rx_axis4s_ch0_tdata	O	Parallel data received from transceiver. n varies with SDI standard selection: n=40 for 6G-SDI and 12G-SDI n=20 for 3G-SDI
intf0_rx_axis4s_ch0_tvalid	O	Data valid
intf0_rx_axis4s_ch0_tready	I	SMPTE SDI RX core ready
intf0_rx_axis4s_ch0_tlast	O	Tuser Information. Not used

S_AXIS_STS_SB_RX Interface Ports

The following table describes S_AXIS_STS_SB_RX interface ports:

Table 10: **S_AXIS_STS_SB_RX Interface Ports**

Signal	I/O	Description
intf0_ctrl_sb_rx_tdata	I	Sideband signal information from transceiver block bit 0: rx_change_done—Indicates that SDI line rate is successful bit 2: gtrxresetdone bit 3: rx_m bit 8: rx_fabric_rst—SMPTE UHD-SDI RX IP is reset when this bit set to 1. All other bits are not used
intf0_ctrl_sb_rx_tvalid	I	Data valid
intf0_ctrl_sb_rx_tready	O	Core ready

TX_Configurable_Debug_Ports

The following table describes TX Configurable debug ports for UDHSDI GT:

Table 11: **TX Configurable Debug Ports**

Signal	I/O	Description
gt_txpmareset_in	I	This port is used to reset the TX PMA inside the GT transceiver. It is driven High and then de-asserted to start the TX PMA reset process. In sequential mode, activating this port resets both the TX PMA and the TX PCS.
gt_txpcsreset_in	I	This port is used to reset the TX PCS. It is driven High and then de-asserted to start the PCS reset process. In sequential mode, activating this port only resets the TX PCS.
gt_txdiffctrl_in	I	Driver Swing Control. The default is user-specified. All listed values are in mVPPD. ***Note***: The peak-to-peak differential voltage is defined when TXPOSTCURSOR = 5'b00000 and TXPRECURSOR =5'b00000. For more information, refer to UltraScale Architecture GTH Transceivers
gt_txpostcursor_in	I	Transmitter post-cursor TX pre-emphasis control. The default is user-specified. All listed values (dB) are typical. ***Note***: The TXPOSTCURSOR values are defined when the TXPRECURSOR =5'b00000 Emphasis = 20log10(Vhigh/Vlow) = |20log10 (Vlow/Vhigh)| Please refer to table TX Configurable POST CURSOR Driver Ports.
gt_txprecursor_in	I	Transmitter pre-cursor TX pre-emphasis control. The default is user-specified. All listed values (dB) are typical. ***Note***: The TXPRECURSOR values are defined when the TXPOSTCURSOR =5'b00000 Emphasis = 20log10(Vhigh/Vlow) = |20log10 (Vlow/Vhigh)| Please refer to table TX Configurable POST CURSOR Driver Ports.

TX_Configurable_POST_CURSOR_Driver_Ports

The following table describes TX Configurable POST CURSOR Driver Ports:

Table 12: **TX Configurable POST CURSOR Driver Ports**

[4:0]	Emphasis (dB)	Coefficient Units
5'b00000	0.00	0
5'b00001	0.22	1

Table 12: **TX Configurable POST CURSOR Driver Ports** *(cont'd)*

[4:0]	Emphasis (dB)	Coefficient Units
5'b00010	0.45	2
5'b00011	0.68	3
5'b00100	0.92	4
5'b00101	1.16	5
5'b00110	1.41	6
5'b00111	1.67	7
5'b01000	1.94	8
5'b01001	2.21	9
5'b01010	2.50	10
5'b01011	2.79	11
5'b01100	3.10	12
5'b01101	3.41	13
5'b01110	3.74	14
5'b01111	4.08	15
5'b10000	4.44	16
5'b10001	4.81	17
5'b10010	5.19	18
5'b10011	5.60	19
5'b10100	6.02	20
5'b10101	6.47	21
5'b10110	6.94	22
5'b10111	7.43	23
5'b11000	7.96	24
5'b11001	8.52	25
5'b11010	9.12	26
5'b11011	9.76	27
5'b11100	10.46	28
5'b11101	11.21	29
5'b11110	12.04	30
5'b11111	12.96	31

TX_Configurable_PRE_CURSOR_Driver_Ports

The following table describes TX Configurable PRE CURSOR Driver Ports:

Table 13: **TX Configurable PRE CURSOR Driver Ports**

[4:0]	Emphasis (dB)	Coefficient Units
5'b00000	0.00	0
5'b00001	0.22	1
5'b00010	0.45	2
5'b00011	0.68	3
5'b00100	0.92	4
5'b00101	1.16	5
5'b00110	1.41	6
5'b00111	1.67	7
5'b01000	1.94	8
5'b01001	2.21	9
5'b01010	2.50	10
5'b01011	2.79	11
5'b01100	3.10	12
5'b01101	3.41	13
5'b01110	3.74	14
5'b01111	4.08	15
5'b10000	4.44	16
5'b10001	4.81	17
5'b10010	5.19	18
5'b10011	5.60	19
5'b10100	6.02	20
5'b10101	6.02	20
5'b10110	6.02	20
5'b10111	6.02	20
5'b11000	6.02	20
5'b11001	6.02	20
5'b11010	6.02	20
5'b11011	6.02	20
5'b11100	6.02	20
5'b11101	6.02	20
5'b11110	6.02	20
5'b11111	6.02	20

Designing with the Core

This section includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

Registering Signals

To simplify timing and increase system performance in a programmable device design, keep all inputs and outputs registered between the user application and the core. This means that all inputs and outputs from the user application should come from, or connect to, a flip-flop. While registering signals might not be possible for all paths, it simplifies timing analysis and makes it easier for the Xilinx® tools to place and route the design.

Recognize Timing Critical Signals

The constraints provided with the example design identify the critical signals and timing constraints that should be applied.

Make Only Allowed Modifications

You should not modify the core. Any modifications can have adverse effects on system timing and protocol compliance. Supported user configurations of the core can only be made by selecting the options in the customization IP dialog box when the core is generated.

Clocking

The UHD-SDI GT core clocking architecture depends on your selection of QPLL and its associated reference clock. The following table describes core clocks:

Table 14: **Core Clock Details**

Clock	Frequency	IP Configuration	Notes
drpclk_in	100.0 MHz (Default)	All	DRPCLK frequency value valid range is device-dependent. See the respective data sheet for clock range (FGTHDRPCLK for GTH transceiver and FGTYDRPCLK for GTY transceiver)
intf_0_qpll0_refclk_in	148.5 MHz for integer SDI line rate or 148.35 MHz for fractional	SDI line rate GT COMMON Shared Logic is in core and QPLL0 is selected	This input clock connection depends on PLL reference clock selection
intf_0_qpll1_refclk_in	148.5 MHz for integer SDI line rate or 148.35 MHz for fractional	SDI line rate GT COMMON Shared Logic is in core and QPLL1 is selected	This input clock connection depends on PLL reference clock selection

There are several clocks required in applications using GTH/GTY transceivers. The SDI protocol, which does not allow for clock correction by stuffing and removing extra data in the data stream, requires careful attention to how these clocks are generated and used in the application. GTH/GTY transceivers require reference clocks to operate. The reference clocks are used by phase-locked loops (PLLs) in the GTH/GTY transceiver quad to generate serial clocks for the receiver and transmitter sections of each transceiver. As described in GTH Transceiver Reference Clocks, the serial bit rate of the GTH/GTY transmitter is an integer multiple of the reference clock frequency it is using. Furthermore, the data rate of the video provided to the input of the SDI transmitter datapath must also exactly match (or be a specific multiple of) the frequency of the reference clock used by the GTH/GTY transmitter. Consequently, you must determine how to generate the transmitter reference clock so that it is frequency-locked exactly with the data rate of the video stream being transmitted.

GTH/GTY Transmitter Clocking

The GTH/GTY transmitter clocking is handled by the Transmitter User Clocking Network Helper block when enabled during GT IP generation from the UltraScale FPGAs Transceiver Wizard. The txusrclk and txusrclk2 output is driven by a BUFG_GT within the helper block and its frequency is exactly equal to the word rate of the data that must enter the txdata port of the GTH/GTY transmitter. The txusrclk and txusrclk2 are generated in the GTH/GTY transmitter by dividing the serial clock from the PLL down to the word rate. See the *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182) UltraScale for more details on Transmitter User Clocking Network Helper block.

GTH/GTY Receiver Clocking

The GTH/GTY receiver reference clock, however, does not need an exact relationship with the bit rate of the incoming SDI signals. This is because the clock and data recovery (CDR) unit in the GTH/GTY receiver can receive bit rates that are up to ±1,250 ppm (≤ 6.6 Gb/s) or ±200 ppm (> 8.0 Gb/s) away from the nominal bit rate as set by the reference clock frequency. This allows the receiver reference clock to be generated by local oscillators that have no exact frequency relationship to the incoming SDI signal. The GTH/GTY receiver generates a recovered clock that is frequency-locked to the incoming SDI bit rate. These clocks are output as `rxusrclk` and `rxusrclk2` ports of the Receiver User Clocking Network Helper Block from the GTH/GTY Wizard IP and are driven by BUFG_GT. As is described in more detail later, `rxusrclk` and `rxusrclk2` are true recovered clocks when receiving all SDI line rates except when receiving SD-SDI signals.

Dynamic Reconfiguration Port (DRP) Clock

One additional clock is required for SDI applications. This is a free-running, fixed-frequency clock that is used as the clock for the dynamic reconfiguration port (DRP) of the GTH/GTY transceiver. This same clock is also usually supplied to the control module in the SDI wrapper where it is used for timing purposes. The valid frequency range for this clock is stated in the UltraScale FPGAs Transceiver Wizard and normally ranges from 3.125 to 200 MHz. The frequency of this clock does not require any specific relationship relative to other clocks or data rates of the SDI application. This clock must not change frequencies when the SDI mode changes. It must remain running at the same nominal frequency at all times. It also must never stop while the SDI application is active. This clock can be used for all SD interfaces in the device.

Clock Frequencies and Clock Enable Requirements

The frequency of the `rxusrclk` and `txusrclk` depend on the SDI mode and the width of the `rxdata` and `txdata` ports of the GTH/GTY transceiver. This relationship is fixed by the architecture of the GTH/GTY transceiver. The RX and the TX both use clock enables to throttle the data stream transfer data rate because, in some cases, the data rate on the data streams is less than the frequency of the clock. The Table 15: Clock Frequencies and Clock Enable Requirements table shows the relationships between SDI mode, number of active data streams, `rxdata`/`txdata` port widths, `rxoutclk`/`txoutclk` frequencies, and clock enable cadences. The clock enable cadences are given in number of clocks between assertions of the clock enable over two data word cycles where 1/1 means that the clock enable is asserted every clock cycle, 2/2 indicates assertion every other clock cycle (50% duty cycle), 4/4 indicates assertion every fourth clock cycle (25% duty cycle), and 5/6 indicates that the clock enable alternates between assertion every 5 or 6 clock cycles, to average once every 5.5 clock cycles (one instance of 5 clock cycles between High pulses on the clock enabled followed by one instance of six clock cycles between High pulses on the clock enable, with this pattern repeating).

Table 15: **Clock Frequencies and Clock Enable Requirements**

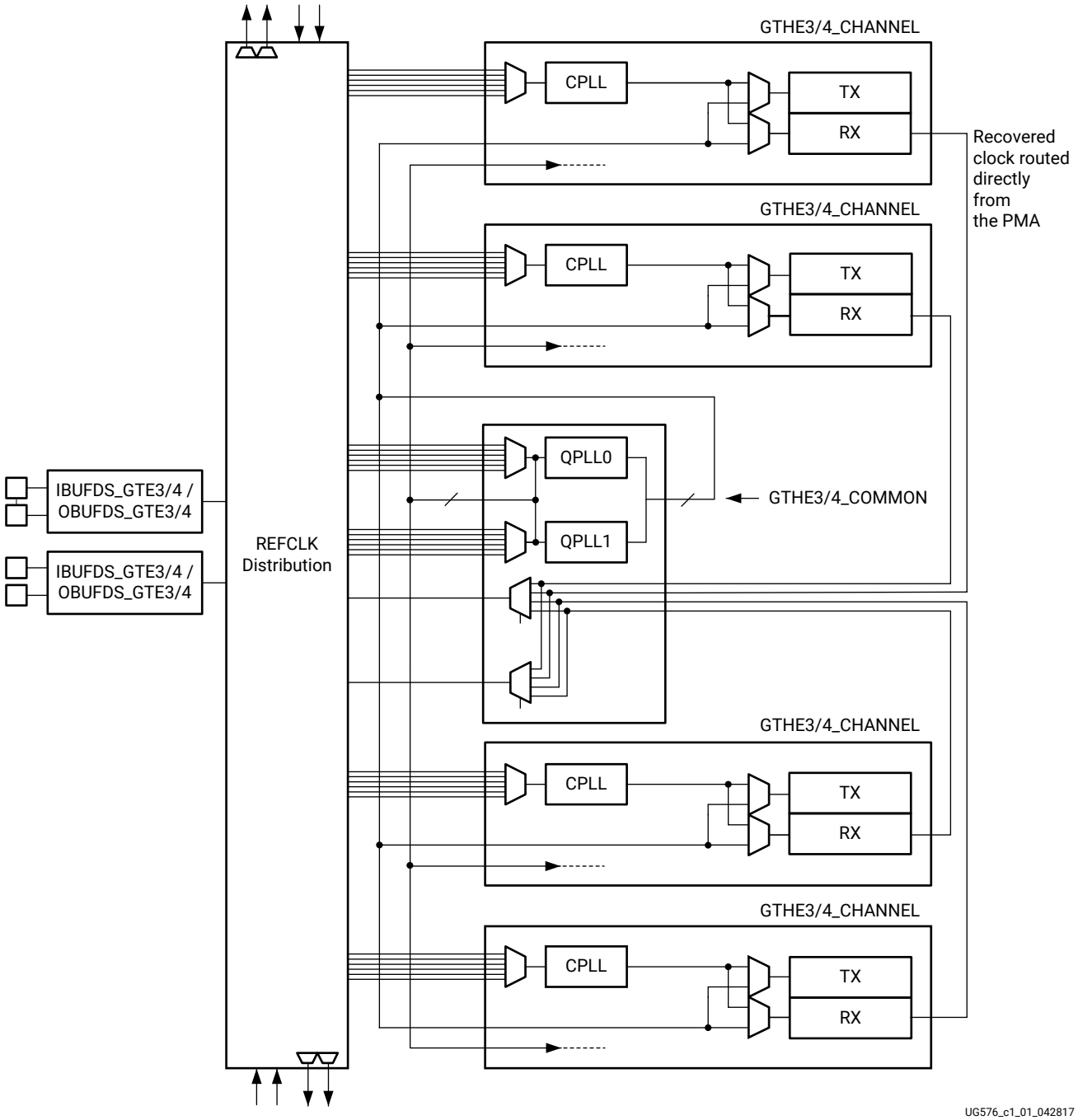
SDI-Mode	Active Data Streams	RX/TXDATA Bit Width	RX/TXOUTCLK Frequency	Clock Enable
SD-SDI	1	20	148.5 MHz	5/6
HD-SDI	2	20	74.25 or 74.25/1.001 MHz	1/1
3G-SDI A	2	20	148.5 or 148.5/1.001 MHz	1/1
3G-SDI B	4	20	148.5 or 148.5/1.001 MHz	2/2
6G-SDI	4	40	148.5 or 148.5/1.001 MHz	1/1
6G-SDI	8	40	148.5 or 148.5/1.001 MHz	2/2
12G-SDI	8	40	297 or 297/1.001 MHz	2/2
12G-SDI	16	40	297 or 297/1.001 MHz	4/4

GTH Transceiver Reference Clocks

UltraScale+™ GTH transceivers are grouped into quads. Each quad contains four GTHE4_CHANNEL transceiver primitives and one GTHE4_COMMON primitive containing two quad PLLs (QPLL0 and QPLL1) as shown in Figure 2: UltraScale+ GTH Transceiver Quad Configuration figure. The clock generated by the QPLL0 and QPLL1 are distributed to all four transceivers in the quad. Each GTHE4_CHANNEL has its own PLL called the Channel PLL (CPLL), which can provide a clock to the RX and TX of that transceiver only. Each RX and TX unit in the quad can be individually configured to use either/both QPLL0 or/and QPLL1 or the CPLL as its clock source. Furthermore, any RX or TX unit can dynamically switch its clock source between QPLL0, QPLL1 and CPLL. This configuration and the dynamic switching capability are particularly useful for SDI applications.

IMPORTANT! *The CPLL and QPLL have maximum line rates of 6.25 Gb/s and 16.375 Gb/s, respectively in an UltraScale -1 speed grade part. This means that CPLL can only be used up to 6G-SDI line rate while QPLLs can support up to 12G-SDI for -1 speed grade UltraScale+ GTH transceivers. The CPLL has a maximum line rate of 4.25 Gb/s and therefore it can only support up to 3G-SDI. This is a limitation only for-1 speed grade devices. See GTH Transceiver Switching Characteristics section of Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics (DS922) for details when selecting the appropriate device for your application*

Figure 2: **UltraScale+ GTH Transceiver Quad Configuration**



Typical UHD-SDI applications require the GTH transceivers to support nine different bit rates:

- 270 Mb/s for SD-SDI
- 1.485 Gb/s for HD-SDI
- 1.485/1.001 Gb/s for HD-SDI

- 2.97 Gb/s for 3G-SDI
- 2.97/1.001 Gb/s for 3G-SDI
- 5.94 Gb/s for 6G-SDI
- 5.94/1.001 Gb/s for 6G-SDI
- 11.88 Gb/s for 12G-SDI
- 11.88/1.001 Gb/s for 12G-SDI

The CDR unit in the RX section of the GTH/GTY transceiver can support receiving bit rates that are up to +/-1250 ppm from the reference frequency at bit rates less than 6.6 Gb/s. HD-SDI, 3G-SDI, 6G-SDI, and 12G-SDI each have two bit rates that differ by exactly 1000 ppm. For HD-SDI, 3G-SDI, and 6G-SDI, both bit rates can be received using a single reference clock frequency. That same reference clock frequency can also support reception of SD-SDI. Thus, for all SDI modes except 12G-SDI, just a single RX reference clock frequency is required. However, at 12G-SDI rates, the CDR unit has only ±200ppm tolerance relative to the reference clock frequency. Thus two different reference clock frequencies are needed to receive the two 12G-SDI bit rates. These two reference clock frequencies are typically 148.5 MHz to receive 11.88 Gb/s and 148.5/1.001 MHz to receive 11.88/1.001 Gb/s.

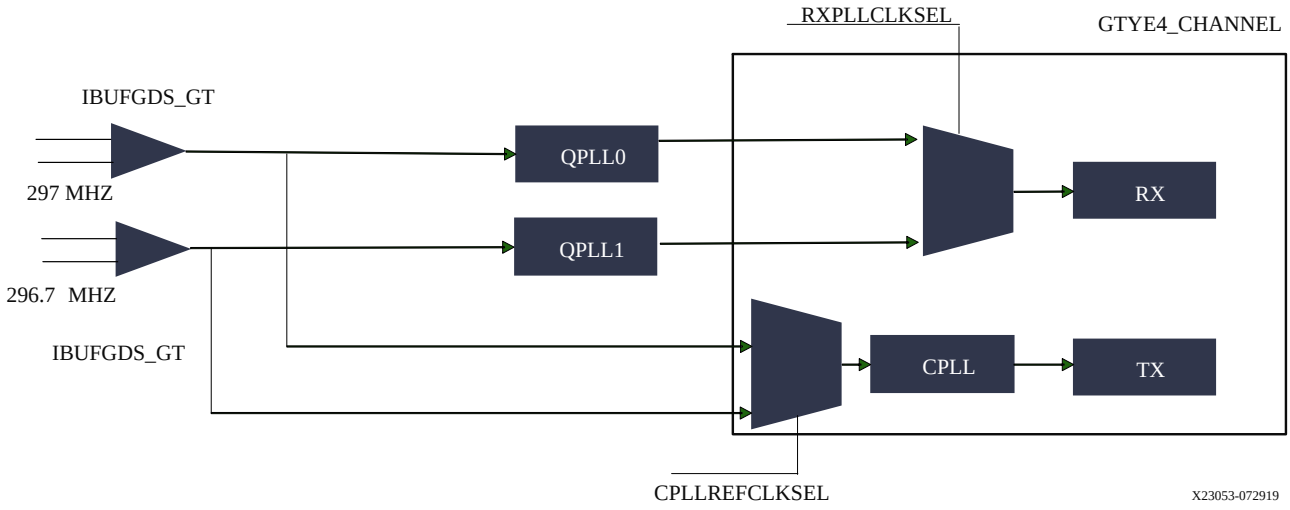
Therefore, most SDI applications provide two separate reference clocks to the GTH/GTY quad. Usually, the supplied reference frequency pair are 148.5 MHz and 148.5/1.001 MHz. This documentation always refers to the reference clock frequency pair 148.5 MHz and 148.5/1.001 MHz.

The source of the GTH/GTY transceiver reference clocks is very application specific. The receiver reference clock source can be a local oscillator because it does not need to match the incoming SDI bit rate exactly. However, because the GTH/GTY transmitter line rate is always an integer multiple of the reference clock frequency, the frequency of the transmitter reference clock must be exactly related to the data rate of the transmitted data. Most often, the transmitter reference clocks are generated by genlock PLLs, thereby deriving the GTH transmitter line rate from the studio video reference signal. In some cases, such as the SDI pass-through connection, the transmitter line rate is derived from the recovered clock of the GTH receiver that is receiving the SDI signal. In such cases, an external PLL is required to reduce the jitter on the recovered clock before using it as the transmitter reference clock.

In a typical UHD-SDI application, two reference clocks are connected to QPLL0 and QPLL1. In a case where the same transceiver is used for receiving and transmitting at 12G rate, Xilinx recommends you to use CPLL-QPLL combination with CPLL for TX and QPLL0/1 for RX as shown in Figure 3: Loopback Example Design GT Clocking Architecture figure. Integer and fractional rates for TX can be selected using CPLL reference clock input selection (CPLLREFCLKSEL) with 297 MHz and 296.7 MHz respectively. The RX and TX units of each transceiver in the quad dynamically switch between the PLL clocks, depending on the bit rate that is required at the moment. The GTH `txsysclksel` and `rxsysclksel` ports are used to

select the TX and RX units serial clock source between the PLLs. This common configuration for SDI applications is shown in Figure 4: Typical GTH Reference Clock Implementation for SDI figure where multiplexers that are not used dynamically in the implementation have been replaced with wires and the reference clock routing between quads is not shown. It is also possible to the connect one reference clock to CPLL and the other to QPLL0/1.

Figure 3: **Loopback Example Design GT Clocking Architecture**



Also, each GTH RX and TX unit has a serial clock divider that divides the selected clock by several selectable integer powers of two. This allows, for example, all of the RX units in the quad to use the same clock frequency from the QPLL but operate at different lines rates by using different serial clock divider values. This is very useful for SD interfaces because the 3G-SDI, 6G-SDI and 12G-SDI bit rates are exactly twice as fast the HD-SDI, 3G-SDI and 6G-SDI bit rates respectively. And, for 270 Mb/s SD-SDI, the GTH transceiver runs at the 3G-SDI line rate using 11X oversampling techniques. The ability of the RX and TX units to locally divide the clock source by four divisors that differ by a factor of two is important, allowing reception and transmission of all SDI bit rates using just two reference clock frequencies.

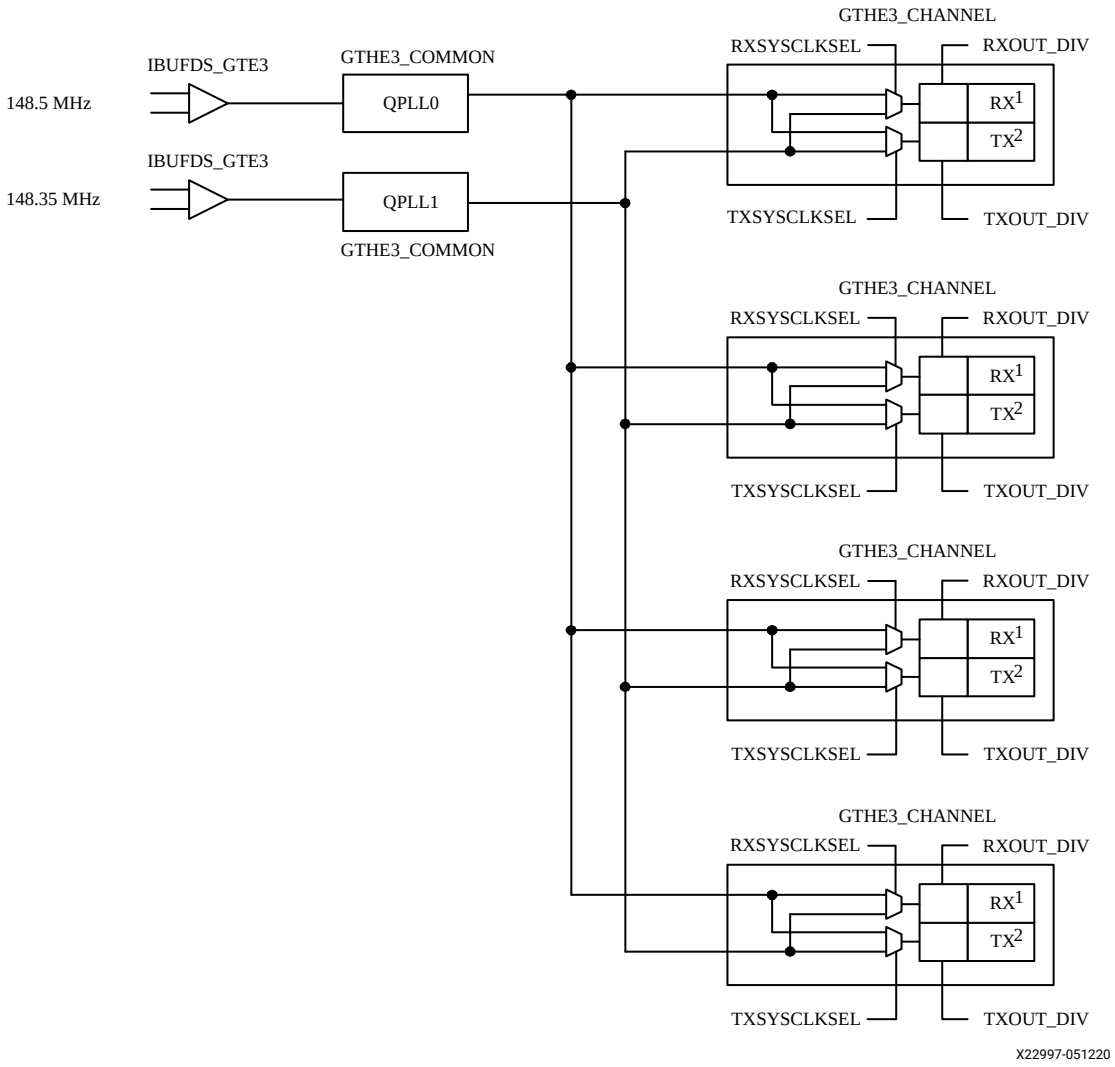
The serial clock divider value of each RX and TX unit can be changed dynamically through the DRP, by using the RXOUT_DIV and TXOUT_DIV attributes.

The configuration shown in Figure 4: Typical GTH Reference Clock Implementation for SDI figure is an optimal solution for most SDI applications for several reasons:

- The receivers can receive all SDI bit rates when using QPLL0 and QPLL1 to provide the serial clock derived from that reference clocks to all receivers in the quad.
- The transmitters have the flexibility to dynamically switch between the clocks from QPLL0 and QPLL1 to get both frequencies they need to transmit all supported SDI bit rates.

- When using QPLL0 and QPLL1 for 12G-SDI integer and fractional (1/1.001) rate change, switching between rates on the SDI-RX can introduce a glitch on the clock which in turn introduces CRC errors on the TX channel. CRC errors do not occur in SD-SDI/HD-SDI/ 3-G SDI/6-G SDI integer/fractional modes with QPLL0 and QPLL1 clocking combination. For more details, see Answer Record 72254 and 72449. Therefore, it is not recommended to use this clocking configuration when both transmit and receive 12G-SDI integer and fractional modes use the same transceiver. If required, Xilinx recommends to use CPLL-QPLL combination with CPLL for TX and QPLL0/1 for RX as shown in Figure 3: Loopback Example Design GT Clocking Architecture figure. The integer and fractional rates for TX can be selected using CPLL reference clock input selection with 297 MHz and 296.7 MHz respectively. This CPLL/QPLL clocking combination is recommended for an UltraScale+ GTH/GTY -2 speed grade or faster rate with >0.85V because this combination is not feasible with -1 speed grade devices due to CPLL bandwidth limitation. In such a case, users must use separate GT for RX and TX to achieve a 12G-SDI line rate with -1 speed grade device. Refer the respective FPGA data sheets for CPLL line rate limits.
- All four receivers and all four transmitters in the quad are fully independent and can each be running at different SDI bit rates and can dynamically switch between bit rates without disrupting the other RX or TX units
- For genlocked applications, modern genlock PLLs usually can simultaneously provide both required reference clock frequencies from the synchronization reference input signal.

Figure 4: **Typical GTH Reference Clock Implementation for SDI**



***Note*:**

1. CPLL-QPLL combination with CPLL for TX and QPLL0/1 for RX GTH RX interface and internal bit width are dynamically changed through RX_DATA_WIDTH and RX_INT_DATAWIDTH DRP attributes depending on the current SDI Mode and data stream inter-leaving pattern.
2. GTH TX interface and internal bit width are dynamically changed through TX_DATA_WIDTH and TX_INT_DATAWIDTH DRP attributes depending on the current SDI Mode and data stream inter-leaving pattern.
3. Xilinx recommends to use a CPLL-QPLL combination with CPLL for TX and QPLL0/1 for RX where both transmit and receive at 12G-SDI integer and fractional modes are using the same transceiver as shown in Figure 3: Loopback Example Design GT Clocking Architecture figure.

In some SDI applications, it might be necessary for different SDI transmitter to be running at slightly different bit rates even though they are transmitting at the same nominal bit rate. This is often the case with SDI routers where the bit rate of each TX must exactly match the bit rate of the SDI signal received by the SDI RX to which the TX is currently connected. In these cases, two transmitters that are transmitting at the same nominal bit rate, in fact, have bit rates that differ by a few ppm. Supporting such applications is possible with the UltraScale+ GTH quad architecture because each TX unit has exclusive use of its own CPLL. But to accomplish this, each CPLL must be provided with its own individual reference clock frequency, and the number of GTH/GTY reference clock inputs is limited. There are two reference clock inputs per GTH/GTY quad. A quad can use reference clocks from the quad above and the quad below. Thus, it is possible to provide some GTH quads in the device with five different reference clock frequencies (one for the RX and four for the four TX units), but overall, there are obviously not enough reference clock inputs to allow every GTH TX in the device to have its own reference clock. The PICXO technique can be very useful in these cases because it allows a GTH TX to be pulled by a few hundred ppm away from the frequency of its serial clock. Thus, applications where the bit rate of each SDI TX must be individually locked to the bit rate of the received SDI signal can be implemented by using common reference clocks as in Figure 4: Typical GTH Reference Clock Implementation for SDI figure and then using the PICXO technique with each GTH TX to set the exact bit rate of each SDI transmitter individually. This documentation does not cover the PICXO technique. For further information about using PICXO, contact Xilinx technical support.

Resets

The Rate Detect Module looks for the clock frequency change and generates a reset signal whenever there is asynchronous clock switching due to rate change or any other reason. It also indicates whenever a drift is seen in the recovered clock beyond a threshold value. This module validates the changes number of times before generating the reset or clock drift status signals.

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis, and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Core Configuration Tab

The following figure shows the Core Configuration tab for customizing the UHD-SDI GT core:

Figure 5: **UHD-SDI GT IP Configuration**

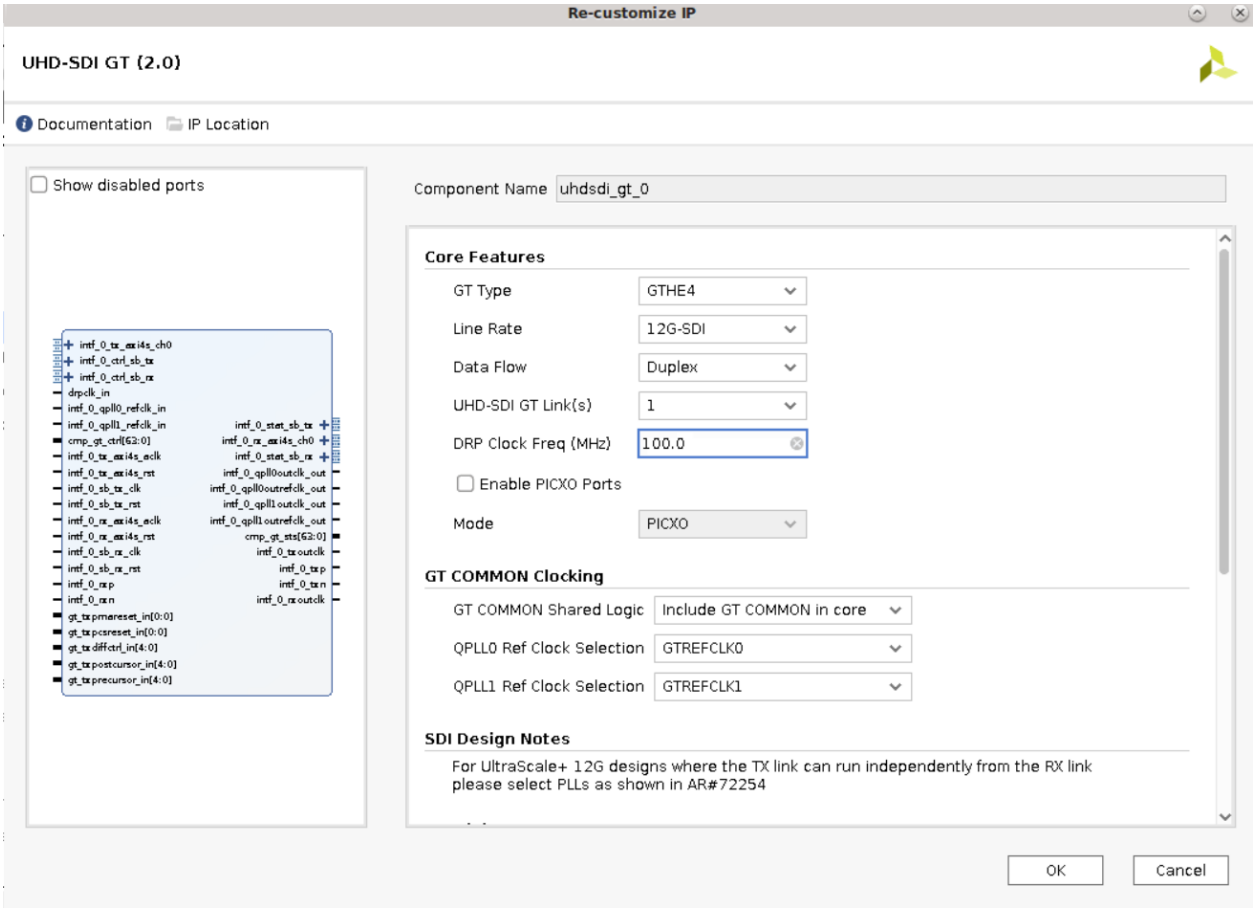
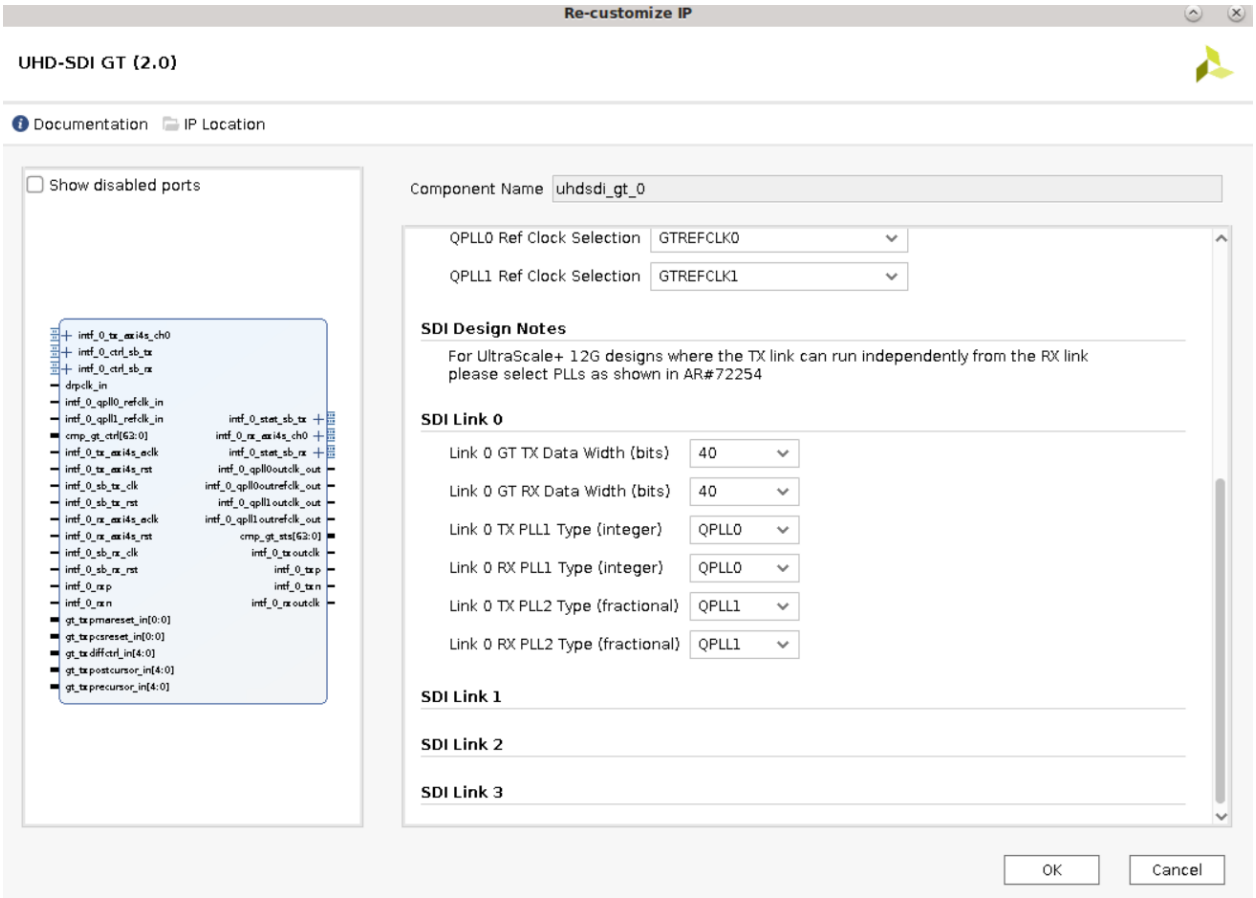


Figure 6: **UHD-SDI GT IP Configuration**



- **Component Name:** The Component Name is the base name of the output files generated for this core.

> **IMPORTANT!** *The name must begin with a letter and be composed of the following characters: a to z, A to Z, 0 to 9 and "_".*

Core Parameters

- **GT Type:** Select the GT type. Available options are:
  - GTHE4 (Default)
  - GTYE4
- **Data Flow:** Select the data flow direction. Available options are:
  - Duplex (Default)
  - RX-Only

  Unlike Duplex configuration, the RX-Only selection generates the core without GT TX ports.

Note: Xilinx UHD-SDI TX subsystem provides an option to generate TX-only example design with PICXO which enables Xilinx UHD-SDI GT core to use with TX-Only data flow option. However, UHD-SDI GT IP core does not provide this option in the core configuration tab.

- **Line Rate:** Select the appropriate line rate. Available options are:
  - 12G-SDI
  - 6G-SDI
  - 3G-SDI
- **UHD-SDI GT Link(s):** Select the number of link(s). Available options are:
  - 1 (Default)
  - 2
  - 3
  - 4
- **DRP Clock Freq:** Provide the DRP clock frequency in MHz. 100 MHz is the default.
- **Enable PIXCO Ports:** Select this option to use the pixco_fraco IP core in your system.
- **GT COMMON Shared Logic:** This option places GT COMMON within the IP Core:
  - Include GT COMMON in core (Default)
- **QPLL0 Ref Clock Selection:** Select the reference clock input source for QPLL0. Available options are:
  - GTREFCLK0 (Default)
  - GTREFCLK1
  - GTNORTHREFCLK0
  - GTNORTHREFCLK1
  - GTSOUTHREFCLK0
  - GTSOUTHREFCLK1
- **QPLL1 Ref Clock Selection:** Select the reference clock input source for QPLL1. Available options are:
  - GTREFCLK0 (Default)
  - GTREFCLK1
  - GTNORTHREFCLK0
  - GTNORTHREFCLK1
  - GTSOUTHREFCLK0

- GTSOUTHREFCLK1

***Note*:** SDI Design: For UltraScale+ 12G designs where the TX link can run independently from the RX link, please select PLLs as shown in AR#72254

The following parameters configure clocking for SDI Link 0:

- **Link 0 TX Data Width (bits):** Select the Link 0 TX data path width used to configure the transceiver TX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI TX subsystem.
  - 40 (default)
  - 20
- **Link 0 RX Data Width (bits):** Select the Link 0 RX data path width used to configure the transceiver RX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI RX subsystem.
  - 40 (default)
  - 20
- **Link 0 TX PLL1 Type(integer):** Select the QPLL for TX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL

***Note*:** In the case of multi-link selection, if Link0 selects CPLL, then all remaining links only support CPLL for TX PLL.

- **Link 0 RX PLL1 Type(integer):** Select the QPLL for RX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
- **Link 0 TX PLL2 Type(fractional):** Select the QPLL for TX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 0 RX PLL2 Type(fractional):** Select the QPLL for RX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0

- QPLL1

The following parameters configure clocking for SDI Link 1:

- **Link 1 TX Data Width (bits):** Select the Link 1 TX data path width used to configure the transceiver TX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI TX subsystem.
  - 40 (default)
  - 20
- **Link 1 RX Data Width (bits):** Select the Link 1 RX data path width used to configure the transceiver RX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI RX subsystem.
  - 40 (default)
  - 20
- **Link 1 TX PLL1 Type(integer):** Select the QPLL for TX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 1 RX PLL1 Type(integer):** Select the QPLL for RX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
- **Link 1 TX PLL2 Type(fractional):** Select the QPLL for TX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 1 RX PLL2 Type(fractional):** Select the QPLL for RX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1

The following parameters configure clocking for SDI Link 2:

- **Link 2 TX Data Width (bits):** Select the Link 2 TX data path width used to configure the transceiver TX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI TX subsystem.
  - 40 (default)
  - 20
- **Link 2 RX Data Width (bits):** Select the Link 2 RX data path width used to configure the transceiver RX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI RX subsystem.
  - 40 (default)
  - 20
- **Link 2 TX PLL1 Type(integer):** Select the QPLL for TX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 2 RX PLL1 Type(integer):** Select the QPLL for RX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
- **Link 2 TX PLL2 Type(fractional):** Select the QPLL for TX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 2 RX PLL2 Type(fractional):** Select the QPLL for RX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1

The following parameters configure clocking for SDI Link 3:

- **Link 3 TX Data Width (bits):** Select the Link 3 TX data path width used to configure the transceiver TX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI TX subsystem.
  - 40 (default)

  - 20
- **Link 3 RX Data Width (bits):** Select the Link 3 RX data path width used to configure the transceiver RX data path. Select 20 when 3G-SDI or HD-SDI is selected in the SMPTE UHD-SDI RX subsystem.
  - 40 (default)
  - 20
- **Link 3 TX PLL1 Type(integer):** Select the QPLL for TX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 3 RX PLL1 Type(integer):** Select the QPLL for RX UHD-SDI integer line rate data path. Available options are:
  - QPLL0
  - QPLL1
- **Link 3 TX PLL2 Type(fractional):** Select the QPLL for TX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1
  - CPLL
- **Link 3 RX PLL2 Type(fractional):** Select the QPLL for RX UHD-SDI fractional line rate data path. Available options are:
  - QPLL0
  - QPLL1

User Parameters

The following table shows the relationship between the fields in the Vivado® IDE and the user parameters (which can be viewed in the Tcl Console).

Table 16: **Vivado IDE Parameter to User Parameter Relationship**

Vivado IDE Parameter	User Parameter	Default Value
Core Parameters		
GT Type	C_GT_TYPE	GTHE4

Table 16: **Vivado IDE Parameter to User Parameter Relationship** *(cont'd)*

Vivado IDE Parameter	User Parameter	Default Value
Data Flow	C_DATA_FLOW	Duplex
LINE RATE	C_LINE_RATE	12G-SDI
SDI link(s)	C_SDI_LINKS	1
GT COMMON Shared Logic	SupportLevel	1 (include GT COMMON in the core)
GT QPLL0 Ref Clock Selection	C_QPLL0_Refclk_Sel	GTREFCLK0
GT QPLL1 Ref Clock Selection	C_QPLL1_Refclk_Sel	GTREFCLK1
DRP Clock Frequency	C_DRP_CLK_FREQ	100.0
LINE_RATE	C_LINE_RATE	12G-SDI
Enable_PICXO_Ports	C_Enable_PICXO_Ports	False
MODE	C_SDI_MODE	PICXO
SDI Link 0		
Link 0 TX PLL1 Type	C_Tx_PLL_Selection_INTF_0	No default value is assigned. User selection is mandatory.
Link 0 RX PLL1 Type	C_Rx_PLL_Selection_INTF_0	
Link 0 TX PLL2 Type	C_Tx_PLL2_Selection_INTF_0	
Link 0 RX PLL2 Type	C_Rx_PLL2_Selection_INTF_0	
SDI Link 1		
Link 1 TX PLL1 Type	C_Tx_PLL_Selection_INTF_1	No default value is assigned. User selection is mandatory
Link 1 RX PLL1 Type	C_Rx_PLL_Selection_INTF_1	
Link 1 TX PLL2 Type	C_Tx_PLL2_Selection_INTF_1	
Link 1 RX PLL2 Type	C_Rx_PLL2_Selection_INTF_1	No default value is assigned. User selection is mandatory
SDI Link 2		
Link 2 TX PLL1 Type	C_Tx_PLL_Selection_INTF_2	No default value is assigned. User selection is mandatory
Link 2 RX PLL1 Type	C_Rx_PLL_Selection_INTF_2	
Link 2 TX PLL2 Type	C_Tx_PLL2_Selection_INTF_2	
Link 2 RX PLL2 Type	C_Rx_PLL2_Selection_INTF_2	
SDI Link 3		
Link 3 TX PLL1 Type	C_Tx_PLL_Selection_INTF_3	No default value is assigned. User selection is mandatory
Link 3 RX PLL1 Type	C_Rx_PLL_Selection_INTF_3	
Link 3 TX PLL2 Type	C_Tx_PLL2_Selection_INTF_3	
Link 3 RX PLL2 Type	C_Rx_PLL2_Selection_INTF_3	

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

Required Constraints

This section defines the additional constraint requirements for the core. Constraints are provided with a Xilinx Design Constraints (XDC) file. The XDC file is provided with the HDL example design to give a starting point for constraints in your design.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

`drpclk_in` should be specified using the following command:

```
create_clock -name drp_clk -period 10.000 [get_ports drpclk_in]
```

This constraint defines the frequency of `drpclk_in` that is supplied to DRP control logic and connected to DRPCLK of GT CHANNEL primitive.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

The UHD-SDI GT core does not have the ability to constrain the transceiver. Constraining the `txp`, `txn`, `rxp`, and `rxn` ports of GTHE4_CHANNEL/GTYE4_CHANNEL is sufficient for transceiver placement.

I/O Standard and Placement

The UHD-SDI GT core generates clock constraints and necessary false path constraints. But it does not constrain GT locations and reference clock locations. See the respective board user guide or board schematics for LOC and add the constraints to the top level XDC file.

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Appendix A

Verification, Compliance, and Interoperability

Hardware Testing

For a list of tested boards, see the Example Design chapter in *SMPTE UHD-SDI Transmitter Subsystem Product Guide* (PG289) and *SMPTE UHD-SDI Receiver Subsystem Product Guide* (PG290).

XILINX

Appendix B

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with an error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

IMPORTANT! *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support. The Xilinx Community Forums are also available where members can learn, participate, share, and ask questions about Xilinx solutions.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Technical Support

Xilinx provides technical support on the Xilinx Community Forums for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To ask questions, navigate to the Xilinx Community Forums.

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado® debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the debug feature for debugging the specific problems.

- **GT Clocking:**
  - Make sure PLLs are getting reset before starting the IP
  - Monitor the PLL LOCK signal.
  - Verify that PLL input clock frequency is of expected value.
  - It is mandatory to reset the PLL if clock input to PLL is stopped or unstable.

- See AR 57738 for debugging GT reference clock issues.
- Make sure to use PLL default settings from latest GT Wizard IP core based on target device.
- Check the voltage rails on the transceivers. See AR 57737 for more information.
- Measure RXOUTCLK is of expected frequency.
- Make sure `RXOUTCLK` of the transceiver is the clock driving `rx_usrclk`, `RXUSRCLK`, and `RXUSRCLK2`.
- Monitor `RXBUFFSTATUS[2:0]` for overflow and underflow errors.

- **GT Initialization:**
  - GTRXRESETDONE is asserted High after GT completes initialization.
  - Make sure GT is not reset during normal operation.
  - See AR 59435 for more information on debugging GT reset problems.
  - Follow the recommended GT reset sequence.

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

1. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)

2. *Vivado Design Suite User Guide: Designing with IP* (UG896)
3. *Vivado Design Suite User Guide: Getting Started* (UG910)
4. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
5. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
6. *Vivado Design Suite User Guide: Implementation* (UG904)
7. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
8. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
9. *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS923)
10. *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
11. *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics* (DS925)
12. *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926)
13. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)
14. *SMPTE UHD-SDI Transmitter Subsystem Product Guide* (PG289)
15. *SMPTE UHD-SDI Receiver Subsystem Product Guide* (PG290)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
01/21/2021 Version 2.0	
Unsupported Features	Added information about multi-link support.
Port Descriptions	Added information about `cmp_gt_ctrl` input ports and `cmp_gt_sts` output ports.
Core Configuration Tab	Added information about core parameters.
06/03/2020 Version 1.0	
Initial release.	N/A

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