Utility Bus Split (v1.00a)

DS484 December 2, 2009 **Product Specification**

Introduction

The Utility Bus Split core splits a bus into smaller buses using the Xilinx Platform Studio (XPS).

The core splits one input bus into two output buses which serve as glue logic between peripherals.

Features

- The Split Operation has the following features:
  - Configurable size of the input and output vectors

LogiCORE™ IP Facts	
Core Specifics	
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Spartan-6, Virtex®-4 /4Q/4QV, Virtex-5/5FX, Virtex-6/6CX
Resources Used	
Not Applicable	
Provided with Core	
Documentation	Product Specification
Design File Formats	VHDL
Constraints File	EDK TCL Generated
Verification	N/A
Instantiation Template	EDK
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 11.4 or later
Verification	ModelSim PE/SE 6.4b or later
Simulation	ModelSim PE/SE 6.4b or later
Synthesis	XST
Support	
Provided by Xilinx, Inc.	

Functional Description

Figure 1 shows a Utility Bus Split in a system.

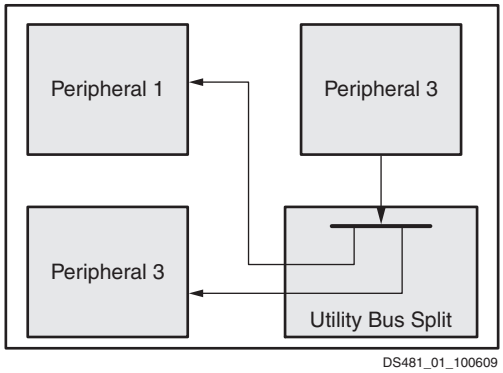

Figure 1: **Utility Bus Split in a System**

Utility Bus Split Parameters

Table 1: **Utility Bus Split Parameters**

Parameter	Description	Default Value	Type
C_SIZE_IN	The vector size of input bus.	8	integer
C_LEFT_POS	The left bit position of the Out1 output bus. The maximum value of C_LEFT_POS is C_SPLIT-1.	0	integer
C_SPLIT	First bit of the Out2 output bus The minimum value of C_SPLIT is 1. The maximum value of C_SPLIT is C_SIZE_IN-1.	4	integer

Allowable Parameter Combinations

The only restrictions between parameters is that C_LEFT_POS must be smaller than C_SPLIT, and both of them must be smaller than C_SIZE_IN.

Utility Bus Split I/O Signals

Table 2: **Utility Bus Split I/O Signals**

Signal	Interface	I/O	Description
Sig	None	I	Input bus
Out1	None	O	Output bus1 after split
Out2	None	O	Output bus2 after split

Parameter-Port Dependencies

Table 3: Port and Parameter Dependencies

Name	Affects	Depends	Relationship Description
Design Parameters			
C_SIZE_IN	Sig	0 to C_SIZE_IN-1	Scale width of input bus
C_SIZE_IN	Out2	C_SPLIT to C_SIZE_IN-1	Least (1) significant bit of Out2 bus
C_LEFT_POS	Out1	C_LEFT_POS to C_SPLIT-1	Most (1) significant bit of Out1 bus
C_SPLIT	Out1	C_LEFT_POS to C_SPLIT-1	Least (1) significant bit of Out1 bus
C_SPLIT	Out2	C_SPLIT to C_SIZE_IN-1	Most (1) significant bit of Out2 bus
Port Signals			
Sig		C_SIZE_IN	Scale width of input bus
Out1		C_LEFT_POS	Most (1) significant bit of Out1 bus
Out1		C_SPLIT	Least (1) significant bit of Out1 bus
Out2		C_SPLIT	Most (1) significant bit of Out2 bus
Out2		C_SIZE_IN	Least (1) significant bit of Out2 bus

1. Assuming reverse big-endian bit ordering.

Utility Bus Split Register Descriptions

There are no registers in this core.

Utility Bus Split Interrupt Descriptions

There are no interrupts associated with this core.

Utility Bus Split Block Diagram

The Utility Bus Split block diagram is shown in Figure 2.

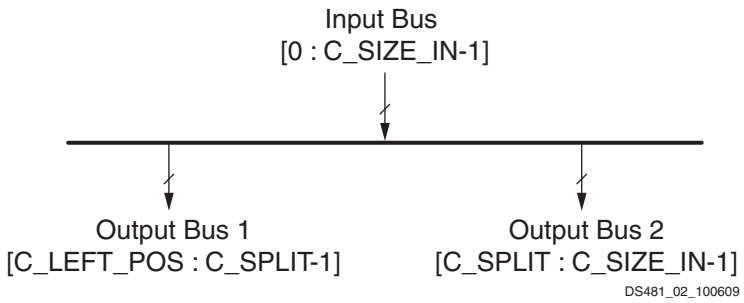

Figure 2: **Utility Bus Split Block Diagram**

Design Implementation

Design Tools

The Utility Bus Split design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Utility Bus Split.

Target Technology

The target technology is an FPGA listed in Supported Device Family field of the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

This core does not contain any logic. There are no performance benchmarks available.

Specification Exceptions

Not applicable

Reference Documents

None

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Description of Revisions
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE IP Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.
8/17/04	1.3	Updated for EDK 6.3. Updated trademarks and supported family device listing.
9/20/04	1.4	Corrected C_LEFT_POS description in parameter table. Updated to new data sheet template
04/24/09	1.5	Replaced references to supported device families and tool name(s) with hyperlinks to PDF files. Updated trademark information.
12/2/09	1.6	Listed supported devices families in LogiCORE Table; added Spartan-6 and Virtex-6 support, converted to new DS template.

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