

Introduction

The Utility IO Multiplexer module provides a multiplexing function between two IO vectors to one IO vector.

Features

- Provides 2 to 1 multiplexing of IO vectors
- Configurable size of vectors

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Spartan-6, Virtex®-4 /4Q/4QV, Virtex-5/5FX, Virtex-6/6CX	
Resources Used		
	Min	Max
LUTs	1	2*C_SIZE
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	EDK	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.4 or later	
Verification	ModelSim PE/SE 6.4b or later	
Simulation	ModelSim PE/SE 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The block diagram for the Utility IO Multiplexer is shown in [Figure 1](#).

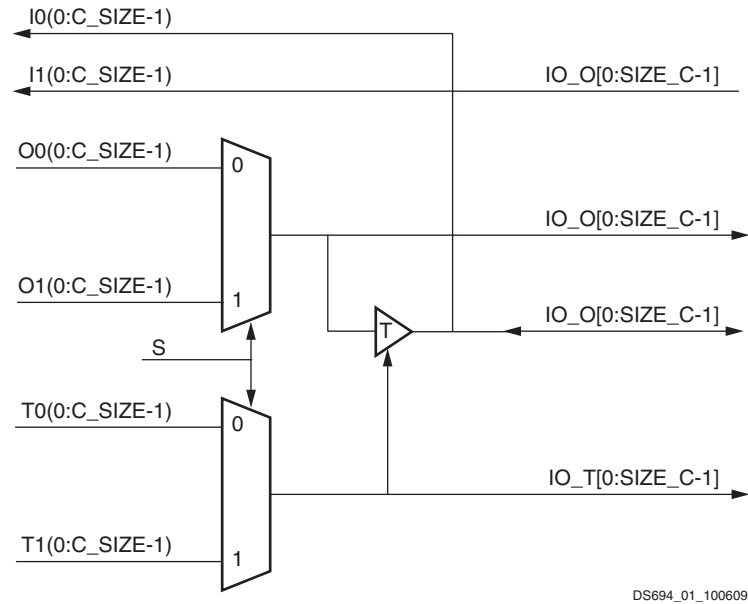


Figure 1: Utility IO Multiplexer Block Diagram

Utility IO Multiplexer I/O Signals

The Utility IO Multiplexer provides a way of selecting which of two IO vectors should be connected to one IO vector. The size of the vectors is determined by the parameter `C_SIZE`, which has the minimum value 1.

Table 1: Utility I/O Multiplexer Signal Descriptions

Signal Name	I/O	Initial State	Description
I0	O		Input vector 0 [0:C_SIZE-1]
O0	I		Output vector 0 [0:C_SIZE-1]
T0	I		Tristate disable vector 0 [0:C_SIZE-1]
I1	O		Input vector 1 [0:C_SIZE-1]
T1	I		Tristate disable vector 1 [0:C_SIZE-1]
S	I		Input select signal. 0 : O0 and T0 drives, IO_O and IO_T respectively 1 : O1 and T1 drives, IO_O and IO_T respectively
IO_I	I		IO input vector [0:C_SIZE-1]
IO_O	O		IO output vector [0:C_SIZE-1]
IO_T	O		IO tristate disable vector [0:C_SIZE-1]
IO	IO		IO tristate vector [0:C_SIZE-1]

Design Parameters

The parameters defined for the Utility IO Multiplexer module are listed and described in [Table 2](#).

Table 2: Utility IO Multiplexer Parameters

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_SIZE	The size of the vectors	natural	8	integer

Parameter-Port Dependencies

The affects of setting various parameters is shown in [Table 3](#).

Table 3: Utility IO Multiplexer Port and Parameter Dependencies

Parameter	Port	Description
C_SIZE	I0, O0, T0, I1, O1, T1, IO_I, IO_O, IO_T, IO	Size of vectors

Design Implementation

Target Technology

The target technology is an FPGA listed in [Supported Device Family](#) field of the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

The device utilization depends on the size of the vectors being multiplexed.

Specification Exceptions

Not applicable

Reference Documents

None

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Description of Revisions
6/13/08	1.0	Initial Xilinx release.
4/24/09	1.1	Replaced references to supported device families, tool name(s), and parameter values with hyperlink to PDF file; converted to current DS template.
12/2/09	1.2	Listed supported devices families in LogiCORE Table; added Spartan-6 and Virtex-6 support, converted to new DS template.

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