Utility Vector Logic (v1.00a)

DS481 December 2, 2009 **Product Specification**

Introduction

The Utility Vector Logic core takes two vector operands and bit wise applies a logic function to generate a single vector result. This core is intended as glue logic between peripherals.

Features

- Configurable size of the vectors
- Configurable logical operation on vectors

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Spartan-6, Virtex®-4 /4Q/4QV, Virtex-5/5FX, Virtex-6/6CX	
Resources Used		
	Min	Max
Slices	1	16 (1)
LUTs	1	32 (1)
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.4 or later	
Verification	ModelSim PE/SE 6.4b or later	
Simulation	ModelSim PE/SE 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

1. For C_SIZE=32. The count increases with C_SIZE.

Functional Description

Figure 1 shows a Utility Vector Logic in a system.

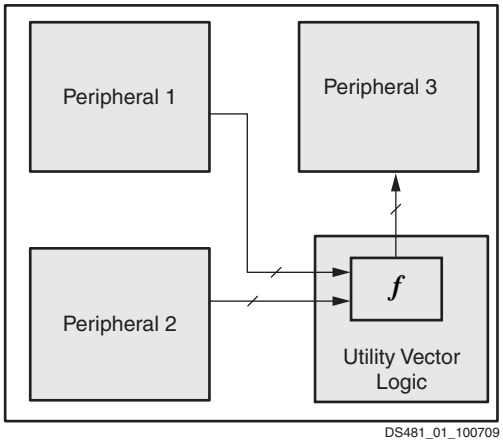

Figure 1: **Utility Vector Logic in a System**

Utility Vector Logic Parameters

Table 1: **Utility Vector Logic Parameters**

Parameter	Description	Type
C_OPERATION	The vector operation to perform. The supported operations are: “and”, “or”, “xor”, “not”	String
C_SIZE	The size of the vectors. Notice that the width of Op1, Op2 and Res must be equal. The minimum value of this parameter is 1.	Integer

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations for this core.

Utility Vector Logic I/O Signals

Table 2: **Utility Vector Logic I/O Signals**

Signal	Interface	I/O	Description
Op1	None	I	Operand 1 vector [0 : C_SIZE-1]
Op2	None	I	Operand 2 vector [0 : C_SIZE-1]. Unused when C_OPERATION = “not”
Res	None	O	Result vector [0 : C_SIZE-1]

Parameter-Port Dependencies

Table 3: Port and Parameter Dependencies

Name	Affects	Depends	Relationship Description
Design Parameters			
C_SIZE	Op1	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Op2	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Res	0 to C_SIZE-1	Scale width of output bus
Port Signals			
Op1		C_SIZE	Scale width of input bus
Op2		C_SIZE	Scale width of input bus
Res		C_SIZE	Scale width of output bus

Utility Vector Logic Register Descriptions

There are no registers in this core.

Utility Vector Logic Interrupt Descriptions

There are no interrupts associated with this core.

Utility Vector Logic Block Diagram

The Utility Vector Logic block diagram is shown in Figure 2.

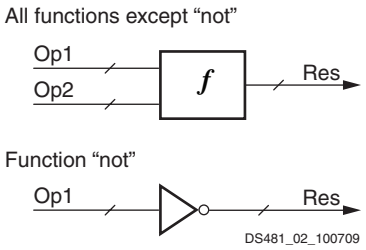

Figure 2: **Utility Vector Logic Block Diagram**

Design Implementation

Design Tools

The Utility Vector Logic design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Utility Vector Logic device.

Target Technology

The target technology is an FPGA listed in Supported Device Family field of the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

Table 4: **Utility Vector Logic Resource Utilization**

Parameter Value		Device Resources		
C_OPERATION	C_SIZE	Slices	Slice Flip-Flops	4-Input LUTs
“and”	8	4	0	8
“xor”	12	6	0	12

There are no performance benchmarks available.

Specification Exceptions

Not applicable

Reference Documents

None

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Description of Revisions
3/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
7/15/04	1.2	Minor corrections and updates.
8/17/04	1.3	Updated for EDK 6.3. Updated trademarks and supported family device listing.
9/22/04	1.4	Updated to use new data sheet template.
4/24/09	1.5	Replaced references to supported device families and tool names with hyperlink to PDF file.
12/2/09	1.6	Listed supported devices families in LogiCORE Table; added Spartan-6 and Virtex-6 support, converted to new DS template.

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