LogiCORE IP Virtex-5 FPGA RocketIO GTX Transceiver Wizard v1.7

DS601 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-5 FPGA RocketIO™ GTX Transceiver Wizard automates the task of creating HDL wrappers (1) to configure the high-speed serial GTX transceivers in the Virtex-5 FXT and TXT sub-families. The menu-driven interface allows one or more GTX transceivers to be configured using pre-defined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols. The Wizard produces a wrapper, an example design, and a test bench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Virtex-5 family RocketIO GTX transceivers
- Users can configure Virtex-5 family GTX transceivers to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Templates include support for the following specifications: Aurora (8B/10B and 64B/66B), CPRI™, Fibre Channel 1x, Gigabit Ethernet, HD-SDI, OBSAI, OC3, OC12, OC48, PCI EXPRESS® (PCIe®) generation I and II, SATA 1.5 Gbps, SATA 3 Gbps, Serial RapidIO, and XAUI
- Automatically configures analog settings
- Each custom wrapper includes example design, test bench; and both implementation and simulation scripts
- Supports 64B/66B and 64B/67B encoding/decoding

LogiCORE IP Facts	
Core Specifics	
Supported Device Family	Virtex-5 (1) FXT/TXT
Provided with Core	
Documentation	Product Specification Getting Started Guide
Design File Formats	Verilog and VHDL
Constraints File	.ucf (user constraints file)
Verification	Example Design and Test Bench
Instantiation Template	Verilog or VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 12.1 (2)
Verification	ISim 12.1 Mentor Graphics ModelSim 6.5c and above
Simulation	ISim 12.1 Mentor Graphics ModelSim 6.5c and above
Synthesis	XST 12.1 Synopsys Synplify Pro D-2009.12
Support	
Provided by Xilinx, Inc. at http://www.xilinx.com/support	

1. For more information on the Virtex-5 devices, see the *Virtex-5 Family Overview* [Ref 2]
2. ISE Service Packs can be downloaded from http://www.xilinx.com/support/download.htm

1. See the *LogiCORE IP Virtex-5 FPGA RocketIO GTX Transceiver Wizard Getting Started Guide* [Ref 1] for an overview of the procedure to create a wrapper.

Functional Overview

Figure 1 outlines the steps required to configure GTX transceivers using the Wizard. Start the CORE Generator™ tool and select the RocketIO GTX Transceiver Wizard, then follow the steps outlined in the chart to configure the transceivers and generate a wrapper that includes an accompanying example design. If you use an existing template with no changes, click Generate. If you are modifying a standard template or starting from scratch, proceed through the Wizard and adjust the settings as needed.

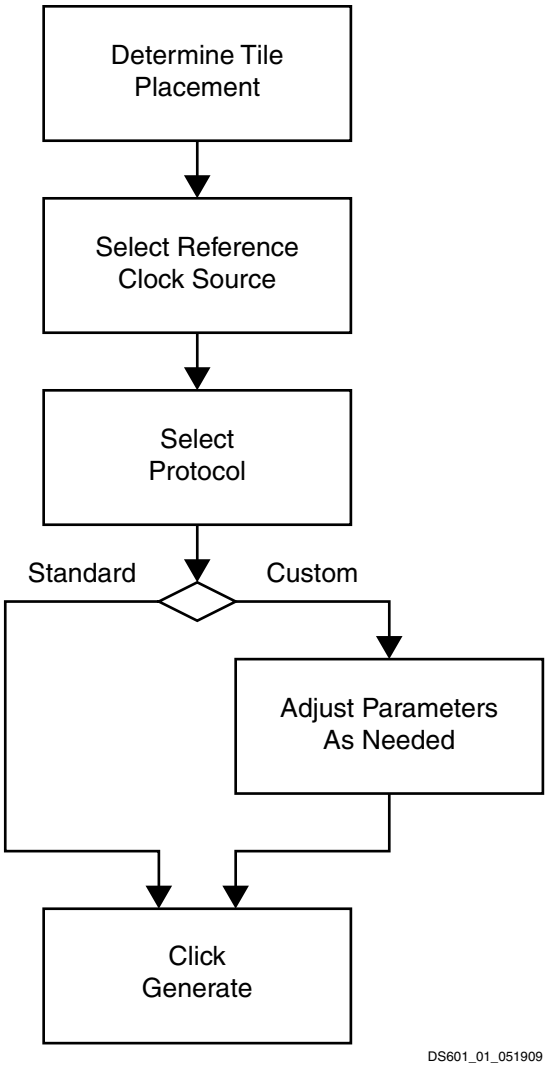

Figure 1: **GTX Wizard Configuration Steps**

See the *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* [Ref 3] for details on the various transceiver features and parameters available.

Wrapper Overview

Figure 2 shows the block diagram of the wrapper, example design, and test bench produced by the Wizard.

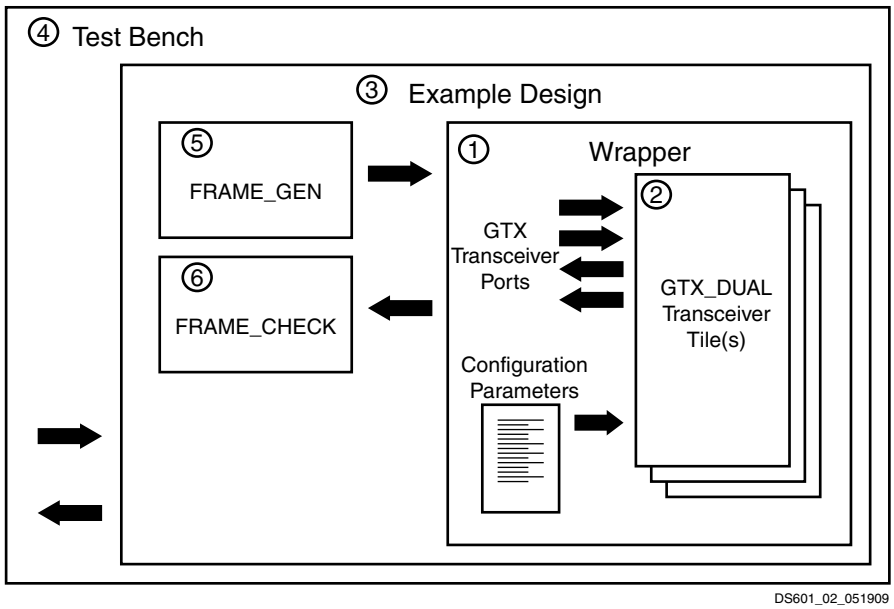

Figure 2: **Wrapper Block Diagram**

The wrapper comprises six components:

1. Wrapper: The specific GTX transceiver configuration parameters set with the Wizard.
2. GTX_DUAL Transceiver Tile(s): Instantiated tiles selected with the Wizard.
3. Example Design: Temporary top-level design that will be replaced with the actual application.
4. Test Bench: Top-level test bench to aid in simulation of the design.
5. FRAME_GEN Module: Generates a user-definable data stream for simulation analysis.
6. FRAME_CHECK Module: Tests for correct transmission of data stream for simulation analysis.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Virtex-5 FPGA RocketIO™ GTX Transceiver Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.1 or higher. For more information, please visit the Architecture Wizards web page. Information about additional Xilinx LogiCORE

modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. UG204: *LogiCORE IP Virtex-5 FPGA RocketIO GTX Transceiver Wizard Getting Started Guide* for a general overview of the wrapper creation procedure.
2. DS100: *Virtex-5 Family Overview*
3. UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
03/24/08	1.2	Initial Xilinx release.
03/24/08	1.2.1	Added Xilinx support link.
04/25/08	1.3	Updated version numbers.
06/26/08	1.4	Revised version numbers. "Features," page 1 bullet item 3: Added OBSAI, PCIe generation I and II.
06/27/08	1.4.1	Updated release date and trademarks.
09/19/08	1.5	Updated version numbers.
06/24/09	1.6	Updated core and tools versions. Added support for the Virtex-5 TXT family.
04/19/10	1.7	Wizard v1.7 release. Updated tools and version numbers. Added support for Aurora (8B/10B and 64B/66B) and CPRI. Added "Ordering Information."

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