LogiCORE IP XAUI v9.2

DS266 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP XAUI core is a high-performance, low pin count 10-Gbps interface intended to allow physical separation between data-link layer and physical layer devices in a 10-Gigabit Ethernet system.

The XAUI core implements a single-speed full-duplex 10-Gbps Ethernet eXtended Attachment Unit Interface (XAUI) solution for the Xilinx® Virtex®-6, Virtex-5, Virtex-4, and Spartan®-6 FPGA families.

The Virtex-6, Virtex-5, Virtex-4, and Spartan-6 FPGA families in combination with the XAUI core, enable the design of XAUI-based interconnects whether they are chip-to-chip, over backplanes, or connected to 10 Gigabit optical modules.

Features

- Designed to 10-Gigabit Ethernet *IEEE 802.3-2008* specification
- Uses four transceivers at 3.125 Gbps line rate to achieve 10-Gbps data rate
  - Virtex-6 FPGA GTX Transceiver
  - Virtex-5 FPGA RocketIO™ GTP or GTX Transceiver
  - Virtex-4 FPGA Multi-Gigabit Transceiver (MGT)
  - Spartan-6 FPGA GTP transceiver
- Implements DTE XGXS, PHY XGXS, and 10GBASE-X PCS in a single netlist
- Uses Virtex-6, Virtex-5, Virtex-4, and Spartan-6 FPGA Digital Clock Management to implement optional XGMII interface clocking
- Uses Virtex-6, Virtex-5, Virtex-4, and Spartan-6 FPGA DDR I/O primitives for the optional XGMII interface
- Elastic buffering of inbound XGMII data (optional)
- Uses device-specific transceivers for the XAUI interface
- *IEEE 802.3-2008* clause 45 MDIO interface (optional)
- *IEEE 802.3-2008* clause 48 State Machines (optional for Virtex-5, Virtex-6, and Spartan-6 FPGAs)
- Supports 10-Gigabit Fibre Channel (10-GFC) XAUI data rates and traffic
- Available under the Xilinx End User License Agreement

LogiCORE IP Facts				
Core Specifics				
Supported Device Family [1]	Virtex-6 CXT/LXT/SXT/HXT Virtex-5 FXT/LXT/SXT/TXT Virtex-4 FX Spartan-6 LXT			
Resources Used[2]	Slices	LUTs	FFs	Block RAMs
	917	1327	700	0
Special Features	Delivered through CORE Generator™			
Provided with Core				
Documentation	Product Specification Getting Started Guide User Guide			
Design File Formats	NGC netlist			
Constraints File	UCF			
Verification	VHDL Test Bench Verilog Test Fixture			
Example design	VHDL and Verilog			
Additional Items	UniSim-based Simulation Models			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® v12.1 software			
Simulation Tools[3]	Mentor Graphics ModelSim v6.5c and above Cadence Incisive Enterprise Simulator (IES) v9.2 and above Synopsys VCS and VCS MX 2009.12 and above			
Support				
Provided by Xilinx, Inc.@ www.xilinx.com/support				

1. For the complete list of supported devices, see the 12.1 release notes for this core.
2. Please see Table 10-14 for resource requirements based on configuration and device.
3. All Virtex family designs require a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. The simulation tools listed in the Facts table are supported. For VHDL simulation, a mixed HDL license is required.

Overview

XAUI is a four-lane, 3.125 Gbps-per-lane serial interface. Each lane is a differential pair carrying current mode logic (CML) signaling, and the data on each lane is 8B/10B encoded before transmission. Special code groups are used to allow each lane to synchronize at a word boundary and to de-skew all four lanes into alignment at the receiving end. The XAUI standard is fully specified in clauses 47 and 48 of the 10-Gigabit Ethernet *IEEE 802.3-2008* specification.

The XAUI standard was initially developed as a means to extend the physical separation possible between MAC and PHY components in a 10-Gigabit Ethernet system distributed across a circuit board, and to reduce the number of interface signals in comparison with the XGMII (10-Gigabit Ethernet Media Independent Interface).

Applications

Figure 1 shows the XAUI core connecting a 10-Gigabit Ethernet MAC to a 10-Gigabit XPAK optical module.

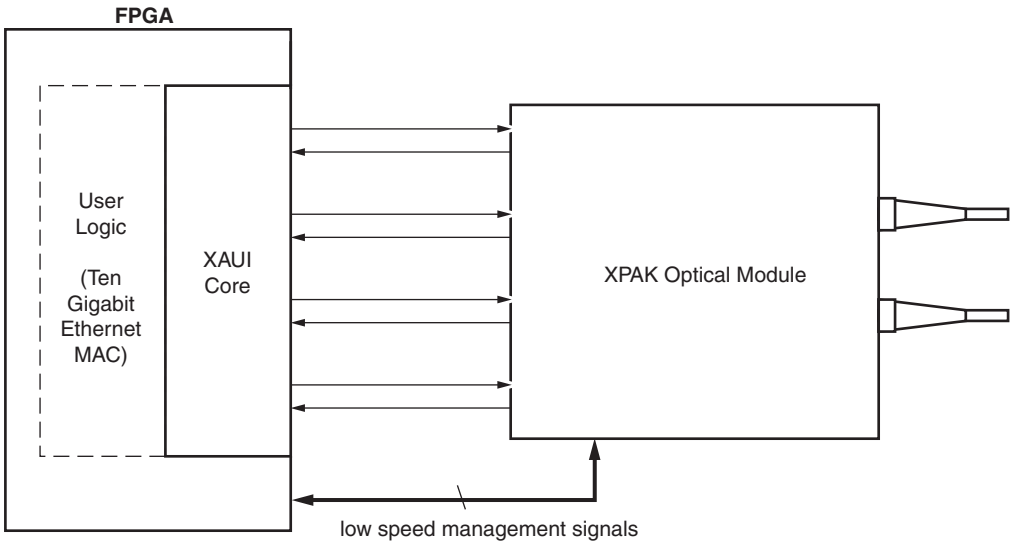

Figure 1: **XAUI Connecting a 10-Gigabit Ethernet MAC to an Optical Module**

Since its publication, the applications of XAUI have extended beyond 10-Gigabit Ethernet to backplane and other general high-speed interconnect applications. Figure 2 shows a typical backplane application.

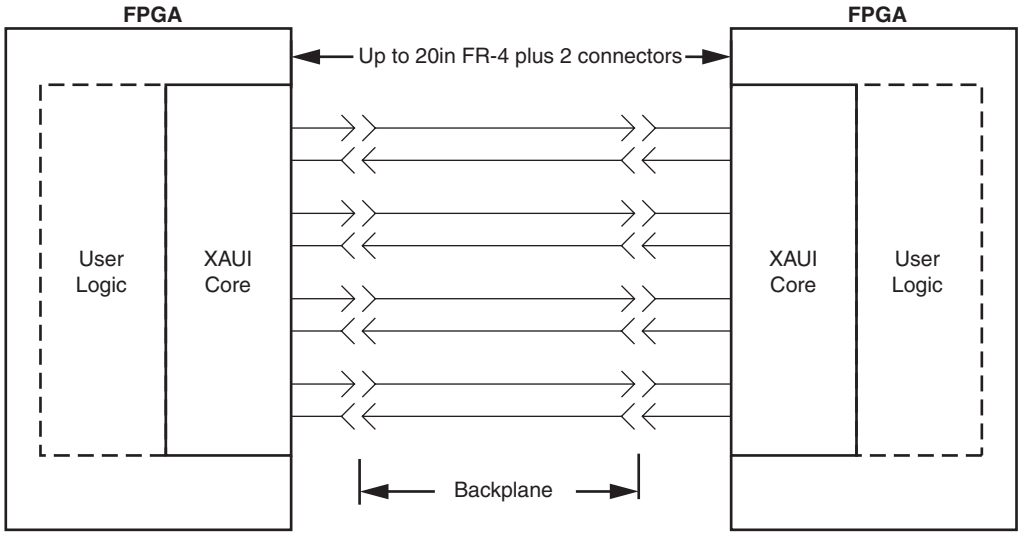

Figure 2: **Typical Backplane Application for XAUI**

Functional Description

Figure 3 shows a block diagram of the XAUI core implementation. The major functional blocks of the core include the following:

- **Client-side XGMII Interface** if necessary, converts 32-bit DDR data into 64-bit SDR data and crosses clock domain for inbound XGMII data using an elastic buffer.
- **Transmit Idle Generation Logic** creates the code groups to allow synchronization and alignment at the receiver.
- **Synchronization State Machine (one per lane)** identifies byte boundaries in incoming serial data.
- **De-skew State Machine** de-skews the 4 received lanes into alignment.
- **Optional MDIO Interface** is a two-wire low-speed serial interface used to manage the core.
- **Four Device-Specific Transceivers** (embedded in the Virtex-6, Virtex-5 or Virtex-4 FPGAs) provide the high-speed transceivers as well as 8B/10B encode and decode, and elastic buffering in the receive data path.

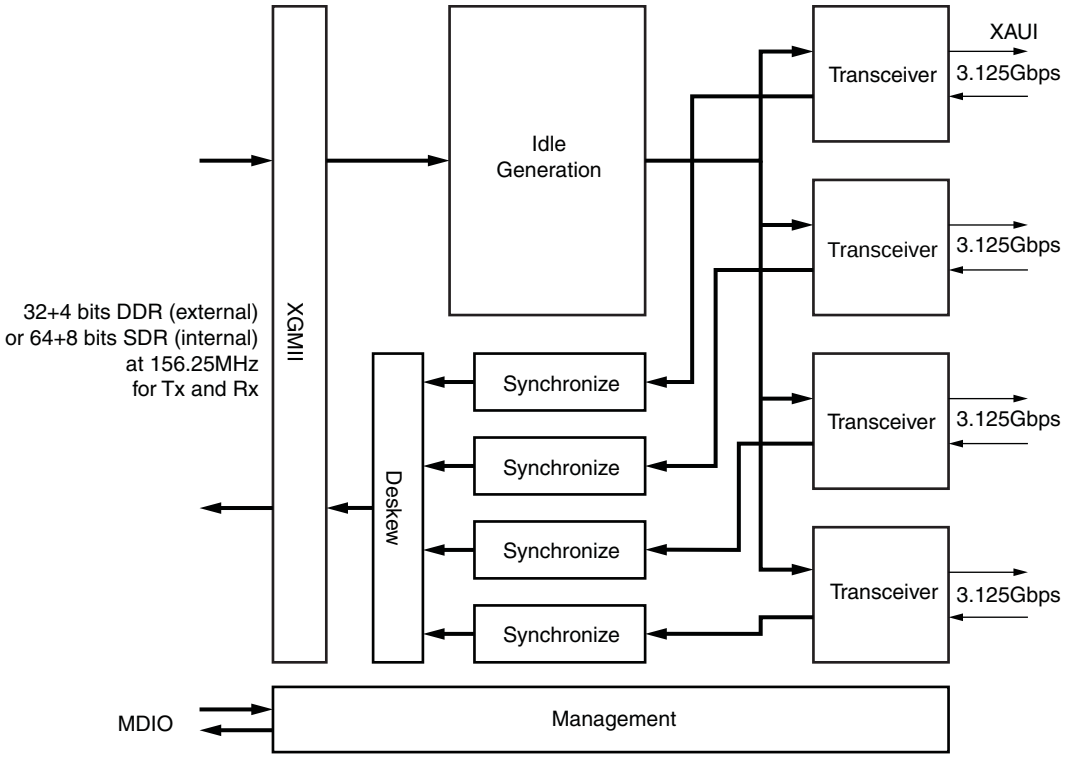

Figure 3: **Implementation of XAUI Core**

The core is implemented with the device-specific transceiver instantiations in the source code rather than in the netlist. This gives you more flexibility in their particular application to use additional device-specific transceiver features and resolve placement issues.

Core Interfaces

XAUI Interface

The XAUI interface consists of four differential transmit and receive pairs plus four low-speed control inputs to indicate the status of an attached optical module. The differential pairs are generated by the device-specific transceiver. The control input signals are connected directly to the core. These signals are described in Table 1.

Table 1: **XAUI Interface Ports**

Signal Name	Direction	Description
`SIGNAL_DETECT[3:0]`	IN	Signals from a 10GBASE-LX4 optical module indicating the optical receivers are illuminated by a signal. If unused, tie this bus to '`1111`.'

Transceiver Interface

The device-specific transceiver interface in the internal connection between the XAUI core netlist and the serial transceivers which provide the XAUI interface. For detailed descriptions of the functions of these signals, see the transceiver user guides. Table 2 describes these signals.

Table 2: **Transceiver Interface Ports**

Signal Name	Direction	Description
MGT_TXDATA	OUT	Data to MGTs
MGT_TXCHARISK	OUT	Control to MGTs
MGT_RXDATA	IN	Data from MGTs
MGT_RXCHARISK	IN	Control from MGTs
MGT_CODEVALID	IN	Code error signals from each MGT
MGT_CODECOMMA	IN	Code comma signals from each MGT
MGT_ENABLE_ALIGN	OUT	Enable comma align signals to each MGT
MGT_ENCHANSYNC	OUT	Enable channel sync signal to the MGTs
MGT_SYNCOK	IN	Sync OK signals from each MGT
MGT_RXLOCK	IN	Receive lock signals from each MGT
MGT_LOOPBACK	OUT	Loopback enable signal to each MGT
MGT_POWERDOWN	IN	Power down signal to each MGT

Client-Side Interface

The client-side interface is a 72-bit (64 data bits and 8 control bits) interface running at 156.25 MHz based on the XGMII standard. It is designed to be easily connected to either user logic within the FPGA or, by using SelectIO™ technology DDR registers in the design top-level, to provide an external 32-bit 312 Mbps DDR XGMII defined in clause 46 of *IEEE 802.3-2008*.

Table 3: **Client-side Interface Ports**

Name	Direction	Description
XGMII_TXD[63:0]	IN	Transmit data, 8 bytes wide
XGMII_TXC[7:0]	IN	Transmit control bits, one bit per transmit data byte.
XGMII_RXD[63:0]	OUT	Received data, 8 bytes wide
XGMII_RXC[7:0]	OUT	Receive control bits, one bit per received data byte.

Figure 4 illustrates transmitting a frame through the client-side interface.

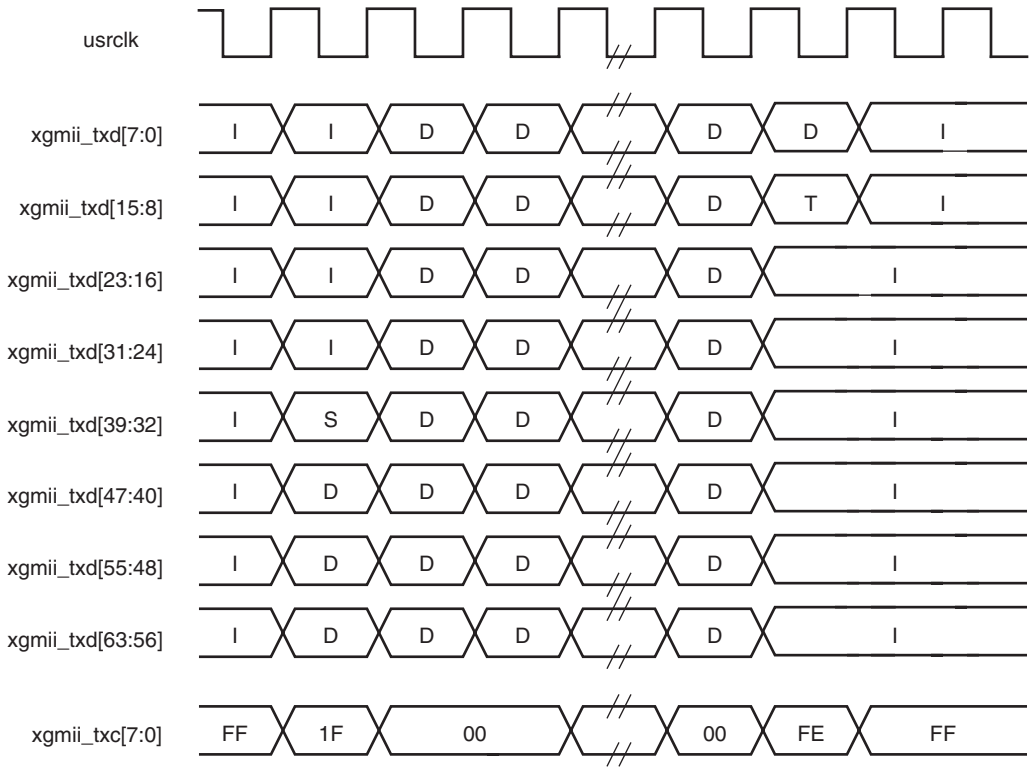

Figure 4: **Transmitting a Frame Through the Client-Side Interface**

Figure 5 illustrates receiving a frame through the client-side interface.

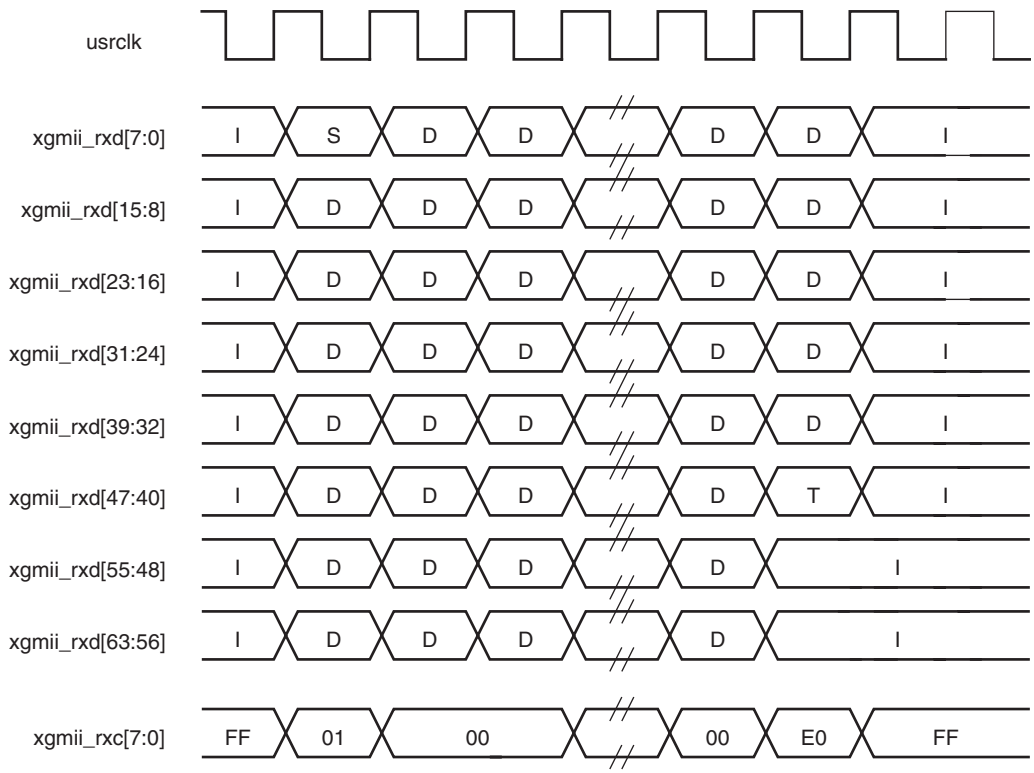

Figure 5: **Receiving a Frame Through the Client-Side Interface**

Management Interface (MDIO)

The MDIO interface is a simple low-speed 2-wire interface for management of the XAUI core, consisting of a clock signal and a bi-directional data signal. The interface is defined in clause 45 of *IEEE 802.3-2008* standard.

In the XAUI core, the MDIO interface is an optional block. If implemented, the bi-directional data signal MDIO is implemented as three unidirectional signals. These can be used to drive a 3-state buffer either in the FPGA IOB or in a separate device.

There are additional signals that control the behavior of the core MDIO interface, specifically to set its position in the MDIO memory map.

Table 4: **MDIO Management Interface Ports**

Signal Name	Direction	Description
MDC	IN	Management clock
MDIO_IN	IN	MDIO input
MDIO_OUT	OUT	MDIO output
MDIO_TRI	OUT	MDIO 3-state. '1' disconnects the output driver from the MDIO bus.
TYPE_SEL[1:0]	IN	Type select. Determines which MDIO Register addresses the core responds to. type_sel = '00' or '01' – 10GBASE-X PCS type_sel = '10' – DTE XS type_sel = '11' – PHY XS See the *XAUI User Guide* for the MDIO Register addresses responded to in each case.
PRTAD[4:0]	IN	MDIO port address. When multiple MDIO-managed ports appear on the same bus, this address can be used to address each one individually.

Configuration and Status Signals

In addition to the pollable MDIO interface, the XAUI core continuously indicates its status on ports as defined in Table 5.

Table 5: **Configuration and Status Vector Ports**

Signal Name	Direction	Description
ALIGN_STATUS	OUT	'1' when the XAUI receiver is aligned across four lanes.
SYNC_STATUS[3:0]	OUT	Each pin is '1' when the respective XAUI lane receiver is synchronized to byte boundaries.
CONFIGURATION_VECTOR[6:0]	IN	Configuration signals for the core. The bits are: Bit 0 - Loopback Bit 1 - Power down transceiver Bit 2 - Reset local fault status Bit 3 - Reset RX link status Bit 4 - Test Enable - '1' transmits test patterns on XAUI TX Bits 6:5 - Test pattern select For a more comprehensive description of these signals, please consult the *XAUI User Guide*. This port only exists on the core if the MDIO interface is omitted.
STATUS_VECTOR[7:0]	OUT	Status indicators for the core. The bits are: Bit 0 - TX local fault Bit 1 - RX local fault Bit 5:2 - Synchronization - identical to SYNC_STATUS[3:0] Bit 6 - Alignment - identical to ALIGN_STATUS Bit 7 - RX link status For a more comprehensive description of these signals, please consult the *XAUI User Guide*. This port only exists on the core if the MDIO interface is omitted.

Clock and Reset

Table 6 describes the clock and reset ports present on the core.

Table 6: **Clock and Reset Ports**

Name	Direction	Description
TX_CLK	IN	This port is only present if the core has been generated including a transmit elastic buffer. This clock is the forwarded reference clock for the source-centred XGMII transmit data. It is used to clock data into the FPGA, and then the data is crossed into the system clock domain by the elastic buffer.
RESET	IN	Synchronous reset for core. The reference clock must be running for the core to emerge from the reset state.
USRCLK	IN	FPGA fabric logic system clock.
MGT_TX_RESET	IN	Connect this to the same signal used to drive the transceiver MGT TXRESET signal.
MGT_RX_RESET	IN	Connect this to the same signal used to drive the transceiver MGT RXRESET signal.

MDIO Management Registers

The XAUI core, when generated with an MDIO interface, implements an MDIO Interface Register block. The core responds to MDIO transactions as either a 10GBASE-X PCS, a DTE XS, or a PHY XS depending on the setting of the type_sel port (see Table 4).

10GBASE-X PCS Registers

Table 7 shows the MDIO registers present when the XAUI core is configured as a 10GBASE-X PCS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 7: **10GBASE-X PCS/PMA MDIO Registers**

Register Address	Register Name
1.0	PMA/PMD Control 1
1.1	PMA/PMD Status 1
1.2,1.3	PMA/PMD Device Identifier
1.4	PMA/PMD Speed Ability
1.5, 1.6	PMA/PMD Devices in Package
1.7	10G PMA/PMD Control 2
1.8	10G PMA/PMD Status 2
1.9	Reserved
1.10	10G PMD Receive Signal OK
1.11 TO 1.13	Reserved
1.14, 1.15	PMA/PMD Package Identifier
1.16 to 1.65 535	Reserved

Table 7: **10GBASE-X PCS/PMA MDIO Registers *(Continued)***

Register Address	Register Name
3.0	PCS Control 1
3.1	PCS Status 1
3.2, 3.3	PCS Device Identifier
3.4	PCS Speed Ability
3.5, 3.6	PCS Devices in Package
3.7	10G PCS Control 2
3.8	10G PCS Status 2
3.9 to 3.13	Reserved
3.14, 3.15	PCS Package Identifier
3.16 to 3.23	Reserved
3.24	10GBASE-X PCS Status
3.25	10GBASE-X Test Control
3.26 to 3.65 535	Reserved

DTE XS Registers

Table 8 shows the MDIO registers present when the XAUI core is configured as a DTE XS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 8: **DTE XS MDIO Registers**

Register Address	Register Name
5.0	DTE XS Control 1
5.1	DTE XS Status 1
5.2, 5.3	DTE XS Device Identifier
5.4	DTE XS Speed Ability
5.5, 5.6	DTE XS Devices in Package
5.7	Reserved
5.8	DTE XS Status 2
5.9 to 5.13	Reserved
5.14, 5.15	DTE XS Package Identifier
5.16 to 5.23	Reserved
5.24	10G DTE XGXS Lane Status
5.25	10G DTE XGXS Test Control

PHY XS Registers

Table 9 shows the MDIO registers present when the XAUI core is configured as a PHY XS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 9: **PHY XS MDIO Registers**

Register Address	Register Name
4.0	PHY XS Control 1
4.1	PHY XS Status 1
4.2, 4.3	PHY XS Device Identifier
4.4	PHY XS Speed Ability
4.5, 4.6	PHY XS Devices in Package
4.7	Reserved
4.8	PHY XS Status 2
4.9 to 4.13	Reserved
4.14, 4.15	PHY XS Package Identifier
4.16 to 4.23	Reserved
4.24	10G PHY XGXS Lane Status
4.25	10G PHY XGXS Test Control

10-Gigabit Fibre Channel Support

The 10-Gigabit Fibre Channel (10GFC) specification describes a XAUI interface similar to the 10-Gigabit Ethernet XAUI but operating at 2% higher line and data rates, equating to a line rate on each device-specific transceiver lane of 3.1875 Gbps.

Virtex-4 FPGA Implementation

The non-*802.3-2008* State Machine option is not available for the Virtex-4 FPGA architecture:

Verification

The XAUI core has been verified using both simulation and hardware testing.

Simulation

A highly parameterizable transaction-based simulation test suite was used to verify the core. Verification tests include:

- Register access over MDIO
- Loss and regain of synchronization
- Loss and regain of alignment
- Frame transmission
- Frame reception
- Clock compensation
- Recovery from error conditions

Hardware Verification

The core has been used in a number of hardware test platforms within Xilinx. In particular, the core has been used in a test platform design with the Xilinx 10-Gigabit Ethernet MAC. This design comprises the MAC, XAUI, a *ping* loopback FIFO, and a test pattern generator all under embedded processor control. This design has been used for conformance and interoperability testing at the University of New Hampshire Interoperability Lab.

Device Utilization

Virtex-6 FPGAs

Table 10 provides approximate slice counts for the various core options on Virtex-6 FPGAs.

Table 10: **Device Utilization – Virtex-6 FPGAs**

Parameter Values				Device Resources		
External XGMII	802.3ae State Machines	TX Elastic Buffer	MDIO Interface	Slices	LUTs	FFs
No	No	No	No	301	676	644
No	No	No	Yes	375	826	745
No	Yes	No	No	359	798	712
No	Yes	No	Yes	423	947	807
Yes	No	No	No	306	675	644
Yes	No	No	Yes	367	825	745
Yes	No	Yes	No	437	1091	1062
Yes	No	Yes	Yes	504	1239	1163
Yes	Yes	No	No	365	798	712
Yes	Yes	No	Yes	441	946	807
Yes	Yes	Yes	No	492	1213	1130
Yes	Yes	Yes	Yes	576	1361	1225

Virtex-5 FPGAs

Tables 11 and 12 provide approximate slice counts for the various core options on Virtex-5 FPGAs.

Table 11: **Device Utilization – Virtex-5 LXT/SXT FPGAs**

Parameter Values				Device Resources		
External XGMII	802.3ae State Machines	TX Elastic Buffer	MDIO Interface	Slices	LUTs	FFs
No	No	No	No	432	564	652
No	No	No	Yes	518	715	753
No	Yes	No	No	551	712	718
No	Yes	No	Yes	644	863	815
Yes	No	No	No	437	564	652
Yes	No	No	Yes	499	715	753
Yes	No	Yes	No	632	965	1075
Yes	No	Yes	Yes	708	1116	1176
Yes	Yes	No	No	534	712	718
Yes	Yes	No	Yes	595	863	815
Yes	Yes	Yes	No	717	1121	1141
Yes	Yes	Yes	Yes	777	1272	1228

Table 12: **Device Utilization – Virtex-5 FXT/TXT FPGAs**

Parameter Values				Device Resources[1]		
External XGMII	802.3ae State Machines	TX Elastic Buffer	MDIO Interface	Slices	LUTs	FFs
No	No	No	No	1043	1189	1652
No	No	No	Yes	1116	1338	1753
No	Yes	No	No	1102	1349	1738
No	Yes	No	Yes	1204	1498	1835
Yes	No	No	No	1028	1189	1652
Yes	No	No	Yes	1096	1348	1753
Yes	No	Yes	No	1203	1538	2075
Yes	No	Yes	Yes	1302	1691	2176
Yes	Yes	No	No	1114	1349	1738
Yes	Yes	No	Yes	1164	1498	1835
Yes	Yes	Yes	No	1288	1698	2161
Yes	Yes	Yes	Yes	1453	1851	2258

1. All implementations require 4 block RAMs/FIFOs and 1 BUFG,

Virtex-4 FPGAs

Table 13 provides approximate slice counts for the various core options on Virtex-4 FPGAs.

Table 13: **Device Utilization – Virtex-4 FPGAs**

Parameter Values			Device Resources		
External XGMII	TX Elastic Buffer	MDIO Interface	Slices	LUTs	FFs
No	N/A	No	1299	1417	1008
No	N/A	Yes	1635	1763	1105
Yes	No	No	1355	1418	1008
Yes	No	Yes	1642	1763	1101
Yes	Yes	No	1717	1844	1431
Yes	Yes	Yes	2044	2118	1524

Spartan-6 FPGAs

Table 14 provides approximate slice counts for the various core options on Spartan-6 FPGAs.

Table 14: **Device Utilization – Spartan-6 FPGAs**

Parameter Values				Device Resources		
External XGMII	802.3ae State Machines	TX Elastic Buffer	MDIO Interface	Slices	LUTs	FFs
No	No	No	No	343	719	732
No	No	No	Yes	462	872	833
No	Yes	No	No	416	837	796
No	Yes	No	Yes	504	989	891

References

1. *IEEE Std. 802.3-2008*, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.
2. *IEEE Std. 802.3-2008*, Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10-Gbps Operation.

Support

Please visit www.xilinx.com/support for technical support. Xilinx provides technical support for this LogiCORE IP product when used as described in product documentation.

Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked *DO NOT MODIFY*.

Ordering Information

The LogiCORE IP XAUI core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated using the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.1 or higher.

This version of the XAUI IP core does not require a license key. Previous versions of the XAUI IP core released in ISE v11.2 and earlier did require a license key; please see the version of the getting started guide for the version of the core you are using for information.

For more information, please visit the XAUI product web page. Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

List of Acronyms

The following table describes acronyms used in this manual.

Acronym	Spelled Out
CML	Current Mode Logic
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DDR	Double Data Rate
DTE	Data Terminal Equipment
FCS	Frame Check Sequence
FF	flip-flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array.
GBIC	Gigabit Interface Converter
Gbps	Gigabits per second
GFC	Gigabit Fibre Channel
GMII	Gigabit Media Independent Interface
IES	Incisive Enterprise Simulator
IO	Input/Output
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mbps	Megabits per second
MDIO	Management Data Input/Output
MGT	Multi-Gigabit Transceiver
MHz	Mega Hertz
NGC	Native Generic Circuit
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment

Acronym	Spelled Out
PMD	Physical Medium Dependent
UCF	User Constraints File
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits).
XAUI	eXtended Attachment Unit Interface
XGMII	10-Gigabit Ethernet Media Independent Interface
XGXS	XGMII Extender Sublayer
XS	Extender Sublayer

Revision History

Date	Version	Revision
9/24/04	1.0	Initial Xilinx release in new data sheet format.
4/28/05	1.1	Document updated to support XAUI core v6.0 and Xilinx software v7.1i.
1/18/06	1.2	Updated dates, version number, and ISE tools 8.1i.
7/13/06	1.3	Updated core version to 6.2; Xilinx tools to 8.2i.
10/23/06	1.4	Updated core version to 7.0, added support for Virtex-5 LXT FPGAs.
2/15/07	1.5	Updated core version to 7.1; Xilinx tools to 9.1i.
8/8/07	1.6	Updated core version to 7.2; Xilinx tools to 9.2i.
3/24/08	1.7	Updated core version to 7.3; Xilinx tools to 10.1.
9/19/08	1.8	Updated core version to 7.4; added support for Virtex-5 TXT FPGAs.
4/24/09	1.9	Updated core version to 8.1; Xilinx tools to 11.1; added support for Virtex-6 FPGAs.
6/24/09	2.0	Updated core version to 8.2; Xilinx tools to 11.2; Added Virtex-6 CXT support.
09/16/09	2.1	Updated core version to 9.1; Xilinx tools to 11.3; Added Virtex-6 HXT, Virtex-6 Lower Power and Spartan-6 support.
12/02/09	2.1.1	Updated licensing information on page 15.
04/19/10	2.2	Updated core version to 9.2; Xilinx tools to 12.1

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