LogiCORE™ IP XAUI v9.2

Getting Started Guide

UG149 April 19, 2010

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/30/04	1.0	Initial Xilinx® release.
04/28/05	1.1	Updated to support XAUI core v6.0 and Xilinx v7.1i.
01/18/05	1.2	Updated to support XAUI core v6.1 and Xilinx ISE® software v8.1i.
07/13/06	1.3	Updated to support XAUI core v6.2 and Xilinx tools ISE software v8.2i.
10/23/06	1.4	Updated to support XAUI core v7.0 and Virtex®-5 LXT FPGAs.
02/15/07	1.5	Updated to support XAUI core v7.1 and Xilinx tools ISE software v9.1i.
08/08/07	1.6	Updated to support XAUI core v7.2 and Xilinx tools ISE software v9.2i.
03/24/08	1.7	Updated to support XAUI core v7.3 and Xilinx tools ISE software v10.1.
09/19/08	1.8	Updated to support XAUI core v7.4. Added support for Virtex-5 TXT FPGA devices.
04/24/09	1.9	Updated to support XAUI core v8.1 and Xilinx tools ISE software v11.1. Added support for Virtex-6 FPGAs.
06/24/09	2.0	Updated to support XAUI core v8.2 and Xilinx tools ISE software v11.2. Added Virtex-6 CXT support.
09/16/09	2.1	Updated to support XAUI core v9.1 and Xilinx tools ISE software v11.3. Added Virtex-6 HXT, Virtex-6 -1L and Spartan-6 support.
12/02/09	2.1.1	Updated licensing information on pages 15 and 16.
04/19/10	2.2	Updated to support XAUI core v9.2 and Xilinx tools ISE software v12.1.

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About This Guide

The *XAUI Getting Started Guide* provides information about generating a LogiCORE™ IP XAUI core, customizing and simulating the core utilizing the provided example design, and running the design files through implementation using the Xilinx® tools.

Guide Contents

This guide contains the following chapters:

- Preface, "About this Guide," introduces the organization and purpose of the design guide and the conventions used in this document.
- Chapter 1, "Introduction" introduces the XAUI core and provides related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx.
- Chapter 2, "Licensing the Core" provides instructions for installing and obtaining a license for the core, which must be completed before using the core in your designs.
- Chapter 3, "Quick Start Example Design" provides instructions for generating a core using the default configuration, implementing the example design, and simulating the core.
- Chapter 4, "Detailed Example Design" provides detailed information about the example design, including the directory structure and associated files, as well as how to modify the design and the associated tests for your applications.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays. Signal names also.	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File →Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Dark Shading	Items that are not supported or reserved	This feature is not supported
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** `[`*`option_name`*`]` *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**`{`**`on`**`|`**`off`**`}`
Angle brackets < >	User-defined variable or in code samples	<directory name>

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Convention	Meaning or Use	Example
Notations	The prefix '0x' or the suffix 'h' indicate hexadecimal notation	A read of address 0x00112975 returned 45524943h.
	An '_n' means the signal is active low	*usr_teof_n* is active low.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Guide Contents" for details. See "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to www.xilinx.com for the latest speed files.

List of Acronyms

The following table describes acronyms used in this manual.

Acronym	Spelled Out
DCM	Digital Clock Manager
DVE	Discovery Visualization Environment
FPGA	Field Programmable Gate Array.
HDL	Hardware Description Language
IES	Incisive Unified Simulator
IP	Intellectual Property
ISE®	Integrated Software Environment
NGD	Native Generic Database
SDF	Standard Delay Format
UCF	User Constraints File
VCS	Verilog Compiled Simulator (Synopsys)
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits).
XAUI	eXtended Attachment Unit Interface
XCO	Xilinx CORE Generator™ core source file
XGMII	10-Gigabit Ethernet Media Independent Interface
XST	Xilinx Synthesis Technology

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Chapter 1

Introduction

The XAUI core is a fully-verified solution that supports both Verilog and VHDL. In addition, the example design in this guide is provided in both Verilog and VHDL.

This chapter introduces the XAUI core and provides related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx®.

System Requirements

Windows

- Windows XP Professional 32-bit/64-bit
- Windows Vista Business 32-bit/64-bit

Linux

- Red Hat Enterprise Linux WS v4.0 32-bit/64-bit
- Red Hat Enterprise Desktop v5.0 32-bit/64-bit (with Workstation Option)
- SUSE Linux Enterprise (SLE) desktop and server v10.1 32-bit/64-bit

Software

- ISE® software v12.1

About the Core

The XAUI core is a CORE Generator™ IP software core, included in the latest IP Update on the Xilinx IP Center. For detailed information about the core see the XAUI product page. For information about system requirements, installation, and licensing options, see Chapter 2, "Licensing the Core."

Recommended Design Experience

Although the XAUI core is a fully-verified solution, the challenge associated with implementing a complete design varies depending on the configuration and functionality of the application. For best results, previous experience building high performance, pipelined FPGA designs using Xilinx implementation software and user constraints files (UCF) is recommended.

Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Additional Core Resources

For detailed information about XAUI technology and updates to the XAUI core, see the following sections.

Documentation

From the XAUI product page:

- *XAUI Data Sheet*
- *XAUI Getting Started Guide*

From the /doc directory after generating the XAUI core:

- *XAUI Release Notes*
- XAUI User Guide

XAUI Technology

For information about XAUI technology basics, including features, FAQs, the XAUI chip interface, typical applications, specifications, and other important information, see www.xilinx.com/products/ipcenter/XAUI.htm.

Ethernet Specifications

Relevant XAUI IEEE standards, which can be downloaded in PDF format from standards.ieee.org/getieee802/:

- *IEEE Std. 802.3-2008*

Technical Support

For technical support, visit www.xilinx.com/support. Questions are routed to a team of engineers with expertise using the XAUI core.

Xilinx provides technical support for use of this product as described in the *LogiCORE IP XAUI User Guide* and the *LogiCORE IP XAUI Getting Started Guide*. Xilinx cannot guarantee timing, functionality, or support of this product for designs that do not follow these guidelines.

Feedback

Xilinx welcomes comments and suggestions about the XAUI core and the documentation supplied with the core.

Core

For comments or suggestions about the XAUI core, submit a webcase from www.xilinx.com/support. Be sure to include the following information:

- Product name
- Core version number
- Explanation of your comments

Document

For comments or suggestions about this document, submit a webcase from www.xilinx.com/support. Be sure to include the following information:

- Document title
- Document number
- Page number(s) to which your comments refer
- Explanation of your comments

Chapter 2

Licensing the Core

This version of the XAUI IP core does not require a license key. Previous versions of the XAUI IP core released in ISE v11.2 and earlier did require a license key; please see the version of the getting started guide for the version of the core you are using for information. The XAUI core is provided under the terms of the Xilinx End User License Agreement.

Chapter 3

Quick Start Example Design

This chapter provides instructions for generating a core using the default configuration, implementing the example design, and simulating your design using Mentor Graphics ModelSim v6.5c, Cadence Incisive Enterprise Simulator (IES) v9.2, and Synopsys VCS and VCS MX 2009.12.

Introduction

Figure 3-1 illustrates the default configuration of the example design.

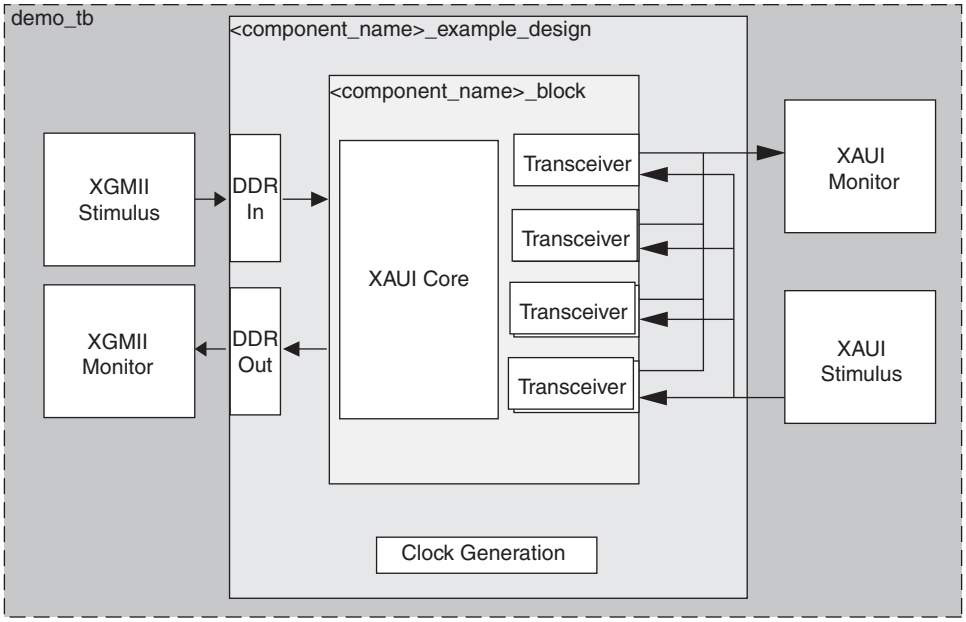

Figure 3-1: **XAUI Example Design and Test Bench: Default Configuration**

The XAUI example design consists of the following:

- A XAUI core netlist
- Transceiver wrappers
- An example HDL wrapper
- A demonstration test bench to exercise the example design

The XAUI Design Example has been tested with Xilinx® ISE® software v12.1, Mentor Graphics ModelSim v6.5c, Cadence Incisive Enterprise Simulator (IES) v9.2 and Synopsys VCS and VCS MX 2009.12.

Generating the Core

To generate a XAUI core with default values using the CORE Generator™ software do the following:

1. Start the CORE Generator software.

   For help starting and using the CORE Generator software, see the documentation supplied with ISE software.

2. Choose File > New Project.
3. Type a directory name.
4. Do the following to set project options:
   - From the Part tab, select a silicon family, part, speed grade, and package that supports the XAUI core, for example, Virtex®-4 FPGAs.

     Note: If an unsupported silicon family is selected, the XAUI core does not appear in the taxonomy tree. For a list of supported architectures, see the *XAUI Data Sheet*.
   - From the Generation tab, select VHDL or Verilog; for Vendor, select Other.
   - On the Advanced tab, accept the default values.
5. After creating the project, locate the core in the taxonomy tree at the left side of the CORE Generator software window. The XAUI core appears under the following categories:
   - Communications & Networking/Ethernet
   - Communications & Networking/Networking
   - Communications & Networking/Telecommunications
6. Double-click the core to open it. A message may appear warning you about the limitations of the Simulation Only license, and then the XAUI customization screen appears.
7. In the Component Name field, enter a name for the core instance.
8. Accept the remaining default options and click Finish to generate the core.

   The core and its supporting files, including the example design, are generated in the project directory. For a detailed description of the directory structure and files, see "Directory and File Contents" in Chapter 4.

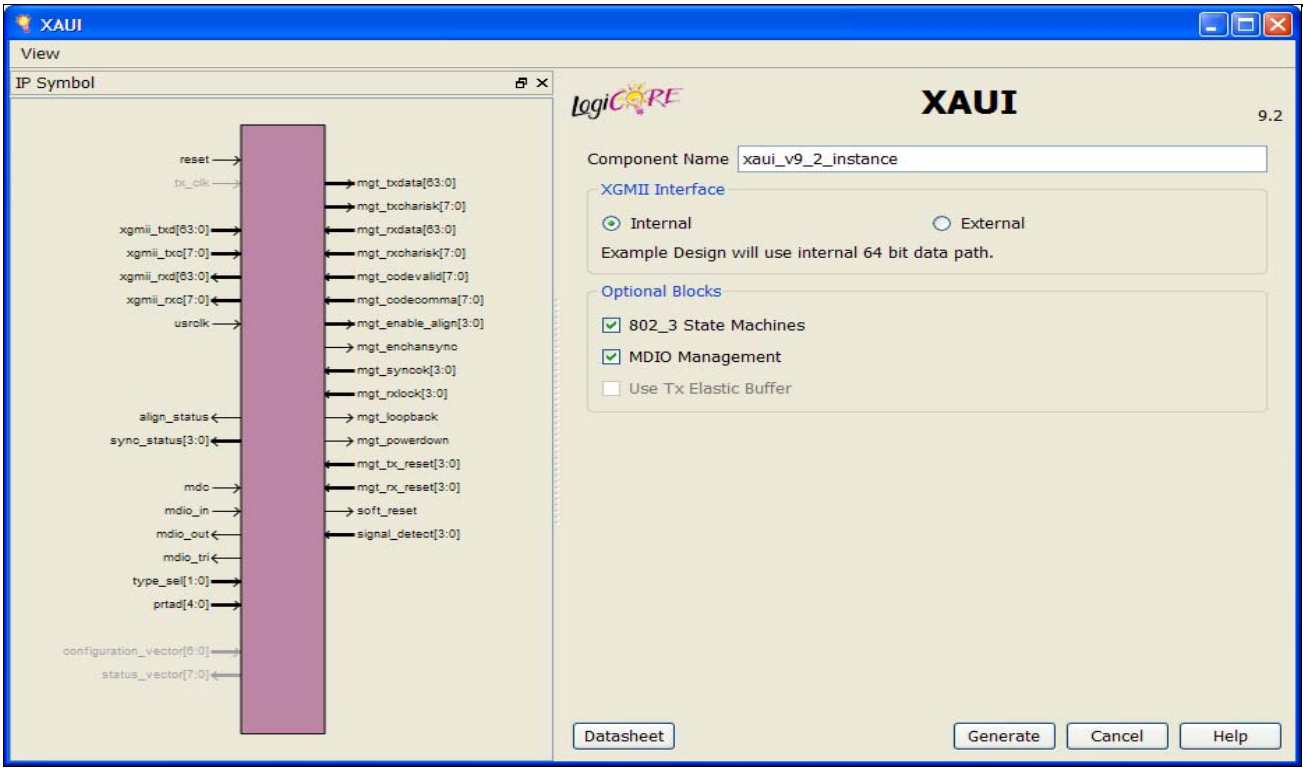

Figure 3-2: **XAUI Main Screen**

Implementing the XAUI Example Design

If the core is generated with a Simulation Only license, the implementation feature of the example design is not available; in this case, go directly to Chapter 3, "Simulating the XAUI Example Design."

After the core is successfully generated, the netlist and example design HDL wrapper can be processed through the Xilinx implementation tools. The generated outputs include several scripts to assist in processing.

Open a command prompt or shell in your project directory and enter the following commands:

Linux

```
% cd <component_name>/implement
% ./implement.sh
```

Windows

```
> cd <component_name>\implement
> implement.bat
```

The implement command accomplishes the following:

- Starts a script to synthesize the example design HDL wrapper
- Builds, maps, and place-and-routes the example design (Full license only)
- Creates gate-level netlist HDL files in both VHDL and Verilog with associated timing information (SDF files)

The created files are placed in the results directory which is created by the implement script at runtime.

Simulating the XAUI Example Design

The example design provided with the XAUI core provides a complete environment which allows you to simulate the core and view the outputs. Scripts are provided for pre- and post-layout simulation. The simulation model is either in VHDL or Verilog depending on the CORE Generator software Design Entry project option.

Setting up for Simulation

To run the gate-level simulation you must have the Xilinx Simulation Libraries compiled for your system. See the Compiling Xilinx Simulation Libraries (COMPXLIB) in the *Xilinx ISE Synthesis and Verification Design Guide*, and the *Xilinx ISE Software Manuals and Help*. You can download these documents from: www.xilinx.com/support/software_manuals.htm.

The Xilinx simulation libraries must be mapped into the simulator. If the libraries are not set for your environment, go to Answer Record 15338 on www.xilinx.com/support for assistance compiling Xilinx simulation models and setting up the simulator environment.

All Virtex family designs require a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator, the following simulators are supported.

- Mentor Graphics ModelSim v6.5c and above
- Cadence Incisive Enterprise Simulator (IES) v9.2 and above
- Synopsys VCS and VCS MX 2009.12 and above

Pre-Implementation Simulation

To run a functional simulation of the example design:

1. Open a command prompt or shell in your project directory and set the current directory to

   ```
   <component_name>/simulation/functional
   ```

2. Launch the simulation script:

   ```
   ModelSim: vsim -do simulate_mti.do
   Cadence sim: ./simulate_ncsim.sh
   vcs: ./simulate_vcs.sh
   ```

The simulation script compiles the functional model and the demonstration test bench, adds some relevant signals to a wave window, and then runs the simulation to completion. You can then inspect the simulation transcript and waveform to observe the operation of the core.

Post-Implementation Simulation

To run a timing simulation of the example design:

1. Open a command prompt or shell in your project directory, then set the current directory to:

   ```
   <component_name>/simulation/timing
   ```

2. Launch the simulation script:

   ```
   ModelSim: vsim -do simulate_mti.do
   ncsim: ./simulate_ncsim.sh
   vcs: ./simulate_vcs.sh
   ```

The simulation script compiles the gate-level model and the demonstration test bench, adds some relevant signals to a wave window, and then runs the simulation to completion. You can then inspect the simulation transcript and waveform to observe the operation of the core.

Additional Information

For more information about the example design, including guidelines for modifying the design and extending the test bench, see Chapter 4, "Detailed Example Design." To start using the XAUI core in your own design, see the *XAUI User Guide*.

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Chapter 4

Detailed Example Design

This chapter provides detailed information about the example design, including a description of files and the directory structure generated by the Xilinx® CORE Generator™ software, the purpose and contents of the provided scripts, the contents of the example HDL wrappers, and the operation of the demonstration test bench.

- **<project directory>**
  Top-level project directory; name is user-defined.
  - <project directory>/<component name>
    Core release notes file
    - <component name>/doc
      Product documentation
    - <component name>/example_design
      Verilog and VHDL design files
    - <component name>/implement
      Implementation script files
      - implement/results
        Results directory, created after implementation scripts are run, and contains implement script results
    - <component name>/simulation
      Simulation scripts
      - simulation/functional
        Functional simulation files
      - simulation/timing
        Timing simulation files

Directory and File Contents

The core directories and their associated files are defined in the following sections.

<project directory>

The project directory contains all the CORE Generator software project files.

Table 4-1: **Project Directory**

Name	Description
<project_dir>	
<component_name>.ngc	A binary Xilinx implementation netlist. Describes how the core is to be implemented. Used as an input to the Xilinx implementation tools.
<component_name>.v[hd]	VHDL or Verilog structural simulation model. File used to support functional simulation of a core.
<component_name>.xco	As an output file, the XCO file is a log file which records the settings used to generate a particular core. An XCO file is generated by the CORE Generator software for each core that it creates in the current project directory. An XCO file can also be used as an input to the CORE Generator software.
<component_name>_flist.txt	List of files delivered with the core
<component_name>.{veo|vho}	A VHDL or Verilog template for the core. This can be copied into your design.

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<project directory>/<component name>

The <component name> directory contains the release notes file provided with the core, which may include last-minute changes and updates.

Table 4-2: **Component Name Directory**

Name	Description
<project_dir>/<component_name>	
xaui_readme.txt	Core release notes file

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<component name>/doc

The doc directory contains the PDF documentation provided with the core.

Table 4-3: **Doc Directory**

Name	Description
<project_dir>/<component_name>/doc	
xaui_ds266.pdf	XAUI Data Sheet
xaui_gsg149.pdf	XAUI Getting Started Guide
xaui_ug150.pdf	XAUI User Guide

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<component name>/example_design

The example design directory contains the example design files provided with the core.

Table 4-4: **Example Design Directory**

Name	Description
<project_dir>/<component_name>/example_design	
<component_name>_block.v[hd]	Block entity containing the XAUI core and transceiver wrappers
<component_name>_example_design.v[hd]	Top-level entity for the example design containing the block level design and clocking circuitry
<component_name>_example_design.ucf	User constraints file for the core and example design
<component_name>_mod.v	Wrapper file for the XAUI core
cal_block_v1_4_1.v[hd] (Virtex-4 FPGAs only)	Virtex®-4 FX FPGA Calibration Block
chanbond_monitor.v[hd]	Transceiver Channel Bonding Monitor
cc_2b_1skp.v[hd] (Virtex-5 FXT/TXT FPGAs only)	Transceiver Clock Correction
rocketio_init_rx.v[hd] (Virtex-4 FPGAs only) rocketio_init_tx.v[hd] (Virtex-4 FPGAs only) tx_sync.v[hd] (Spartan-6, Virtex-5 and Virtex-6 FPGAs)	Transceiver initialization circuitry

Table 4-4: **Example Design Directory <EM EmphasisItalic>(Continued)**

Name	Description
rocketio_wrapper.v[hd] (Virtex-4, Virtex-5 FPGAs only) rocketio_wrapper_tile.v[hd] (Virtex-5 FPGAs only) gtp_wrapper.v[hd] (Spartan-6 FPGAs only) gtp_wrapper_tile.v[hd] (Spartan-6 FPGAs only) gtx_wrapper_gtx.v[hd] (Virtex-6 FPGAs only) gtx_wrapper.v[hd] (Virtex-6 FPGAs only)	Wrappers for the transceivers

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<component name>/implement

This directory contains the support files necessary for implementation of the example design with the Xilinx tools. Execution of an implement script creates a results directory and an xst project directory.

Table 4-5: **Implement Directory**

Name	Description
<project_dir>/<component_name>/implement	
implement.bat	Windows batch file that process the example design through the Xilinx tool flow
implement.sh	Linux shell script that processes the example design through the Xilinx tool flow
xst.scr	XST script file for the example design
xst.prj	XST project file for the example design
xst.xcf	XCF constraint file for the example design

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implement/results

This directory is created by the implement scripts and is used to run the example design files and the `<component_name>.ngc` file through the Xilinx implementation tools. On completion of an implement script, this directory contains the following files for timing simulation. Output files from the Xilinx implementation tools can also be found in this directory.

Table 4-6: **Results Directory**

Name	Description
`<project_dir>/<component_name>/implement/results`	
`routed.v[hd]`	The back-annotated SimPrim-based VHDL or Verilog design. Used for timing simulation.
`routed.sdf`	Timing information for simulation

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<component name>/simulation

The simulation directory and the subdirectories below it contain the files necessary to test a VHDL or Verilog implementation of the example design.

Table 4-7: **Simulation Directory**

Name	Description
<project_dir>/<component_name>/simulation	
`demo_tb.v[hd]`	The VHDL or Verilog demonstration test bench for the XAUI core

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simulation/functional

The functional directory contains functional simulation scripts provided with the core.

Table 4-8: **Functional Directory**

Name	Description
<project_dir>/<component_name>/simulation/functional	
`simulate_mti.do`	ModelSim macro file that compiles the example design sources, the structural simulation model and the demonstration test bench then runs the functional simulation to completion.
`simulate_ncsim.sh`	Linux shell script that compiles the example design sources and the structural simulation model then runs the functional simulation to completion using the Cadence IES simulator.
`simulate_vcs.sh (verilog only)`	Linux shell script that compiles the example design sources and the structural simulation model then runs the functional simulation to completion using VCS.
`ucli_commands.key (verilog only)`	VCS command file. This file is called by the simulate_vcs.sh script.
`vcs_session.tcl (verilog only)`	VCS DVE tcl script that opens wave windows and adds interesting signals to it. This macro is used by the simulate_vcs.sh script.
`wave_mti.do`	ModelSim macro file that opens a wave window and adds interesting signals to it. This macro is called by the `simulate_mti.do` macro file.
`wave_ncsim.sv`	The Cadence IES simulator macro file that opens a wave windows and adds interesting signals to it. This macro is called by the simulate_ncsim.sh script.

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simulation/timing

The timing directory contains timing simulation scripts provided with the core.

Table 4-9: **Timing Directory**

Name	Description
<project_dir>/<component_name>/simulation/timing	
`simulate_mti.do`	ModelSim macro file that compiles the timing simulation model and the demonstration test bench then runs the timing simulation to completion.
`simulate_ncsim.sh`	Linux shell script that compiles the test bench and the timing model then runs the timing simulation to completion using the Cadence IES simulator.
`simulate_vcs.sh`	Linux shell script that compiles the example design sources and the timing simulation model then runs the timing simulation to completion using VCS.
`ucli_commands.key (verilog only)`	VCS command file. This file is called by the simulate_vcs.sh script.
`vcs_session.tcl (verilog only)`	VCS DVE tcl script that opens wave windows and adds interesting signals to it. This macro is called by the simulate_vcs.sh script.
`wave_mti.do`	ModelSim macro file that opens a wave window and adds interesting signals to it. This macro is called by the `simulate_mti.do` macro file.
`wave_ncsim.sv`	The Cadence IES simulator macro file that opens a wave windows and adds interesting signals to it. This macro is called by the `simulate_ncsim.sh` script.

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Implementation and Test Scripts

Implementation Script

The implementation script is either a shell script or batch file that processes the example design through the Xilinx tool flow. The script is located at:

Linux

```
<project_dir>/<component_name>/implement/implement.sh
```

Windows

```
<project_dir>/<component_name>/implement/implement.bat
```

The implement script performs the following steps:

- The example HDL wrapper is synthesized using XST.
- ngdbuild is run to consolidate the core netlist and the wrapper netlist into the NGD file containing the entire design.
- The design is mapped to the target technology.
- The design is place-and-routed on the target device.
- Static timing analysis is performed on the routed design using trce.
- A bitstream is generated.
- netgen runs on the routed design to generate VHDL and Verilog netlists and timing information in the form of SDF files.

Setting up for Simulation

The Xilinx UniSim library must be mapped into the simulator. If the library is not set up for your environment, go to Answer Record 15338 for assistance compiling Xilinx simulation models and for setting up the simulator environment.

All Virtex family designs require a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator, the following simulators are supported.

- Mentor Graphics ModelSim v6.5c and above
- Cadence Incisive Enterprise Simulator (IES) v9.2 and above
- Synopsys VCS and VCS MX 2009.12 and above

Simulation Scripts

Simulation macro files are provided for ModelSim and shell scripts are provided for the Cadence IES simulator and Synopsys VCS simulator. The scripts automate the simulation of the test bench and can be found in the following location:

Functional

`<project_dir>/<component_name>/simulation/functional/simulate_mti.do`

`<project_dir>/<component_name>/simulation/functional/simulate_ncsim.sh`

`<project_dir>/<component_name>/simulation/functional/simulate_vcs.sh`

Timing

`<project_dir>/<component_name>/simulation/timing/simulate_mti.do`

`<project_dir>/<component_name>/simulation/timing/simulate_ncsim.sh`

`<project_dir>/<component_name>/simulation/timing/simulate_vcs.sh`

The scripts perform the following tasks:

- Compiles the gate level netlist
- Compiles the demonstration test bench
- Starts a simulation of the test bench
- Opens a Wave window and adds some interesting signals (`wave_mti.do/wave_ncsim.sv/vcs_session.tcl`)
- Runs the simulation to completion

XAUI Core with External XGMII Client-Side Interface

Example HDL Wrapper

In Figure 4-1, the example generated HDL wrapper contains the following:

- The RocketIO™ transceiver instances
- Virtex-4 FPGA RocketIO transceiver Calibration Blocks (see Answer Record 22477 for information about the Calibration Block User Guide)
- Initialization blocks for the transmit and receive RocketIO transceivers
- Clock management logic, including DCM and Global Clock Buffer instances
- DDR logic for the XGMII interface

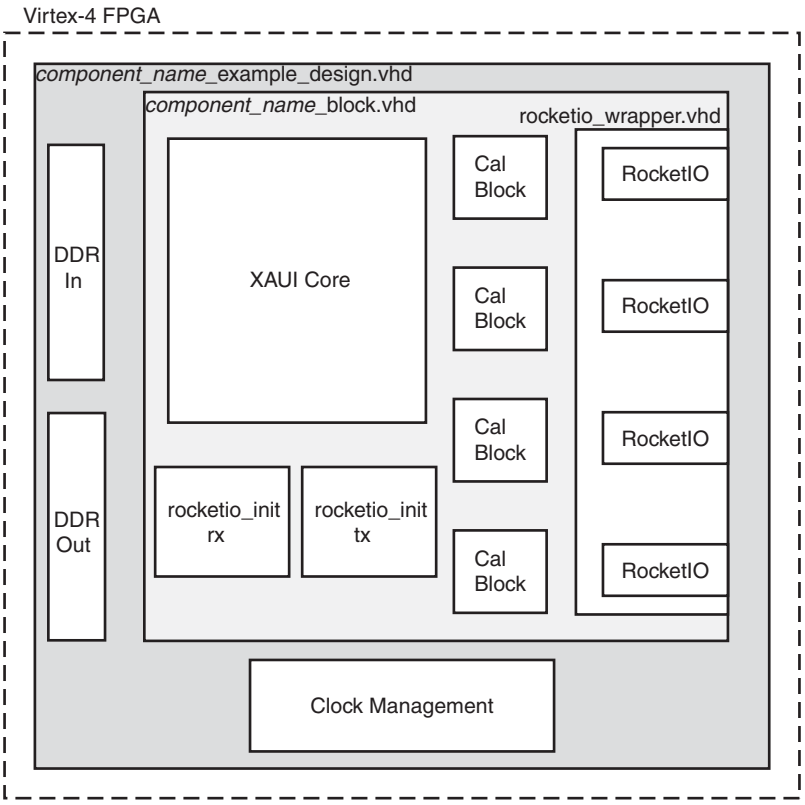

Figure 4-1: **Example HDL Wrapper for XAUI with XGMII (Virtex-4 FPGAs)**

In Figure 4-2, the example generated HDL wrapper contains the following:

- The RocketIO transceiver tile instances
- The wrapper for the two RocketIO transceiver tiles
- A RocketIO transceiver transmit initialization block
- Clock management logic, including DCM and Global Clock Buffer instances
- DDR logic for the XGMII interface

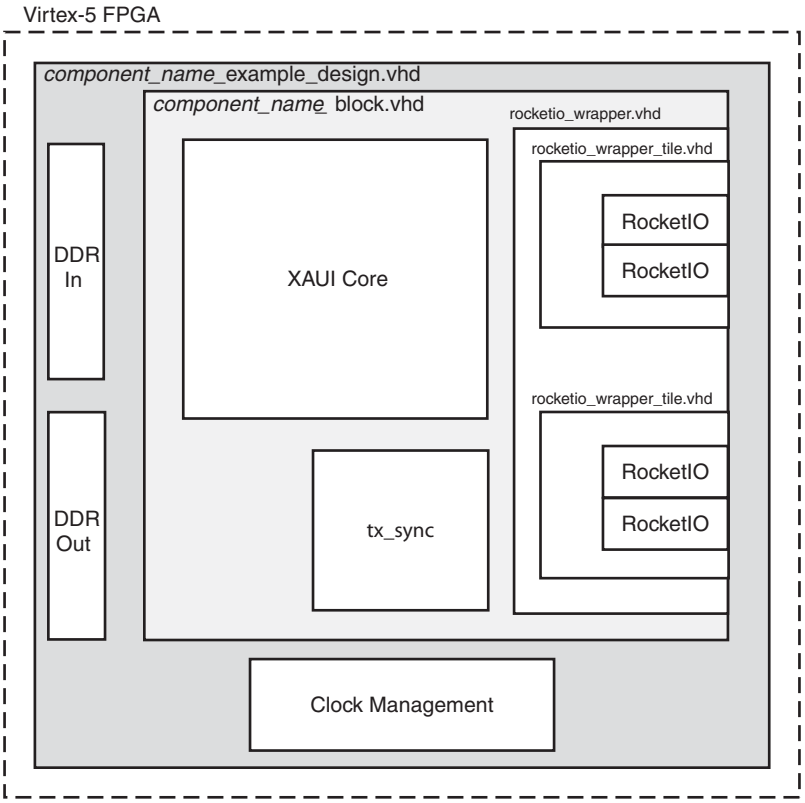

Figure 4-2: **Example HDL Wrapper for XAUI with XGMII (Virtex-5 FPGAs)**

In Figure 4-3, the example generated HDL wrapper contains the following:

- The Transceiver Instances
- A wrapper for the four transceivers
- A transceiver transmit initialization block
- Clock management logic, including MMCM and Global Clock Buffer instances
- DDR logic for the XGMII interface

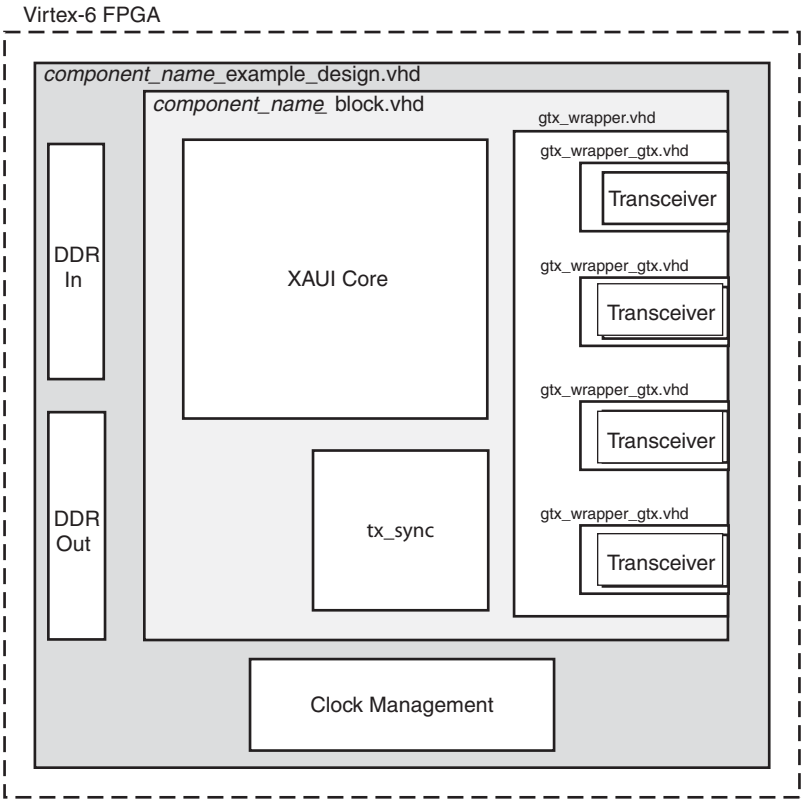

Figure 4-3: **Example HDL Wrapper for XAUI with XGMII (Virtex-6 FPGAs)**

Demonstration Test Bench

The demonstration test bench in Figure 4-4 is a simple VHDL or Verilog program to exercise the example design and the core itself. This test bench consists of transactor procedures or tasks which connect to the major ports of the example design, and a control program that pushes frames of varying length and content through the design and checks the values as they exit the core.

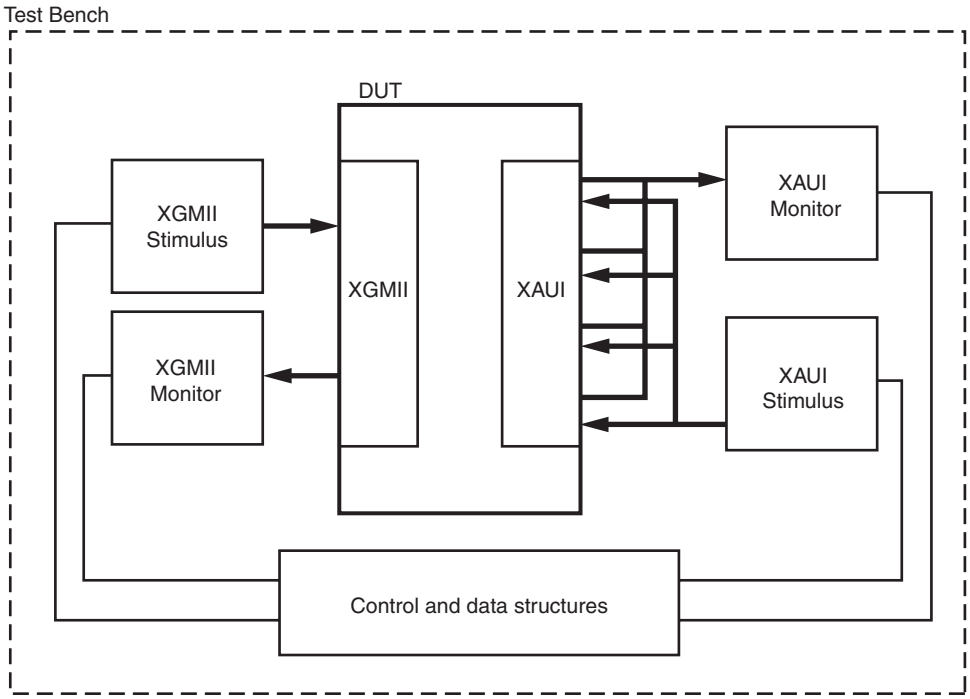

Figure 4-4: **Demonstration Test Bench for XAUI with XGMII Interface**

XAUI Core with Internal Client-side Interface

Example HDL Wrapper

In Figure 4-5, the example HDL wrapper generated when the internal client-side interface is selected contains the following:

- The RocketIO transceiver instances
- Virtex-4 device RocketIO transceiver Calibration Blocks (see Answer Record 22477 for information about the Calibration Block User Guide)
- Initialization blocks for the transmit and receive RocketIO transceivers
- Clock management logic, including DCM and Global Clock Buffer instances
- Re-timing registers on the parallel data interface, both on input and output

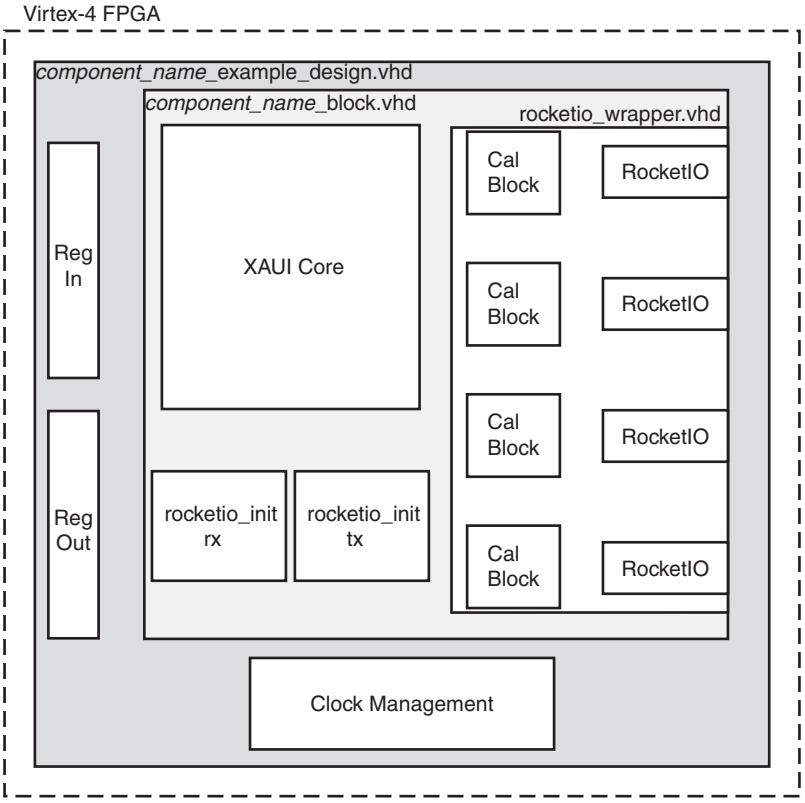

Figure 4-5: **Example HDL Wrapper for XAUI without XGMII (Virtex-4 FPGAs)**

In Figure 4-6, the example HDL wrapper generated when the internal client-side interface is selected contains the following:

- The RocketIO transceiver tile instances
- The wrapper for the two RocketIO transceiver tiles
- A RocketIO transceiver transmit initialization block
- Clock management logic, including DCM (if required) and Global and Clock Buffer instances
- Re-timing registers on the parallel data interface, both on input and output

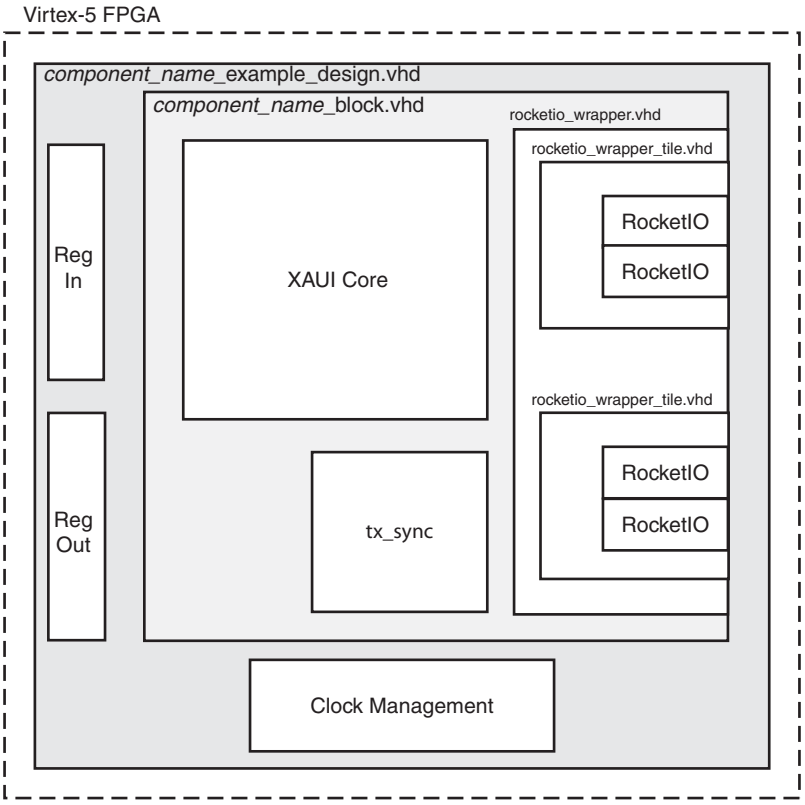

Figure 4-6: **Example HDL Wrapper for XAUI without XGMII (Virtex-5 FPGAs)**

In Figure 4-7, the example HDL wrapper generated when the internal client-side interface is selected contains the following:

- The Transceiver Instances
- The wrapper for the four transceivers
- A transceiver transmit initialization block
- Clock management logic and Clock Buffer instances
- Re-timing registers on the parallel data interface, both on inputs and outputs

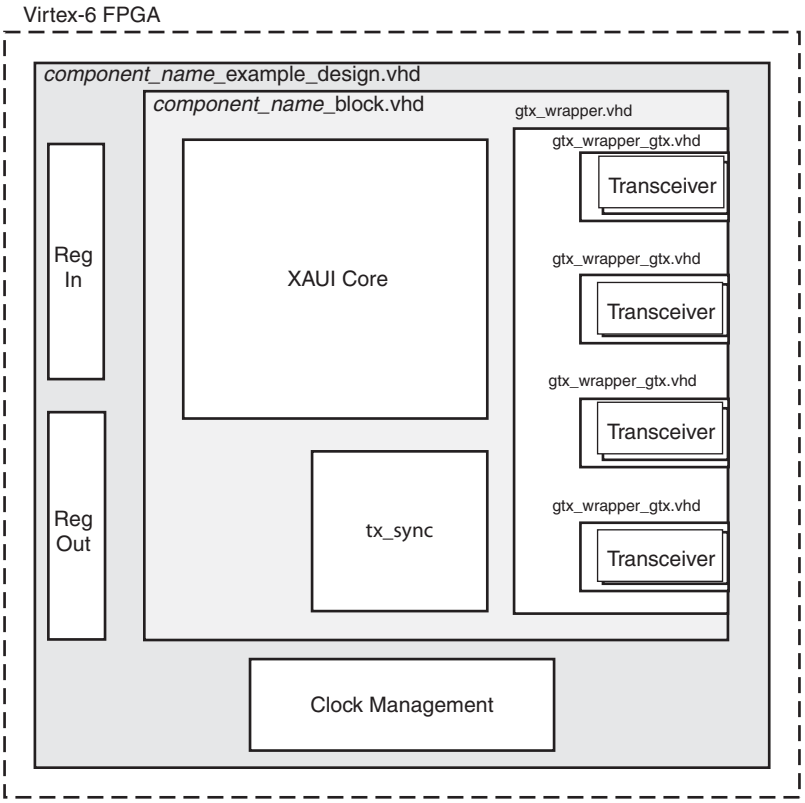

Figure 4-7: **Example HDL Wrapper for XAUI without XGMII (Virtex-6 FPGAs)**

In Figure 4-8, the example HDL wrapper generated when the internal client-side interface is selected contains the following:

- The Transceiver Instances
- The wrapper for the four transceivers
- A transceiver synchronization block
- Clock management logic and Clock Buffer instances
- Re-timing registers on the parallel data interface, both on inputs and outputs

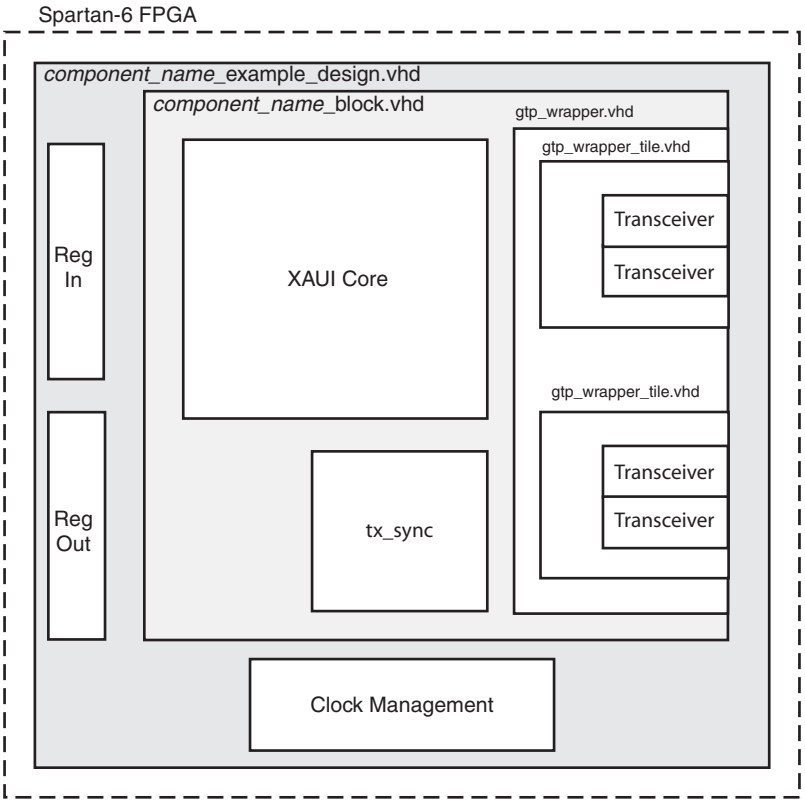

Figure 4-8: **Example HDL Wrapper for XAUI without XGMII (Spartan-6 FPGAs)**

Demonstration Test Bench

In Figure 4-9, the demonstration test bench is a simple VHDL or Verilog program to exercise the example design and the core itself. This test bench consists of transactor procedures or tasks that connect to the major ports of the example design, and a control program that pushes frames of varying length and content through the design and checks the values as they exit the core.

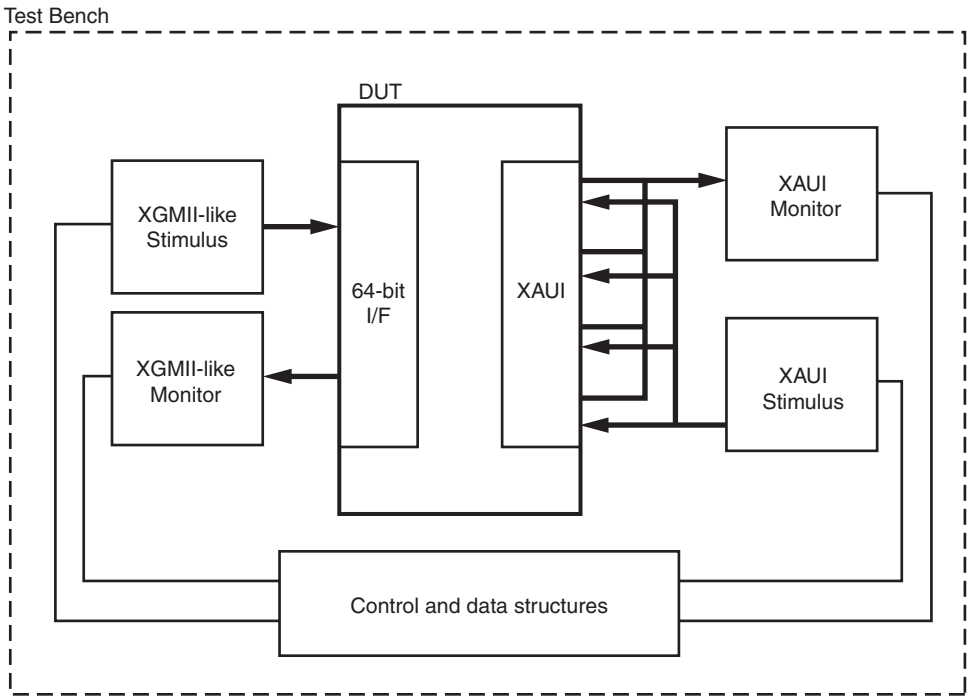

Figure 4-9: **Demonstration Test Bench for XAUI without XGMII Interface**