

Introduction

The Constant IP core is used to drive a constant value on a bus. Often there is a need to drive a signal or a bus to a predetermined value. The Constant IP core provides this capability in the block design.

Additional Information

See the [product page](#).

Features

- Parameterizable bus width
- Value to be driven in decimal, binary (b), octal (0), and hexadecimal format (0x or 0X) formats.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows⁽²⁾	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	N/A
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

The Constant IP core is used to drive a static value on a bit or a bus.

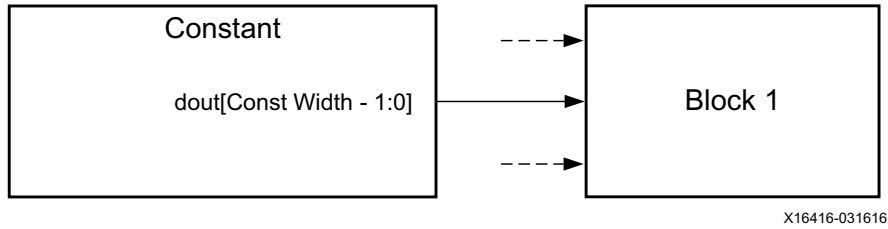


Figure 1: Constant Block in a System

Block Diagram

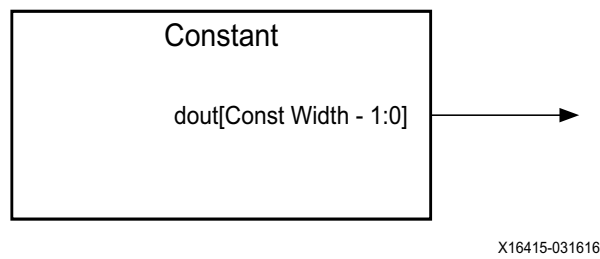


Figure 2: Constant Block Diagram

Using Constant IP Core in a Block Design

In a block design you instantiate the Constant IP core by right clicking in the block design canvas and selecting Add IP from the context menu.

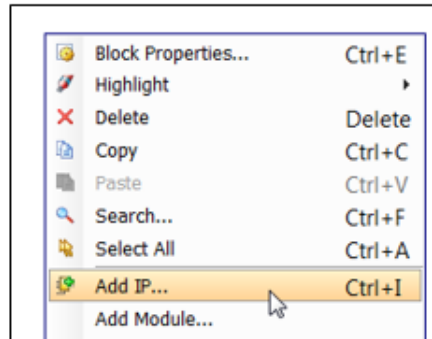


Figure 3: Adding the Constant Block in the Block Design Canvas

In the Search field of the IP catalog, type **Constant** and double click on the selection to instantiate it.

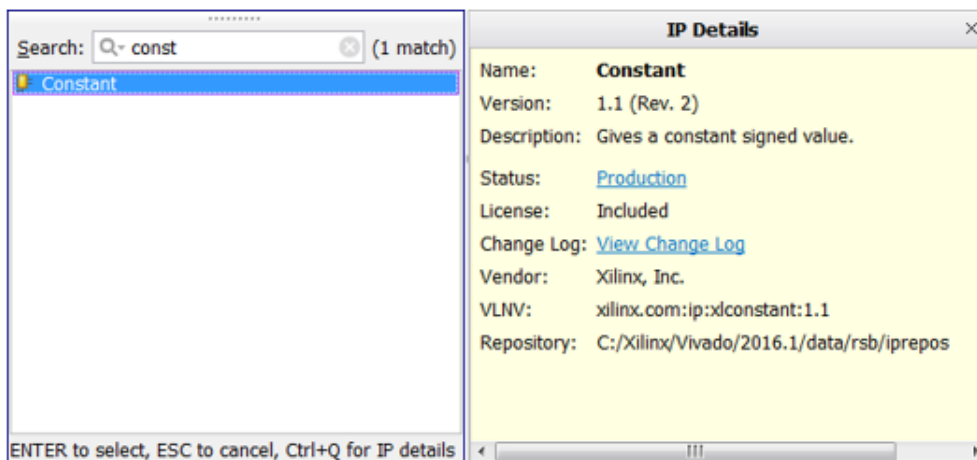


Figure 4: Search the Constant IP Core in the IP Catalog and Instantiate

This instantiates the Constant IP core in the design as shown in [Figure 5](#).

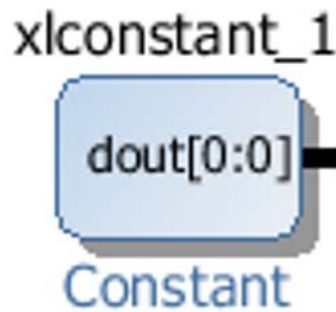


Figure 5: Constant IP Core Before Customization

Double-click the Constant block to open the Re-customize IP dialog box.

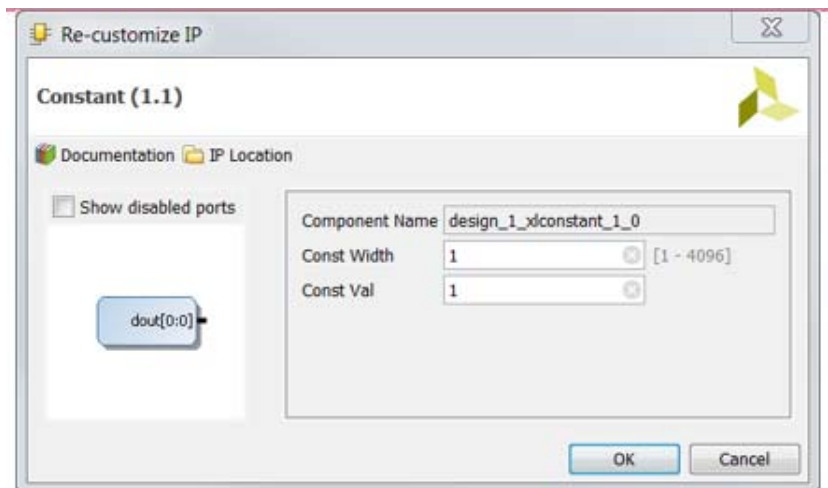


Figure 6: Re-customize IP Dialog Box

In Figure 6, set the **Const Width** value to the desired bit-width. In the **Const Val** field, specify the constant value in decimal, binary (b), octal (0), or hexadecimal (0x or 0X) format. If you specify the values in binary, octal, or hexadecimal format, a prefix of b, 0, or 0x/0X should be added respectively. For example, if you specify the **Const Val** as decimal 12, this is 1100 in binary. This means 4 bits are needed for this value and therefore, the Const Width should be 4 at a minimum.

I/O Signals

The I/O signals are listed and described in Table 1.

Table 1: I/O Signals

Port Name	Description
dout[Const Width - 1: 0]	Output port of the Constant block that drives the constant value.

Design Parameters

The parameters are listed and described in [Table 2](#).

Table 2: Design Parameters

Parameter	Description	Type
Const Width	The bit width of the output port.	

Design Implementation

Design Tools

Note: This IP can only be used in the Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within Vivado Design Suite.

HDL file for the IP is generated during Output Product generation.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series.

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

Licensing and Ordering Information

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/09/2018	1.1	Added support for specifying the constant value in decimal, binary (b), octal (0) or hexadecimal (0x or 0X) format. Updated the legal notices.
04/06/2016	1.1	Initial Xilinx release.

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