LogiCORE IP XPS Timebase Watchdog Timer (v1.02a)

DS582 July 23, 2010 **Product Specification**

Introduction

The XPS Timebase Watchdog Timer Interface is a 32-bit peripheral that provides a 32-bit free-running timebase and watchdog timer.

Features

- Connects as a 32-bit slave on PLB V4.6 buses of 32, 64 or 128 bits
- Watchdog timer (WDT) with selectable timeout period and interrupt
- Configurable WDT enable: enable-once or enable-disable
- One 32-bit free-running timebase counter with rollover interrupt

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Virtex®-4, Virtex-4Q, Virtex-4QV, Virtex-5, Virtex-6, Spartan®-3E, Automotive Spartan-3E, Spartan-3, Automotive Spartan-3, Spartan-3A, Automotive Spartan-3A, Spartan-3A DSP, Automotive Spartan-3A DSP
Supported User Interfaces	32-bit PLBv46 Slave
Resources	
See Table 8, Table 9, Table 10, Table 11, and Table 12.	
Provided with Core	
Documentation	Product Specification
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Design Files
Tested Design Tools	
Design Entry Tools	Provide version of Xilinx tools tested, e.g., PlanAhead™ tool, CORE Generator™ tool, System Generator, Platform Studio, XPS
Simulation	Mentor Graphic ModelSim v6.5c and above
Synthesis Tools	XST
Support	
Provided by Xilinx, Inc.	

Notes:

1. For a complete listing of supported devices, see the release notes for this core.

Functional Description

The top-level block diagram for the XPS Timebase Watchdog Timer is shown in Figure 1.

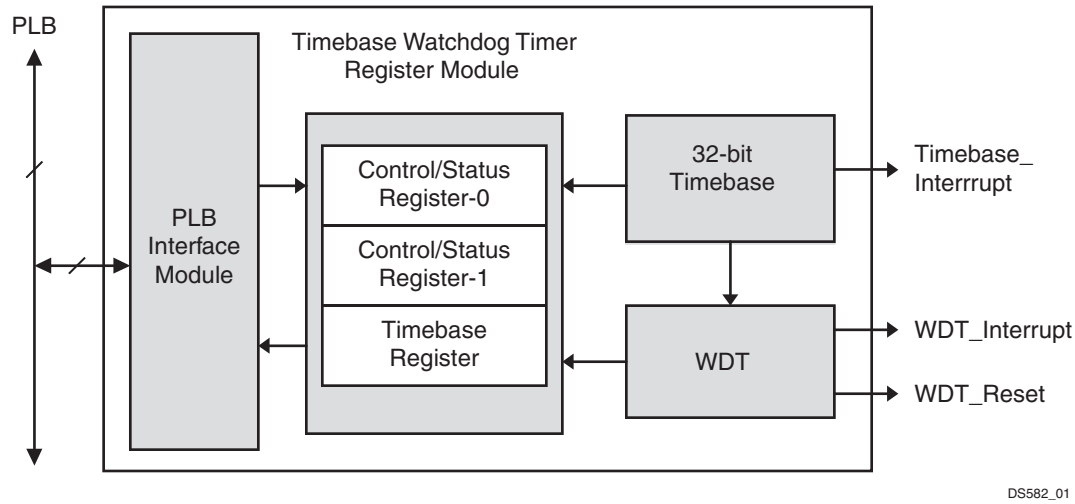

Figure 1: **Block Diagram of XPS Timebase Watchdog Timer**

The XPS Timebase Watchdog Timer modules are described in the sections below

PLB Interface Module: The PLB Interface Module provides the interface to the PLB. Read and write transactions at the PLB are translated into equivalent IP Interconnect (IPIC) transactions. The register interfaces of the XPS Timebase Watchdog Timer connect to the IPIC. The PLB Interface Module also provides an address decoding service.

Timebase Watchdog Timer Register Module: The Timebase Watchdog Timer Register Module includes all memory mapped registers (as shown in Figure 1). It interfaces to the PLB. It consists of an 32-bit control/status register-0, an 32-bit control/status register-1 and an 32-bit timebase register (TBR).

32-bit Timebase: The 32-bit timebase consists of free-running 32-bit timebase counter.

WDT: The Watchdog Timer (WDT) provides the functionality of timeout.

XPS Timebase Watchdog Timer Characteristics

The XPS Timebase Watchdog Timer has the following characteristics:

- Consists of a free-running 32-bit timebase counter that is used for both the general purpose timing and the WDT facility
- The timebase counter always counts up from system reset and is read-only
- The WDT timeout interval is set by generic C_WDT_INTERVAL, which determines the bit in the timebase to be used as input to the WDT state machine
- The WDT uses a dual-expiration architecture. After one expiration of the timeout interval an interrupt is generated and the WDT state bit is set to one in the status register. If the state bit is not cleared (by writing a '1' to the state bit) before the next expiration of the timeout interval, a WDT reset is generated. A WDT reset, sets the WDT reset status bit in the status register so that the application code can determine if the last system reset was a WDT reset.
- The WDT can only be disabled by writing to two distinct addresses, reducing the possibility of inadvertently disabling the WDT in the application code.

XPS Timebase Watchdog Timer Operation

Timebase Operation

The timebase is a 32-bit up counter that is incremented by one on the rising edge of the clock provided to the Timebase Watchdog Timer. The counter is reset to zero when the reset input is high or when the WDT is enabled. The TBR contains the full timebase count value of 32 bits.

The TWCSR0 contains the most-significant 28 bits of the timebase count, as well as the WDT enable and status bits. The timing resolution from the upper 28 bits of the timebase count is T_{clk} x 16 (T_{clk} is the period of the input clock). As a result, a single access can be used to read the state of the watchdog timer, as well as a reduced resolution version of the timebase.

An interrupt signal is provided that pulses high for one clock period as the counter rolls over from `0xFFFFFFFF` to `0x00000000`. This interrupt can be used by the software to keep track of how many timebase rollovers have occurred.

WDT Operation

The WDT timeout interval is configured by a parameter to be $2^{C\_WDT\_INTERVAL}$ clock cycles, where C_WDT_INTERVAL is any integer from 8 to 31. The WDT interval is set at FPGA configuration time and cannot be modified dynamically through a control register. Figure 2 shows the WDT state diagram.

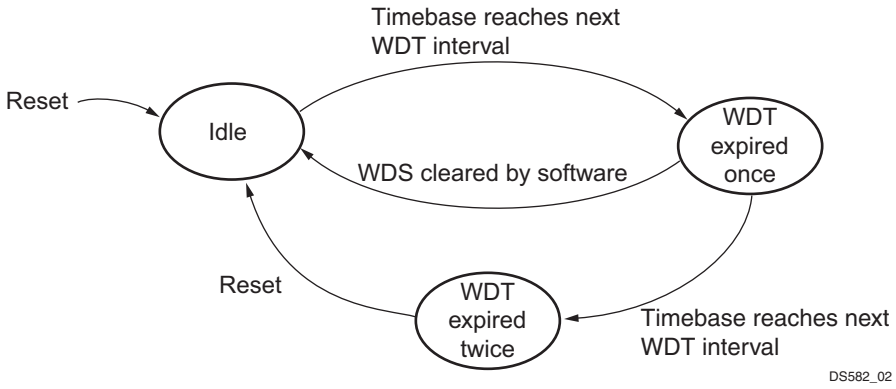

Figure 2: **State Diagram**

I/O Signals

The XPS Timebase Watchdog Timer I/O signals are listed and described in Table 1.

Table 1: **I/O Signal Descriptions**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0 : 31]	PLB	I	-	PLB address bus
P4	PLB_PAValid	PLB	I	-	PLB primary address valid
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier

Table 1: **I/O Signal Descriptions *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P8	PLB_size[0 : 3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0 : 31]	PLB	I	-	PLB upper address bits
P12	PLB_SAValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P18	PLB_lockErr	PLB	I	-	PLB lock error
P19	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P20	PLB_rdBurst	PLB	I	-	PLB burst read transfer
P21	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P22	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P23	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P24	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P25	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
P26	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P27	Sl_addrAck	PLB	O	0	Slave address acknowledge
P28	Sl_SSize[0 : 1]	PLB	O	0	Slave data bus size
P29	Sl_wait	PLB	O	0	Slave wait
P30	Sl_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	Sl_wrDAck	PLB	O	0	Slave write data acknowledge
P32	Sl_wrComp	PLB	O	0	Slave write transfer complete
P33	Sl_rdDBus[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	Sl_rdDAck	PLB	O	0	Slave read data acknowledge
P35	Sl_rdComp	PLB	O	0	Slave read transfer complete
P36	Sl_MBusy[0 :C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	Sl_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	Sl_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					

Table 1: **I/O Signal Descriptions *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P39	SI_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	SI_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P41	SI_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
Timebase Watchdog Timer Interface Signals					
P43	WDT_Reset	Timebase Watchdog Timer	O	0	Asserted upon second expiration of the WDT timeout interval. (Active High = '1').
P44	Timebase_Interrupt	Timebase Watchdog Timer	O	0	Asserted as a one clock period wide pulse upon rollover of the timebase from 0xFFFFFFFF to 0x00000000.
P45	WDT_Interrupt	Timebase Watchdog Timer	O	0	Asserted high and stays high until the WDS bit is cleared in the TWCSR0 register.

Design Parameters

To allow the user to obtain a XPS Timebase Watchdog Timer that is uniquely tailored for the system, certain features can be parameterized in the XPS Timebase Watchdog Timer design. This allows the user to configure a design that utilizes the resources required by the system only and that operates with the best possible performance. The features that can be parameterized are as shown in Table 2.

Table 2: **Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters					
G1	Target FPGA family	C_FAMILY			string
PLB Parameters					
G2	PLB base address	C_BASEADDR	Valid Address (1)	None[2]	std_logic_vector
G3	PLB high address	C_HIGHADDR	Valid Address[1]	None[2]	std_logic_vector
G4	PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer
G5	PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
G6	Shared bus topology	C_SPLB_P2P	0 = Shared bus topology[3]	0	integer
G7	PLB master ID bus Width	C_SPLB_MID_WIDTH	$\log_2$(C_SPLB_NUM_MASTERS) with a minimum value of 1	1	integer
G8	Number of PLB masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
G9	Width of the slave data bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
G10	Burst support	C_SPLB_SUPPORT_BURSTS	0 = No burst support[4]	0	integer

Table 2: **Design Parameters *(Cont'd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Timebase Watchdog Timer Parameters					
G11	Indicates the exponent for setting the length of the WDT interval. WDT interval = $2^{C\_WDT\_INTERVAL} \times T_{clk}$	C_WDT_INTERVAL	8 - 31	30	Integer
G12	Indicates WDT enable behavior	C_WDT_ENABLE_ ONCE	0 = WDT can be repeatedly enabled and disabled via software 1 = WDT can only be enabled once (no disable possible after initial enable)	1	Integer

Notes:

1. The range C_BASEADDR to C_HIGHADDR is the address range for the XPS SPI.This range is subject to restrictions to accommodate the simple address decoding scheme that is employed: The size, C_HIGHADDR - C_BASEADDR + 1, must be a power of two and must be at least 0x10 to accommodate all XPS SPI registers. However, a larger power of two may be chosen to reduce decoding logic. C_BASEADDR must be aligned to a multiple of the range size.
2. No default value will be specified to insure that an actual value appropriate to the system is set.
3. Point to point bus topology is not allowed.
4. Burst is not supported.

Parameter - Port Dependencies

The dependencies between the XPS Timebase Watchdog Timer core design parameters and I/O signals are described in Table 3.

Table 3: **XPS Timebase Watchdog Timer Parameter-Port Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_SPLB_DWIDTH	P7, P10, P33	-	Affects the number of bits in data bus
G7	C_SPLB_MID_WIDTH	P5	G8	This value is calculated as: $\log_2$(C_SPLB_NUM_MASTERS) with a minimum value of 1
G8	C_SPLB_NUM_MASTERS	P36, P37, P38, P42	-	Affects the number of PLB masters
I/O Signals				
P5	PLB_masterID[0 : C_SPLB_MID_WIDTH - 1]	-	G7	Width of the PLB_mastedID varies according to C_SPLB_MID_WIDTH
P7	PLB_BE[0 : (C_SPLB_DWIDTH/8) -1]	-	G5	Width of the PLB_BE varies according to C_SPLB_DWIDTH
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	-	G5	Width of the PLB_wrDBus varies according to C_SPLB_DWIDTH
P33	Sl_rdDBus[0 : C_SPLB_DWIDTH - 1]	-	G5	Width of the Sl_rdDBus varies according to C_SPLB_DWIDTH
P36	Sl_MBusy[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the Sl_MBusy varies according to C_SPLB_NUM_MASTERS

Table 3: **XPS Timebase Watchdog Timer Parameter-Port Dependencies *(Cont'd)***

Generic or Port	Name	Affects	Depends	Relationship Description
P37	SI_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MWrErr varies according to C_SPLB_NUM_MASTERS
P38	SI_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MRdErr varies according to C_SPLB_NUM_MASTERS
P42	SI_MIRQ[0 : C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MIRQ varies according to C_SPLB_NUM_MASTERS

Register Descriptions

Table 4 shows the XPS Timebase Watchdog Timer registers and their addresses.

Table 4: **XPS Timebase Watchdog Timer Registers**

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0	TWCSR0	Read/Write	0x0	Control/Status register-0
C_BASEADDR + 0x4	TWCSR1	Write (1)	0x0	Control/Status register-1, state is mirrored in TWCSR0 for read
C_BASEADDR + 0x8	TBR	Read (2)	0x0	Timebase register

Notes:

1. Reading of this register returns undefined value.
2. Writing into this register has no effect.

Control/Status Register-0 (TWCSR0)

Control/Status Register-0 contains the watchdog timer reset status, watchdog timer state, and watchdog timer enables. The TWCSR0 bit definitions are shown in Figure 3 and explained in Table 5.

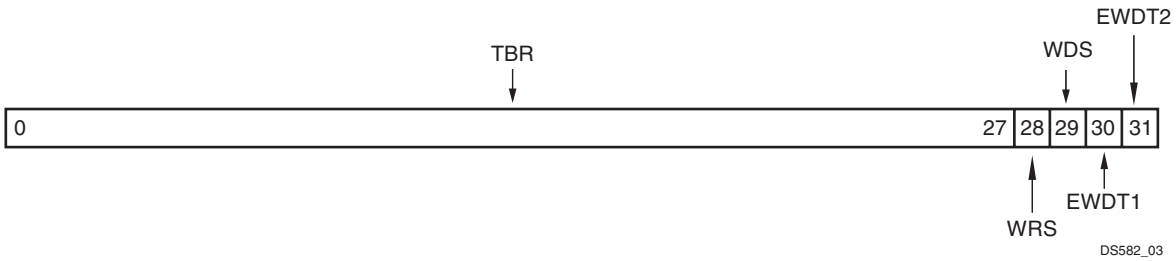

Figure 3: **Control/Status Register-0 (TWCSR0)**

Table 5: **Control/Status Register-0 (TWCSR0)**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 27	TBR	Read	0	Timebase Register (Most significant 28 bits): This read-only field contains the most significant 28 bits of the timebase register. The timebase register is mirrored here so that a single read can be used to obtain the count value and the watchdog timer state if the upper 28 bits of the timebase provide sufficient timing resolution.
28	WRS	Read/Write	'0'	Watchdog Reset Status: Indicates the WDT reset signal was asserted. This bit is not cleared by a system reset so that it can be read after a system reset to determine if the reset was caused by a watchdog timeout. Writing a '1' to this bit clears the watchdog reset status bit. Writing a '0' to this bit has no effect. '0' = WDT reset has not occurred '1' = WDT reset has occurred
29	WDS	Read/Write	'0'	Watchdog Timer State: Indicates the WDT period has expired. The WDT_Reset signal will be asserted if the WDT period expires again before this bit is cleared by software. Writing a '1' to this bit clears the watchdog timer state. Writing a '0' to this bit has no effect. '0' = WDT period has not expired '1' = WDT period has expired, reset will occur on next expiration
30	EWDT1	Read/Write	'0'	Enable Watchdog Timer (Enable 1): This bit must be used in conjunction with the EWDT2 bit in the TWCSR1 register. Both bits must be 0 to disable the WDT. '0' = Disable WDT function if EWDT2 also equals '0' '1' = Enable WDT function
31	EWDT2	Read	'0'	Enable Watchdog Timer (Enable 2): This bit is read only and is the only place to read back a value written to bit 31 of TWCSR1.

Control/Status Register-1 (TWCSR1)

Control/Status Register-1 contains the second Watchdog Timer (WDT) enable bit. The WDT enable must be cleared in both TWCSR0 and TWCSR1 to disable the WDT. If the WDT is configured as enable-once, then the WDT cannot be disabled after it has been enabled. The TWCSR1 bit definitions are shown in Figure 4 and explained in Table 6.

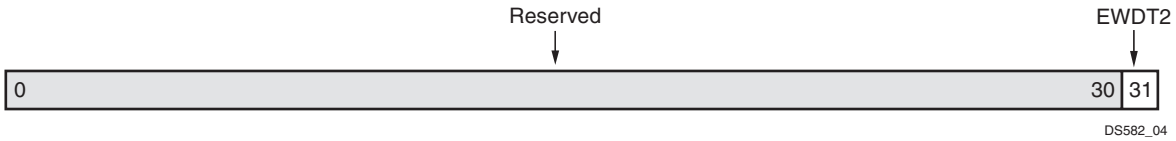

Figure 4: **Control/Status Register 1 (TWCSR1)**

Table 6: **Control/Status Register-1 (TWCSR1)**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 30	Reserved	N/A	N/A	Reserved
31	EWDT2	Write[1]	'0'	Enable Watchdog Timer (Enable 2): This bit must be used in conjunction with the EWDT1 bit in the TWCSR0 register to disable the WDT. Both bits must be 0 to disable the WDT. This bit is write-only in this register. The value of EWDT2 can be read back only in TWCSR1. '0' = Disable WDT function if EWDT1 also equals '0' '1' = Enable WDT function

Notes:

1. Reading of this register returns undefined value.

Timebase Register (TBR)

The TBR bit definitions are shown in Figure 5 and explained in Table 7.

The Timebase Register is the output of a free-running incrementing counter that clocks at the input clock rate (no prescaling of the clock is done for this counter). This register is read-only and is reset by the following:

- A system reset
- Enabling the WDT after power on reset
- Enabling the WDT after the WDT has been disabled. (EWDT1 and EWDT2 must both be '0' to disable the WDT.) The WDT is enabled when either EWDT1 or EWDT2 are set to '1'. Note that when the WDT mode is enable-once, the TBR can only be reset when the WDT is first enabled.

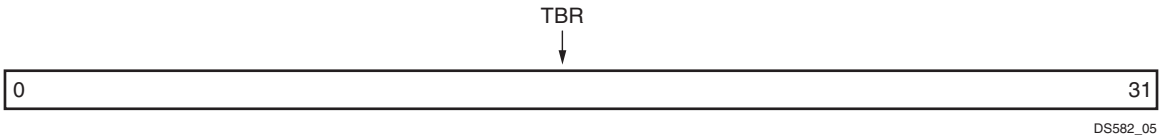

Figure 5: **Timebase Register (TBR)**

Table 7: **Timebase Register (TBR)**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 31	TBR	Read[Ref 1]	0	Timebase register: This register indicates the free-running incrementing counter value.

Notes:

1. Writing into this register has no effect.

Timing Diagrams

Figure 6 shows the WDT Expired Once operation waveform and Figure 7 shows the WDT Expired Twice operation waveform. The state of the WDT is given by the WDS bit in the TWCSR0 register. If the WDT interval expires while the WDS bit is '1', the WDT reset signal is asserted. An interrupt is provided when the WDS bit is set so that the software can clear the bit before the second expiration of the WDT. The WDS bit is cleared by writing a '1' to it. Writing a '0' to the WDS bit has no effect. Figure 6 shows the operation performed where WDS bit is cleared by the software before the second expiration occurs. Figure 7 shows the operation performed where WDS bit is not cleared and WDT expired twice state is reached.

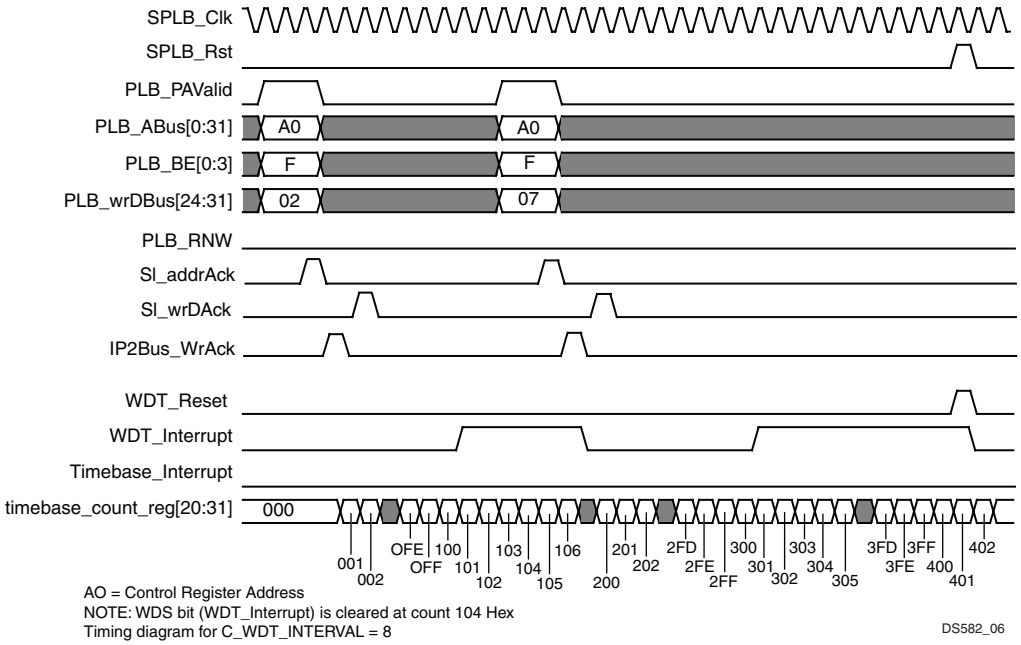

Figure 6: **WDT Expired Once Operation Waveform**

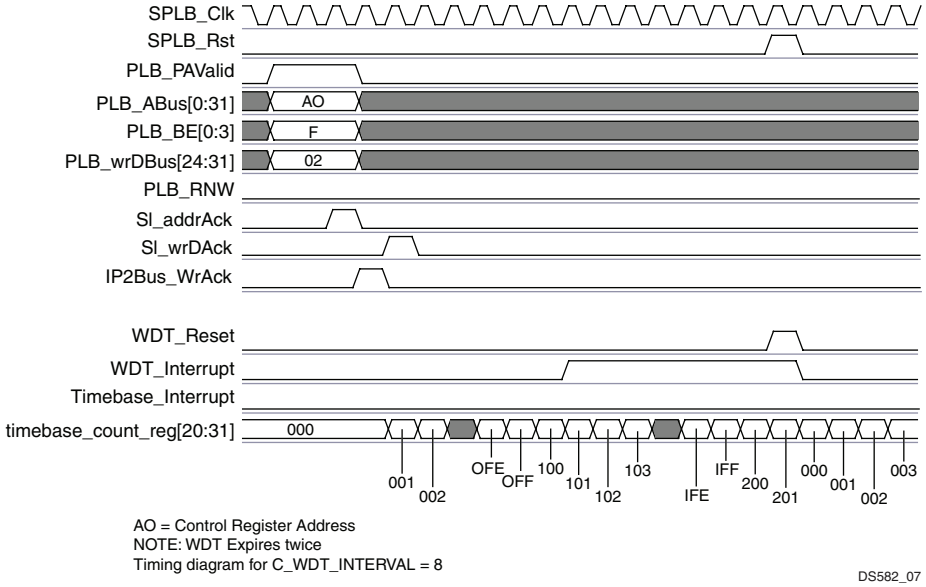

Figure 7: **WDT Expired Twice Operation Waveform**

Design Implementation

Target Technology

The intended target technology is an FPGA listed in the Supported Device Family field of the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

Core Performance

Since the XPS Timebase Watchdog Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the XPS Timebase Watchdog Timer core is combined with other designs in the system, the utilization of FPGA resources and timing of the XPS Timebase Watchdog Timer design will vary from the results reported here.

The XPS Timebase Watchdog Timer resource utilization for various parameter combinations measured with Virtex®-4 as the target device are detailed in Table 8.

Table 8: **Performance and Resource Utilization Benchmarks on the Virtex-4 FPGA (xc4vlx25-ff668-10)**

Parameter Values (Other parameters at default values)		Device Resources			Performance
C_WDT_INTERVAL	C_WDT_ENABLE_ONCE	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
8	0	66	56	104	146
30	1	65	56	106	133
31	1	65	56	106	139

The XPS Timebase Watchdog Timer resource utilization for various parameter combinations measured with Virtex-5 as the target device are detailed in Table 9.

Table 9: **Performance and Resource Utilization Benchmarks on the Virtex-5 FPGA (xc5vlx50-ff676-1)**

Parameter Values (Other parameters at default values)		Device Resources		Performance
C_WDT_INTERVAL	C_WDT_ENABLE_ONCE	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
8	0	56	76	198
30	1	56	78	184
31	1	56	78	209

The XPS Timebase Watchdog Timer resource utilization for various parameter combinations measured with Spartan®-3E as the target device are detailed in Table 10.

Table 10: **Performance and Resource Utilization Benchmarks on the Spartan-3E FPGA (xc3s1600e-fg320-4)**

Parameter Values (Other parameters at default values)		Device Resources			Performance
C_WDT_INTERVAL	C_WDT_ENABLE_ONCE	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
8	0	54	56	73	102
30	1	52	56	75	101
31	1	52	56	75	101

The XPS Timebase Watchdog Timer resource utilization for various parameter combinations measured with Spartan®-3E as the target device are detailed in Table 11.

Table 11: **Performance and Resource Utilization Benchmarks on the Spartan-6 FPGA (xc6slx45-2-fgg4844)**

Parameter Values (Other parameters at default values)		Device Resources			Performance
C_WDT_INTERVAL	C_WDT_ENABLE_ONCE	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
8	0	60	77	125	126
30	1	63	77	128	126
31	1	62	77	126	128

The XPS Timebase Watchdog Timer resource utilization for various parameter combinations measured with Spartan®-3E as the target device are detailed in Table 12.

Table 12: **Performance and Resource Utilization Benchmarks on the Virtex-6 FPGA (xc6vlx195t-1-ff1156)**

Parameter Values (Other parameters at default values)		Device Resources			Performance
C_WDT_INTERVAL	C_WDT_ENABLE_ONCE	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
8	0	67	77	139	197
30	1	73	77	139	212
31	1	71	77	139	206

System Performance

To measure the system performance (F_{MAX}) of this core, this core was added to a Virtex-4 system, a Virtex-5 system, a Spartan-3A system, a Virtex-6 system, and a Spartan-6 system as the Device Under Test (DUT) as shown in Figure 8, Figure 9, Figure 10, Figure 11 and Figure 12.

Because the XPS Timebase Watchdog Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other

designs in the system, the utilization of FPGA resources and timing of the core design will vary from the results reported here.

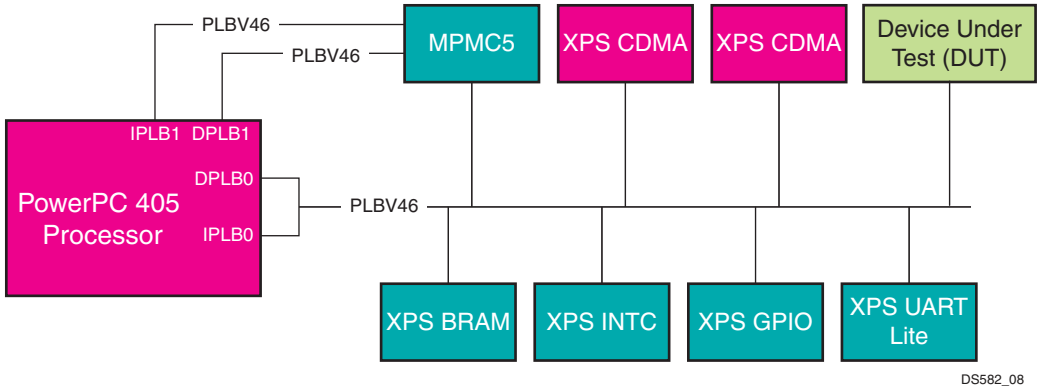

Figure 8: **System with the Virtex-4 FX FPGA as the DUT**

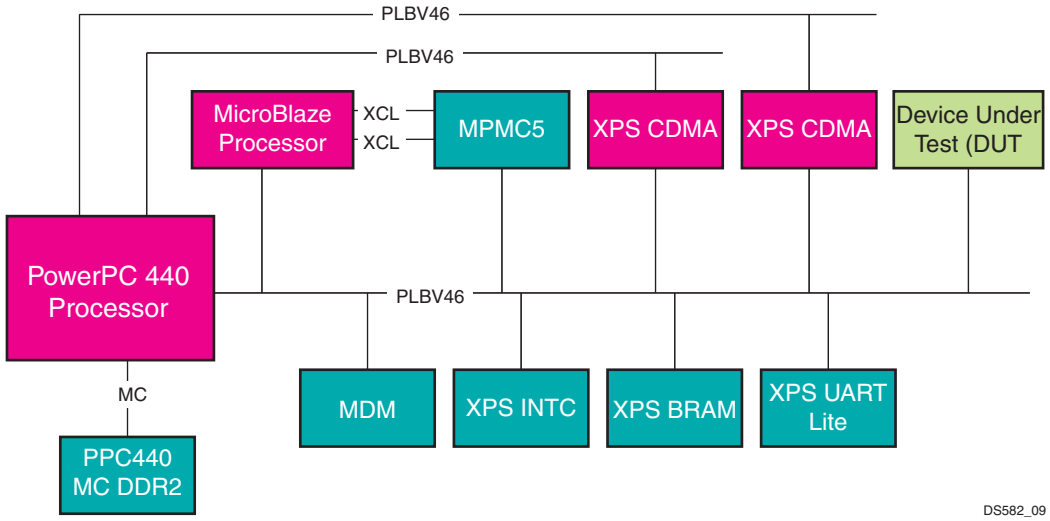

Figure 9: **System with the Virtex-5 FX FPGA as the DUT**

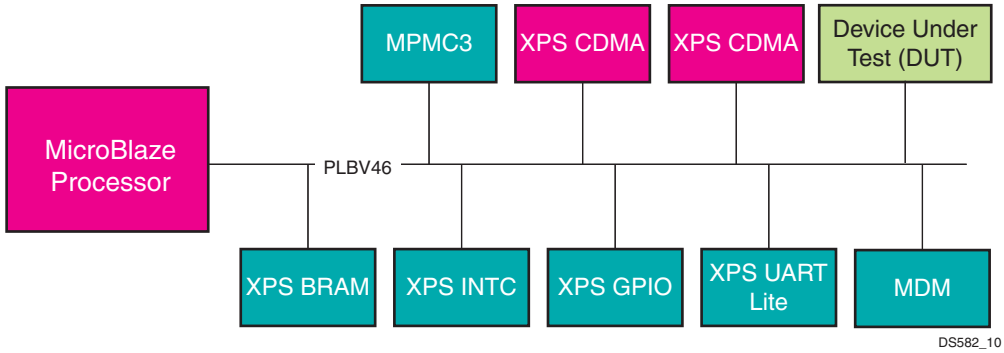

Figure 10: **System with the Spartan-3A FPGA as the DUT**

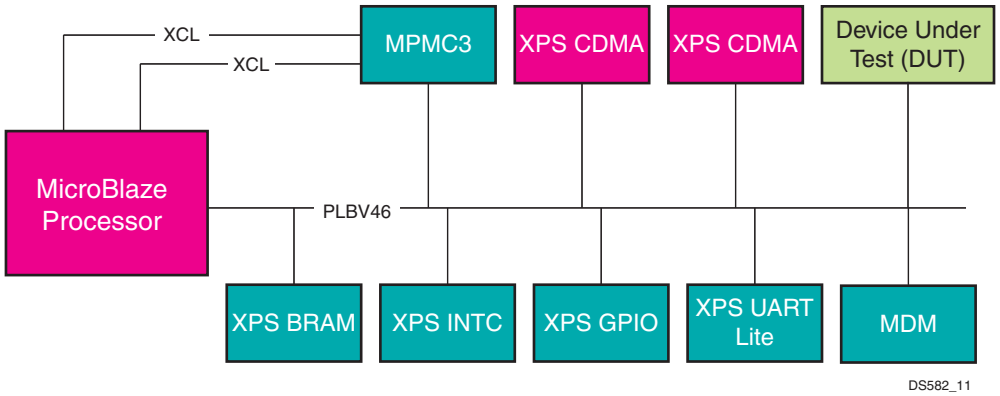

Figure 11: **System with the Virtex-6 FPGA as the DUT**

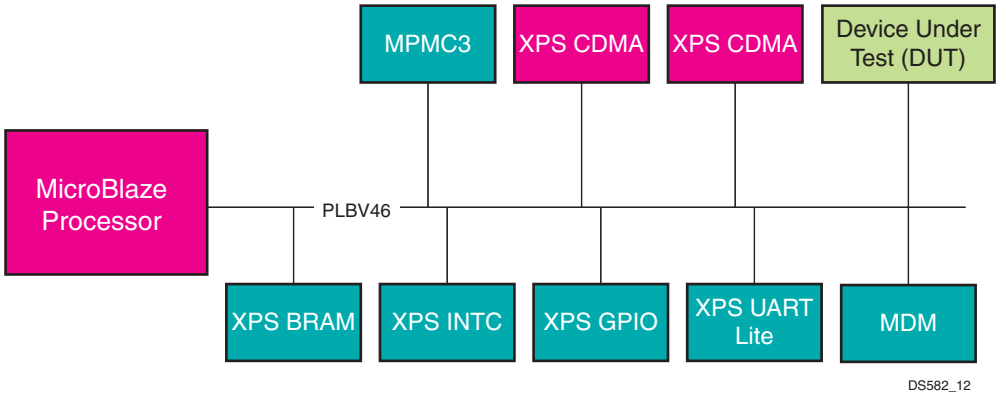

Figure 12: **System with the Spartan-6 FPGA as the DUT**

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 13.

Table 13: XPS Timebase Watchdog Timer System Performance

Target FPGA	Target F_{MAX} (MHz)
S3A700 -4	90
V4FX60 -10	100
V5FXT70 -1	120
V6LX130t - 1	150
S6LX45t - 2	100

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Reference Documents

1. IBM CoreConnect *128-Bit Processor Local Bus, Architectural Specification* (v4.6).

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK).

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Revision History

Date	Version	Description of Revisions
04/24/08	1.0	Initial Xilinx release.
4/24/09	1.1	Replaced references to supported device families, tool name(s), and parameter values with hyperlink to PDF file; converted to current DS template.
04/19/10	1.2	S6/V6 resource utilzation tables added
07/23/10	1.3	Updated to v1.02.a for the 12.2 release; converted to current DS template.

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