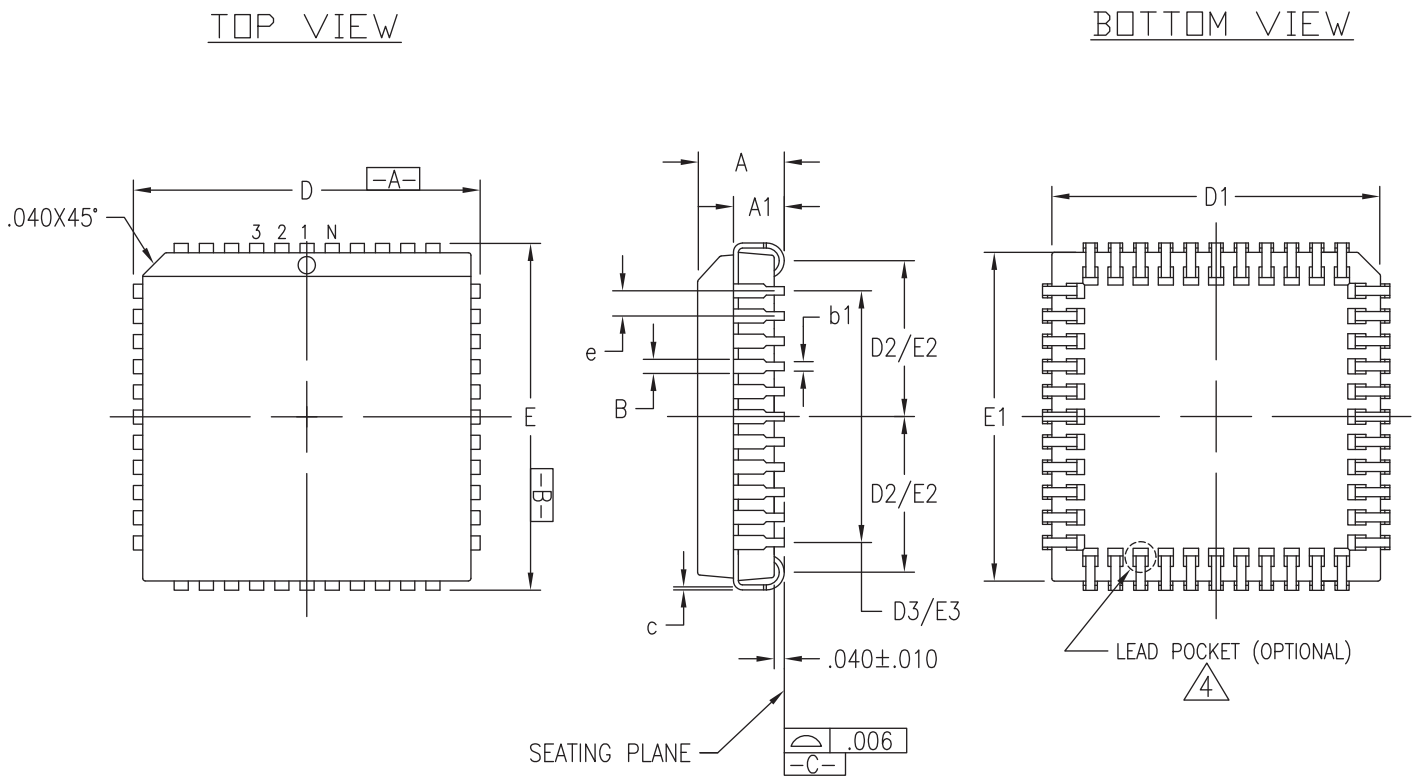
XILINX®

PK064 (v1.1) March 6, 2019

Ceramic Chip Carrier (CC44) Package



SYMBOL	INCHES		
	MIN	NOM	MAX
A	.155	.172	.190
A1	.090	---	.120
B	.026	.028	.032
b1	.017	.019	.022
c	.006	.007	.012
D/E	.685	.690	.695
D1/E1	.630	.650	.665
D2/E2	.290	.305	.320
D3/E3	.500 REF.		
e	.050 BSC		
N	44		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1982.
2. LEAD WIDTH DIMENSION INCLUDE LEAD TRIM OFFSET and LEAD FINISH, LEAD FINISH: (HOT SOLDER DIP) 63/37 Sn/Pb
3. SYMBOL 'N' IS THE NUMBER OF TERMINALS.
4. LEAD POCKET MAY OR MAY NOT EXIST ON THE PACKAGE.
5. THIS PACKAGE MEET DIMENSIONAL REQUIREMENTS OF JEDEC MO–087–AB

Figure 1: **Ceramic Chip Carrier (CC44)**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/28/2002	1.0	Initial Xilinx release.
03/06/2019	1.1	This package is obsolete per the Xilinx Product Change Notice *Hermetic Package Assembly Location Change for Defense-grade PROM and Virtex SMD Products* (XCN16002). See the replacement package: *CK44 Ceramic Leaded Chip Carrier (CLCC) Package* (PK444).