ALL PROGRAMMABLE SOLUTIONS FOR AUTOMOTIVE SYSTEMS
As Xilinx celebrates more than 30 years, 3,500 patents and 6,500 industry firsts, we also reflect on the remarkable progress of automotive technology over the same period. Nothing has been more transformative to the automobile than the electronics revolution which includes the introduction of the microprocessor into nearly every vehicle system from entertainment to engine controls. Software programmability has also resulted in a geometric progression of vehicle capability which has greatly enhanced the driver and passenger experience.

As millions of lines of software code become commonplace in many automotive systems, the next evolutionary surge of programmable electronic platforms is underway. This next frontier stems from the desire for the connected car that sees, understands, reacts, and communicates intuitively with the outside world and vehicle occupants; keeping them safe, informed, productive, and entertained.

The system flexibility and processing throughput, required for this next big step is exceeding what can practically be achieved in traditional software programmable embedded processors. Fixed hardware processors and application specific devices are giving way to all programmable devices and systems, where dynamic configuration and optimization of system hardware will be achieved with the same ease that system designers now take for granted in the software domain. This may seem far-fetched to some, but so did a million lines of embedded code in the early days of 8-bit controllers programmed in assembly language.

Xilinx is at the forefront of the this new challenge; reinventing and producing all programmable devices, SoCs, design tools, and — with our partners — the application solutions needed to realize the next generation of automotive electronic systems including Infotainment, Driver Information, and Advanced Driver Assistance Systems. Welcome to the future of automotive electronics.
Dedicated Automotive Product Line

Xilinx offers the most comprehensive, fully automotive-qualified FPGA and All Programmable SoC product lines in the market. With a wide variety of densities, packages and extended temperature grades, Xilinx began the XA (Xilinx Automotive) program in 2004, and has become the world’s leading supplier of automotive-grade programmable logic devices. The flexibility and scalability of the XA product line enables Xilinx customers to develop customized platforms to meet the demands for greater product differentiation and innovation. With the recent addition of the Zynq-7000 All Programmable SoC to the XA product line, Xilinx has revolutionized the automotive semiconductor industry with the first hardware and software programmable device to address the technical and business challenges for one of the fastest growing automotive applications: Advanced Driver Assistance Systems (ADAS).

These automotive-grade devices deliver increased system performance through a highly integrated architecture utilizing a hardened dual-core ARM processing system, coupled with programmable logic including DSP blocks for hardware acceleration, all on a single monolithic chip. The insatiable need for more bandwidth and performance, along with the programmable imperative, has arrived to the automotive market, and Xilinx’s XA product line continues to lead the way.

Beyond the AEC-Q100

Xilinx began its Xilinx Automotive (XA) program by testing according to the automotive AEC-Q100 qualification standard. However, it quickly became obvious that this standard is just a baseline, and many automotive suppliers and OEM automakers required further testing. Based on this acquired knowledge, starting with the 90nm XA Spartan-3A family, Xilinx created and began testing to “Beyond AEC-Q100.” Combining the automotive industry’s toughest test requirements from customers worldwide, Xilinx has created a world-class in-house semiconductor device qualification standard, doubling many of the AEC-Q100 test element requirements, and allowing shipment of high quality and robust XA products into the automotive market.

Click here for more information

About the Xilinx Zynq All Programmable SoC

The Xilinx Automotive (XA) Zynq-7000 All Programmable SoC is a highly integrated device with unprecedented design flexibility as it is a single chip that combines a dual core ARM Cortex-A9 processor system for serial application processing and system control, high-speed programmable I/O, and programmable logic including DSP blocks for hardware acceleration of critical design components. The programmability of this architecture enables end product differentiation with complete control of the IP, and can help system designers keep up with constantly changing feature requirements, especially in emerging application areas such as ADAS.

With the immense processing power of this integrated device, driver assistance systems that have typically utilized an FPGA (image capture and pixel-level processing), a DSP (object processing) and a microcontroller (frame-level processing, decision making and communication), can now replace these with one XA Zynq All Programmable SoC device, reducing overall system power, lowering system bill of material (BOM) costs, and system design complexity.

XA Spartan-6 FPGA Family

The XA Spartan-6 family of products was built to offer an optimal balance of cost, power and performance. The Spartan-6 LX FPGAs are cost-optimized for logic, DSP slices and memory, while the Spartan-6 LX FPGAs also include embedded 3.125Gbps low-power serial transceivers, along with PCIe interface cores for high-speed serial connectivity. With various densities in the same package, automotive Tier One designers can choose the right-sized FPGA device for their OEM vehicle platform needs.

XA Artix-7 FPGA Family

The Artix-7 is a low-power and high-performance FPGA device line-up available in smaller packages. With a range of devices from 35k logic cells to 100k logic cells, the highest BRAM and DSP block ratios available in the XA product line, integration of Analog Mixed Signal and 6.25Gbps transceivers for the latest serial interface standards, such as PCIe Gen 2, the Artix-7 FPGAs can be utilized for key automotive applications requiring high performance. The enhanced productivity of the Vivado® Design Suite, and design optimization techniques such as clock gating through the tool, enables as much as 50% total power reduction over XA Spartan-6.
Rapid Algorithm Deployment

All Programmable Abstractions, through system modelling environment Alliance Members like the MathWorks® and National Instruments®, allow system engineers to evaluate the feasibility and performance of their algorithms on all programmable FPGAs and SoCs early in the development process to optimize system performance through hardware/software partitioning. These abstractions automate the rapid deployment of algorithms onto application specific hardware platforms interfaced to real-world signals, videos or networks.

For model-based design, the MathWorks has released a new guided workflow which enables software developers and hardware design engineers to create and model their algorithms in MATLAB™ and Simulink™, partition their designs between software and hardware, and automatically target, integrate, debug and test those models on Xilinx targeted design platforms for Zynq-7000 All Programmable SoC devices.

The new flow helps users to partition an algorithm into software and hardware modules and then generate C code for the ARM processor-based Zynq All Programmable SoC with the MathWorks Embedded Coder and RTL code for the programmable logic using the MathWorks HDL Coder or Xilinx’s System Generator.

Vivado IP Integrator

The Vivado Design Suite is also now delivering intelligent IP integration with the new IP Integrator feature. Vivado IP Integrator (IPI), provides a graphical and Tcl based, correct by-construction, IP- and system-centric design development flow. This integration environment is platform aware which simplifies the integration of hardware board peripherals and device aware to ensure that maximum system bandwidth is achieved.

C-Based IP Generation with Vivado High-Level Synthesis

Advanced algorithms used today in applications like Advanced Driver Assistance Systems (ADAS) are more sophisticated than ever before. To model these algorithms, many design teams turn to C/C++ or SystemC because of the sheer simulation performance over RTL-based simulations, making the process up to a thousand times faster. The challenge becomes the need to recode these algorithms in RTL for hardware implementation which is time consuming and error prone.

With C-based IP generation with Vivado High-level Synthesis (HLS), this process is greatly accelerated, by enabling the C specification to be directly targeted into Xilinx all programmable devices without the need to manually create RTL. Vivado HLS is part of the Vivado Design Suite, System Edition.

Vivado High-Level Synthesis automatically generates the hardware description for a given C code using its library of fixed-point arithmetic, functions, and operations. The C code is compiled with the GNU Compiler Collection (GCC) and the source code is transformed into a combination of register transfer level (RTL) code and C code which is optimized and synthesized into hardware. This process enables the rapid deployment of algorithms onto application specific hardware platforms interfaced to real-world signals, videos or networks.

SDAccel™ Development Environment

Part of the SDx™ family of development environments for systems and software engineers, the SDAccel development environment helps customers to achieve up to 25X better performance/watt when designing FPGAs. It’s the industry’s first architecturally optimizing compiler supporting any combination of OpenCL, C, and C++ kernels, along with libraries, development boards, and the first complete CPU/GPU-like development and run-time experience for FPGAs.

The integrated design environment (IDE) provides coding templates and software libraries, and enables compiling, debugging, and profiling against the full range of development targets including emulation on x86, performance validation using fast simulation, and native execution on FPGA processors.
**Xilinx in ADAS**

The XA product family of FPGAs and All Programmable SoC devices are well-suited to meet the needs of today’s Forward-Looking Camera ADAS systems. In these applications, a wide variety of features are based on complex image analytics from single camera video sequences. Diverse analytics methods are needed to support each feature—from a classification process for Pedestrian Detection, to pattern recognition for Traffic Sign Recognition. Additionally, unique RF and antenna control functions can be processed automatically in real time.

The Zynq All Programmable SoC and its fine-grain programmable logic allow developers to create independent and simultaneous processing paths to carry out the full calculations with hardware acceleration support. Additionally, high bandwidth interconnect allows the multi-core Cortex A9s to exchange data with the hardware accelerators and run multi-threaded applications which complete the functionality of each feature from a software perspective.

Further processing power is required with the inclusion of a second camera to add stereo perspective. The ability to create independent hardware processing channels for various features is a key enabler in allowing developers to create vehicle-specific feature bundles. And because each processing chain can be fully customized, customers can now differentiate their ADAS system performance from the competition.

As an alternative to the centralized approach of today’s ADAS systems, the centralized multi-sensor fusion model is under consideration. The Zynq All Programmable SoC offers a unique platform to develop and deliver these type of systems. The Zynq All Programmable SoC off-chip DDR controller subscriptions can be accommodated on the Zynq All Programmable SoC. Additionally, unique RF and antenna control functions can be processed automatically in real-time.

Creating effective ADAS systems require characterisation of the vehicle driving environment with higher fidelity than previously achieved. This technological challenge is accompanied by previous to reduce system development costs.

One approach is to create multi-modal radar systems which provide the required detection sensitivity at long ranges as well as high resolution spatial discrimination at near ranges over a wide field of view. Creating such a sensor means combining complex antenna structures, adaptive front-end RF electronics, and powerful back-end digital processing. For these types of sensor architectures, the Zynq All Programmable SoC is a natural fit.
Connected to the Future

Many new functions of next generation cars like semi-autonomous driver assistance, car-to-x communication or advanced user interfaces are distributed and leverage different ECUs. This trend drives significant changes in the vehicle’s network architecture and the required bandwidth. In addition telematics and connectivity with consumer devices like tablets or smartphones drive new external communication standards with increased security requirements.

Xilinx XA FPGAs provide the performance for high-bandwidth and low-latency communication with strong security. These devices offer the flexibility to quickly adopt new communication standards while allowing maximum integration to minimize BOM cost and use of PCB real estate.

Companion Chip Design Platform

Xilinx XA FPGAs offer high bandwidth combined with programmable I/Os. They deliver performance, flexibility and scalability to implement multiple bridging solutions around a host processor on a single FPGA. With pin compatibility between the same packages through multiple device densities the design can be optimized for multiple ECU variants reducing BOM costs and power. The Xilinx Automotive Companion Chip Platform provides flexible interfacing and is optimized to complement a variety of host processors. A rich portfolio of available IP and software enables rapid extension of system interfaces, peripherals or processing with minimal development effort. Various popular host processor interfaces are supported and can be changed quickly based on host availability and overall bandwidth requirements.

Augmented Reality HMI Solution

Augmented reality using eye tracking, gesture recognition, 3D reconstruction based on Structure from Motion and perspective rendering requires massive parallel processing. The scalable Xilinx XA Zynq All Programmable SocC family provides the right mix of power efficient parallel processing in the programmable logic and ARM processor performance to implement advanced HMI solutions in a cost efficient way in a single chip. The LogiADAK reference platform enables short time to market. The Xilinx XA Zynq solution can be used as a stand-alone center stack solution or augmented reality companion inside the head unit.

New HMI Experience

With more communication services like in-vehicle Internet access and Advanced Driver Assistance functions now available in cars, driver distraction is a real challenge. One possible solution is a more natural Human Machine Interface (HMI) that includes augmented reality (AR) technologies and driver distraction monitoring. This will give the driver a differentiating and completely new experience of interacting with the car by integrating camera based eye tracking and gesture detection. High-resolution wide-angle head-up displays will provide the driver all the information required while leading to minimum distraction. AR combines information from internal and external cameras with a rendered graphics overlay.
Why Intellectual Property?
As today's designs integrate increasing amounts of functionality, designers must have access to proven, up-to-date, easy-to-use Intellectual Property (IP) from reliable sources to accelerate their design cycles. The ability to deliver high-performance systems at the lowest total design cost on time and within budget depends upon the ability to rapidly combine and configure dozens or hundreds of design elements. These include on-chip blocks, processor cores, and a wide range of IP cores. Xilinx's growing IP portfolio is the response to the growing customer demand for system-level support. These IP blocks combined with Xilinx all programmable devices families including FPGAs, SoCs and 3D ICs allows design teams to maximize system performance, lower power consumption, and reduce BOM costs with maximum design flexibility across a wide range of end markets and target applications. To ensure portability and interoperability among IP from Xilinx and its Alliance members, Xilinx has taken a standards-based approach.

Xilinx offers via our AUTOSAR partner ARCCORE a high-quality, efficient, reliable and scalable AUTOSAR-compliant set of Microcontroller Abstraction Layer (MCAL) drivers for the Xilinx XA Zynq family. The drivers are developed in an automotive SPICE level 3 process framework and can be used in ECU’s developed according to ISO26262. Supported are the industry standard compilers GCC and ARM Compiler 5. The MCAL drivers are provided with a command-line based code generator to be integrated in any AUTOSAR configuration tool and basic software. In addition, ARCCORE offers a complete AUTOSAR solution for the Zynq All Programmable SoC with their Arctic Core Embedded Software platform and the Arctic Studio Development Tooling.

AUTOSAR software Package

AUTOSAR standardizes the basic automotive ECU software functionality including operating system and basic services like communication and diagnosis. An RTE based on a virtual functional bus abstracts the underlying hardware. AUTOSAR also includes an ECU development methodology which allows scalability for different vehicle and platform variants re-use of software and support of different functional domains.

Premier Automotive Partner IP Examples

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<tr>
<th>IP provider</th>
<th>IP core</th>
<th>Description</th>
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<tr>
<td>Xilinx</td>
<td>CAN FD</td>
<td>CAN 2.0B compatible network controller supporting FD protocol extension</td>
</tr>
<tr>
<td>Xilinx</td>
<td>CAN</td>
<td>CAN 2.0B compatible network controller</td>
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<td>Xylon</td>
<td>logiVIEW</td>
<td>Perspective Transformation and Lens Correction Image Processor</td>
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<td>Xylon/vES</td>
<td>logiPDET</td>
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<td>Xylon</td>
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<td>Versatile Video Input Controller</td>
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<td>Xylon</td>
<td>logiBITBLT</td>
<td>Bit Block Transfer 2D Graphics Accelerator</td>
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<td>Xylon</td>
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<td>CAN 2.0B compatible network controller</td>
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<td>Xylon</td>
<td>logiBAYER</td>
<td>Color Camera Sensor Bayer Decoder</td>
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<td>Xylon</td>
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<td>Audio I2S Transmitter/Receiver</td>
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<td>Xylon</td>
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<td>Xylon</td>
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<td>SD Card Host Controller</td>
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Click here for information
ISO 26262
The standard ISO 26262 is an adaptation of the functional safety standard IEC 61508 for automotive electric/electronic systems. ISO 26262 defines functional safety for automotive equipment applicable throughout the lifecycle of all automotive electronic and electrical safety-related systems. It covers functional safety aspects of the entire development process, starting with requirements specification, design, implementation, verification, validation, and configuration.

ISO 26262-8:2011 according to IEC 61508-3:2010 has been certified by TÜV SÜD.

ISE Design Suite – Xilinx FPGA
ISE Design Suite allows the user to leverage the benefits of the FPGA while meeting the functional safety requirements imposed by the established standards.

Xilinx provides a certified and comprehensive functional safety design flow solution for FPGAs and All Programmable SoCs which includes:
- Certificate and reports
- FPGA design and verification tools and methodologies
- IP and devices

This solution delivers essential project documentation and guidelines along with functional safety system IP, and significantly helps shorten the customer’s certification process.

Xilinx’s unique and certified functional safety design methodologies allow customers to integrate safety with general applications in the same device. Xilinx’s Isolation Design Flow (IDF) and Isolation Verification Tools (IVT) provide a certified methodology to separate areas on the FPGA.

Designs can be placed into these areas and physically isolated. The areas can be changed at any time without impacting other isolated locations, proven by the IVT tools.

Design with Confidence
- Alliance members provide products across all technology and market solutions relevant to customer needs
- Members demonstrate the highest quality, expertise, and customer satisfaction standards
- Deliver Better Products Faster
  - Leverage leading-edge products from members to improve overall system performance while minimizing resource utilization
  - Accelerate product development by easily integrating member solutions with your design on Xilinx technologies
  - Reduce design integration time through solutions supporting industry key standards such as AMBA AXI4 and FMC

Instant Access to a Comprehensive Ecosystem
- Easily identify required expertise from a wide range of qualified companies
- Quickly find member solutions supporting Xilinx All Programmable devices

Instant Access to a Comprehensive Ecosystem
- Easy to find solutions that help customers save time and money
- Help customers meet their design goals

Automotive Ecosystem
To realize the next generation of automotive solutions in Infotainment, Driver Information and Advanced Driver Awareness Systems, Xilinx is delivering a portfolio of all programmable devices, SoCs, design tools and automotive application solutions. To deliver these application solutions, Xilinx leverages the best in the industry by maintaining an Ecosystem of trusted companies with proven solutions on Xilinx platforms, stable business and technical processes, and automotive market experience.

These automotive alliance partners complement the Xilinx portfolio by providing high quality IP, solutions and design services that enable our customers to succeed with their toughest design challenges.

Functional Safety Requirements
Xilinx FPGAs and All Programmable SoCs are used at the heart of products that comply with functional safety requirements. Designers are specifically concerned with how to leverage the benefits of the FPGA while meeting the functional safety requirements imposed by the established standards.

Xilinx provides a comprehensive and functional safety design flow solution for FPGAs and All Programmable SoCs which includes:
- Certificate and reports
- FPGA design and verification tools and methodologies
- IP and devices

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Click here for information

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### ZYNQ XC7A200T All Programmable SoC

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<th>Z-7020</th>
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<tr>
<td>Part Number</td>
<td>AX7520</td>
<td>AX7530</td>
<td>AX7530</td>
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**Processor Core**
- Dual ARM Cortex-A9 with TrustZone™
- Dual Core: 950 MHz
- Dual Core: 950 MHz

**Processor Resources**
- 64-bit Memory

**Memory Resources**
- 32 KB Instruction, 32 KB Data per processor
- 512 KB

**On-Chip Memory**
- 1056 KB

**External Memory Support**
- DDR2, DDR3, HMC, NOR

**DMA Channels**
- 8 (dedicated to Programmable Logic)

**Peripheral Fabric Block (MBA)**
- 2x USB 2.0 (OTG), 2x TQ-coded Gigabit Ethernet, 2x 10G DDR

**Security**
- AES and SHA 256 Decryption and Authentication for Secure Boot

**Integrated Peripherals**
- 2x 12-bit, MSP430 ADCs with up to 17 Differential Inputs

**Max LUTs**
- 157,600

**Flip-Flops**
- 105,408

**Embedded Block RAM (ReProgrammable)**
- 244 KB (99)

**Programmable DSP (Total 3600+)**
- 2x 128x16, MPS430 ADCs with up to 17 Differential Inputs

**Multi-Standards and Multi-Voltage SelectIO**
- 2x PCIe (Full-Speed)

**Clock Resources**
- 66555

**Pitch**
- 0.8 mm

**Size**
- 13x13 mm

**Package**
- X-MLB (v1.1)

**Notes:**
1. Supports PCI Express Base 2.1 specification @ Gen1 and Gen2 data rates.
2. GTP transceivers: 6.25 Gb/s available in -2 speed grade only; 3.75 Gb/s in -1 speed grade.
3. Package varies with the usage of many peripherals that could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
4. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

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### XA Artix-7 FPGAs

**Optimized for Lowest Cost and Lowest Power Applications**

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**Notes:**
1. Supports PCI Express Base 2.1 specification @ Gen1 and Gen2 data rates.
2. GTP transceivers: 6.25 Gb/s available in -2 speed grade only; 3.75 Gb/s in -1 speed grade.

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**Important:** Verify all data in this document with the device data sheets found at www.xilinx.com.
### Spartan-6 FPGA Descriptions

#### Spartan-6 LX FPGAs

- **Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V)**

<table>
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<tr>
<th>Part Number</th>
<th>Spartan-6 LX6000</th>
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<th>Spartan-6 LX9000</th>
<th>Spartan-6 LX1500</th>
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#### Spartan-6 LX FPGAs

- **Optimized for Lowest-Cost Logic, DSP, and Memory with Serial Connectivity (1.2V)**

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### Spartan-3E FPGAs

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### Spartan-3E FPGAs

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### Important Notes

1. Verify all data in this document with the device data sheets found at www.xilinx.com.